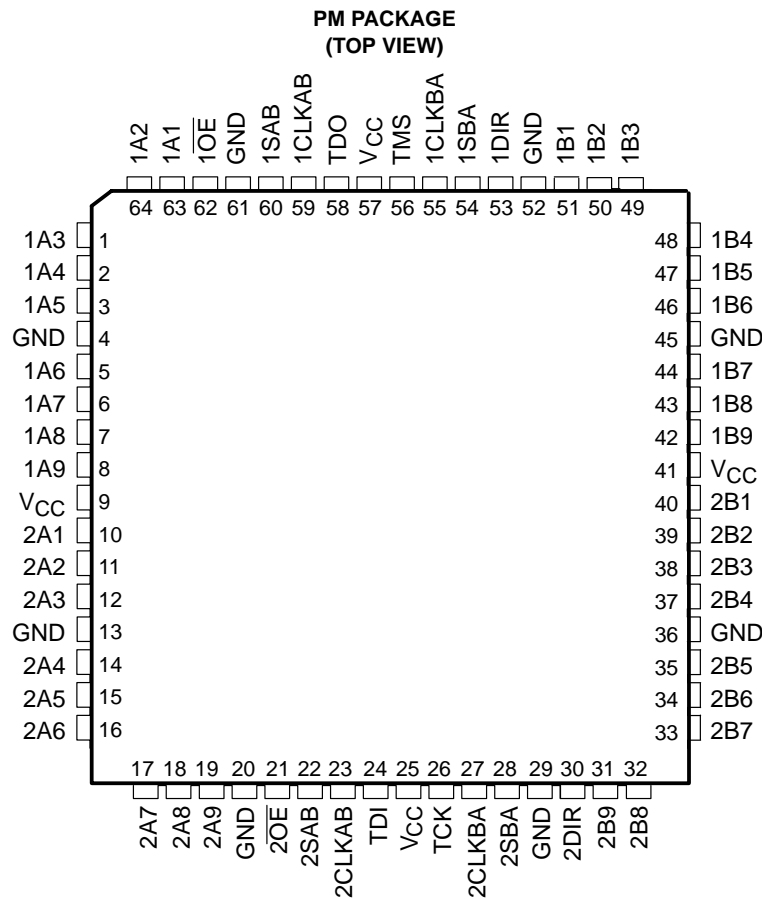


**SN74ABT18646**  
**SCAN TEST DEVICE**  
**WITH 18-BIT TRANSCEIVER AND REGISTER**  
SCBS131A – AUGUST 1992 – REVISED JANUARY 2002

- **Member of the Texas Instruments Widebus™ Family**
- **Compatible With IEEE Std 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture**
- **Includes D-Type Flip-Flops and Control Circuitry to Provide Multiplexed Transmission of Stored and Real-Time Data**
- **Two Boundary-Scan Cells Per I/O for Greater Flexibility**
- **SCOPE™ Instruction Set**
  - IEEE Std 1149.1-1990 Required Instructions, Optional INTEST, and P1149.1A CLAMP and HIGHZ
  - Parallel Signature Analysis at Inputs With Masking Option
  - Pseudorandom Pattern Generation From Outputs
  - Sample Inputs/Toggle Outputs
  - Binary Count From Outputs
  - Device Identification
  - Even-Parity Opcodes



**description**

This scan test device with a 18-bit bus transceiver and register is a member of the Texas Instruments SCOPE™ testability IC family. This device supports IEEE Std 1149.1-1990 boundary scan to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the four-wire test access port (TAP) interface.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SCOPE and Widebus are trademarks of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2002, Texas Instruments Incorporated

# SN74ABT18646 SCAN TEST DEVICE WITH 18-BIT TRANSCEIVER AND REGISTER

SCBS131A – AUGUST 1992 – REVISED JANUARY 2002

## description (continued)

In the normal mode, this device is an 18-bit bus transceiver and register that allows for multiplexed transmission of data directly from the input bus or from the internal registers. It can be used either as two 9-bit transceivers or one 18-bit transceiver. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self-test on the boundary test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPE bus transceivers and registers.

Transceiver function is controlled by output-enable ( $\overline{OE}$ ) and direction (DIR) inputs. When  $\overline{OE}$  is low, the transceiver is active and operates in the A-to-B direction when DIR is high or in the B-to-A direction when DIR is low. When  $\overline{OE}$  is high, both the A and B outputs are in the high-impedance state, effectively isolating both buses.

Data flow is controlled by clock (CLKAB and CLKBA) and select (SAB and SBA) inputs. Data on the A bus is clocked into the associated registers on the low-to-high transition of CLKAB. When SAB is low, real-time A data is selected for presentation to the B bus (transparent mode). When SAB is high, stored A data is selected for presentation to the B bus (registered mode). The function of the CLKBA and SBA inputs mirrors that of CLKAB and SAB, respectively. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the SN74ABT18646.

In the test mode, the normal operation of the SCOPE bus transceivers and registers is inhibited, and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry can perform boundary scan test operations according to the protocol described in IEEE Std 1149.1-1990.

Four dedicated test pins are used to observe and control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry can perform other testing functions, such as parallel signature analysis on data inputs and pseudorandom pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

Additional flexibility is provided in the test mode through the use of two boundary scan cells (BSCs) for each I/O pin. This allows independent test data to be captured and forced at either bus (A or B). A PSA/COUNT instruction is also included to ease the testing of memories and other circuits where a binary count addressing scheme is useful.

## ORDERING INFORMATION

| TA            | PACKAGE†  |      | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---------------|-----------|------|-----------------------|------------------|
| -40°C to 85°C | LQFP – PM | Tray | SN74ABT18646PM        | ABT18646         |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

**SN74ABT18646**  
**SCAN TEST DEVICE**  
**WITH 18-BIT TRANSCEIVER AND REGISTER**

SCBS131A – AUGUST 1992 – REVISED JANUARY 2002

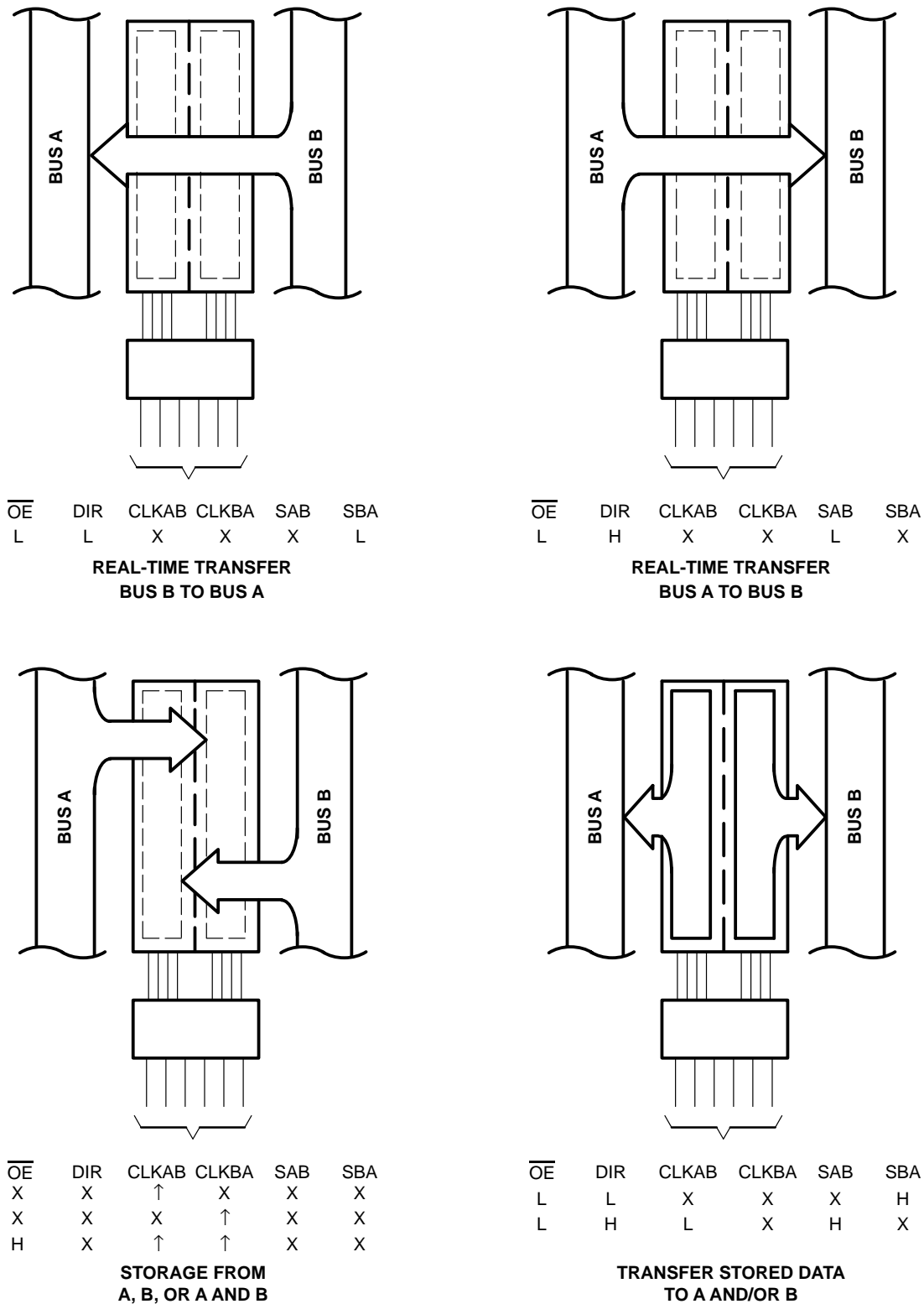
**FUNCTION TABLE**  
(normal mode, each 9-bit section)

| INPUTS |     |       |       |     |     | DATA I/O       |                | OPERATION OR FUNCTION     |
|--------|-----|-------|-------|-----|-----|----------------|----------------|---------------------------|
| OE     | DIR | CLKAB | CLKBA | SAB | SBA | A1–A9          | B1–B9          |                           |
| X      | X   | ↑     | X     | X   | X   | Input          | Unspecified†   | Store A, B unspecified†   |
| X      | X   | X     | ↑     | X   | X   | Unspecified†   | Input          | Store B, A unspecified†   |
| H      | X   | ↑     | ↑     | X   | X   | Input          | Input          | Store A and B data        |
| H      | X   | L     | L     | X   | X   | Input disabled | Input disabled | Isolation, hold storage   |
| L      | L   | X     | X     | X   | L   | Output         | Input          | Real-time B data to A bus |
| L      | L   | X     | X     | X   | H   | Output         | Input disabled | Stored B data to A bus    |
| L      | H   | X     | X     | L   | X   | Input          | Output         | Real-time A data to B bus |
| L      | H   | L     | X     | H   | X   | Input disabled | Output         | Stored A data to B bus    |

† The data output functions can be enabled or disabled by various signals at the OE and DIR inputs. Data input functions are always enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

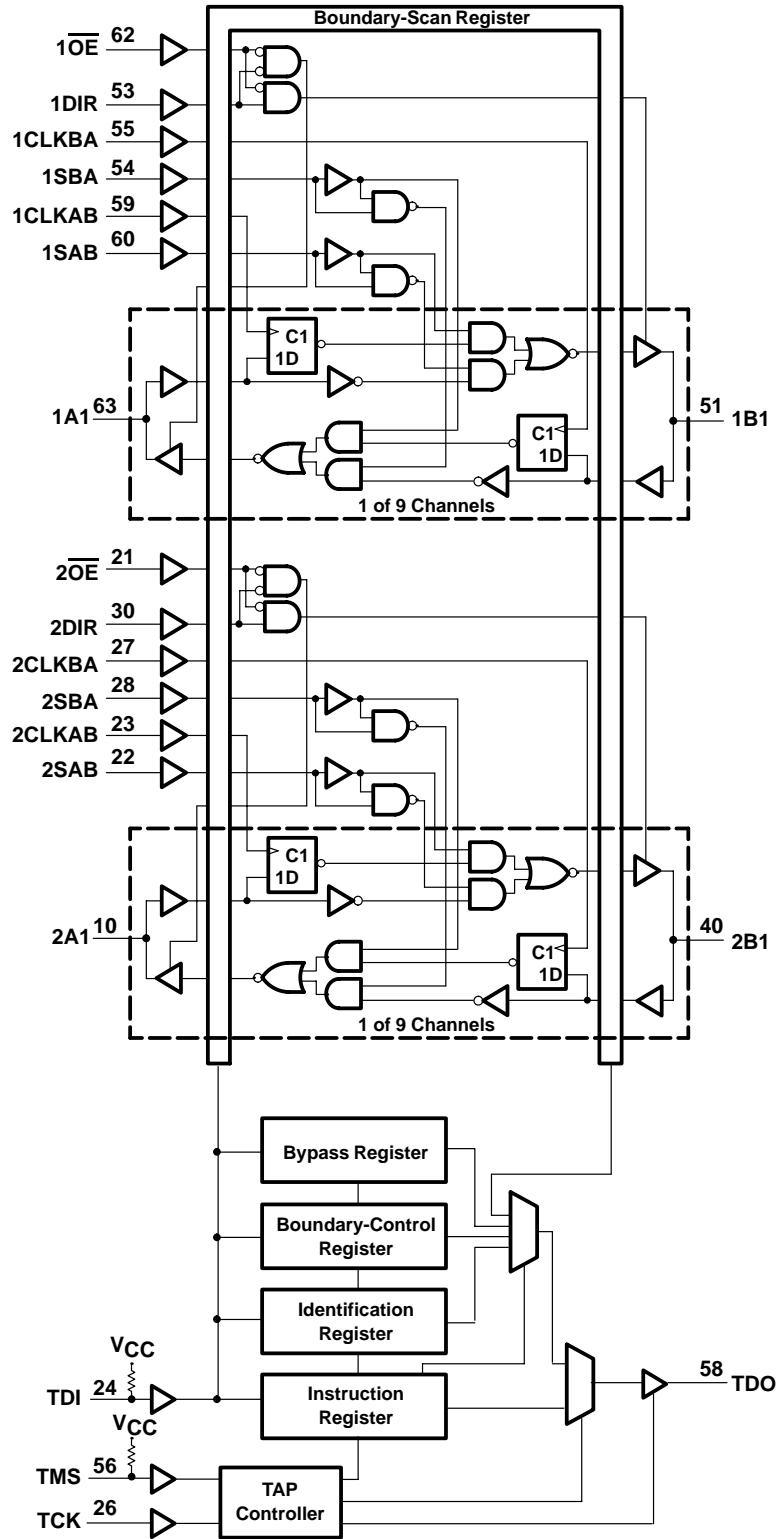
**SN74ABT18646**  
**SCAN TEST DEVICE**  
**WITH 18-BIT TRANSCEIVER AND REGISTER**

SCBS131A – AUGUST 1992 – REVISED JANUARY 2002



**Figure 1. Bus-Management Functions**

functional block diagram



**SN74ABT18646**  
**SCAN TEST DEVICE**  
**WITH 18-BIT TRANSCEIVER AND REGISTER**

SCBS131A – AUGUST 1992 – REVISED JANUARY 2002

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

|   |                 |
|---|-----------------|
| Supply voltage range, $V_{CC}$  | –0.5 V to 7 V   |
| Input voltage range, $V_I$ : Except I/O ports (see Note 1)                      | –0.5 V to 7 V   |
| I/O ports (see Note 1)  | –0.5 V to 5.5 V |
| Voltage range applied to any output in the high state or power-off state, $V_O$ | –0.5 V to 5.5 V |
| Current into any output in the low state, $I_O$                                 | 128 mA          |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ )                                     | –18 mA          |
| Output clamp current, $I_{OK}$ ( $V_O < 0$ )                                    | –50 mA          |
| Package thermal impedance, $\theta_{JA}$ (see Note 2)                           | 34°C/W          |
| Storage temperature range, $T_{stg}$  | –65°C to 150°C  |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. The package thermal impedance is calculated in accordance with JESD 51-7.

**recommended operating conditions (see Note 3)**

|  | MIN | MAX      | UNIT |
|--|-----|----------|------|
| $V_{CC}$ Supply voltage                                | 4.5 | 5.5      | V    |
| $V_{IH}$ High-level input voltage                      | 2   |          | V    |
| $V_{IL}$ Low-level input voltage                       |     | 0.8      | V    |
| $V_I$ Input voltage                                    | 0   | $V_{CC}$ | V    |
| $I_{OH}$ High-level output current                     |     | –32      | mA   |
| $I_{OL}$ Low-level output current                      |     | 64       | mA   |
| $\Delta t/\Delta v$ Input transition rise or fall rate |     | 10       | ns/V |
| $T_A$ Operating free-air temperature                   | –40 | 85       | °C   |

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 4)**

| PARAMETER          | TEST CONDITIONS   |                                  | MIN                                | TYP† | MAX       | UNIT          |
|--------------------|---|----------------------------------|------------------------------------|------|-----------|---------------|
| $V_{IK}$           | $V_{CC} = 4.5\text{ V}$ ,   | $I_I = -18\text{ mA}$            |                                    |      | -1.2      | V             |
| $V_{OH}$           | $V_{CC} = 4.5\text{ V}$ ,   | $I_{OH} = -3\text{ mA}$          | 2.5                                |      |           | V             |
|                    | $V_{CC} = 4.5\text{ V}$ ,   | $I_{OH} = -32\text{ mA}$         | 2                                  |      |           |               |
| $V_{OL}$           | $V_{CC} = 4.5\text{ V}$ ,   | $I_{OL} = 64\text{ mA}$          |                                    |      | 0.55      | V             |
| $I_I$              | $V_{CC} = 5.5\text{ V}$ ,   | $V_I = V_{CC}$ or GND            | CLK, DIR, $\overline{OE}$ , S, TCK |      | $\pm 1$   | $\mu\text{A}$ |
|                    |   |                                  | A or B ports                       |      | $\pm 100$ |               |
| $I_{IH}$           | $V_{CC} = 5.5\text{ V}$ ,   | $V_I = V_{CC}$ ,                 | TDI, TMS                           |      | 10        | $\mu\text{A}$ |
| $I_{IL}$           | $V_{CC} = 5.5\text{ V}$ ,   | $V_I = \text{GND}$ ,             | TDI, TMS                           |      | -150      | $\mu\text{A}$ |
| $I_{OZH}^\ddagger$ | $V_{CC} = 5.5\text{ V}$ ,   | $V_O = 2.7\text{ V}$             |                                    |      | 50        | $\mu\text{A}$ |
| $I_{OZL}^\ddagger$ | $V_{CC} = 5.5\text{ V}$ ,   | $V_O = 0.5\text{ V}$             |                                    |      | -50       | $\mu\text{A}$ |
| $I_{off}$          | $V_{CC} = 0$ ,  | $V_I$ or $V_O \leq 5.5\text{ V}$ |                                    |      | $\pm 100$ | $\mu\text{A}$ |
| $I_{CEX}$          | $V_{CC} = 5.5\text{ V}$ ,   | $V_O = 5.5\text{ V}$ ,           | Outputs high                       |      | 50        | $\mu\text{A}$ |
| $I_O^\S$           | $V_{CC} = 5.5\text{ V}$ ,   | $V_O = 2.5\text{ V}$             | -50                                |      | -200      | mA            |
| $I_{CC}$           | $V_{CC} = 5.5\text{ V}$ ,<br>$I_O = 0$ ,<br>$V_I = V_{CC}$ or GND | A or B ports                     | Outputs high                       |      | 5.5       | mA            |
|                    |   |                                  | Outputs low                        |      | 38¶       |               |
|                    |   |                                  | Outputs disabled                   |      | 5         |               |
| $\Delta I_{CC}^\#$ | $V_{CC} = 5.5\text{ V}$ ,   | One input at 3.4 V,              | Other inputs at $V_{CC}$ or GND    |      | 2         | mA            |
| $C_i$              | $V_I = 2.5\text{ V}$ or $0.5\text{ V}$ ,                          |                                  | Control inputs                     |      | 3         | pF            |
| $C_{iO}$           | $V_O = 2.5\text{ V}$ or $0.5\text{ V}$ ,                          |                                  | A or B ports                       |      | 10        | pF            |
| $C_o$              | $V_O = 2.5\text{ V}$ or $0.5\text{ V}$ ,                          |                                  | TDO                                |      | 8         | pF            |

NOTE 4: Preliminary specifications based on SPICE analysis

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ The parameters  $I_{OZH}$  and  $I_{OZL}$  include the input leakage current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ If both A and B ports are low,  $I_{CCL}$  is 76 mA.

# This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

**timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Note 4 and Figure 2)**

|                    |                 |                                    | MIN | MAX | UNIT |
|--------------------|-----------------|------------------------------------|-----|-----|------|
| $f_{\text{clock}}$ | Clock frequency | CLKAB or CLKBA                     |     | 100 | MHz  |
| $t_w$              | Pulse duration  | CLKAB or CLKBA high or low         | 4   |     | ns   |
| $t_{su}$           | Setup time      | A before CLKAB↑ or B before CLKBA↑ | 4.5 |     | ns   |
| $t_h$              | Hold time       | A after CLKAB↑ or B after CLKBA↑   | 0   |     | ns   |

NOTE 4: Preliminary specifications based on SPICE analysis

**SN74ABT18646**  
**SCAN TEST DEVICE**  
**WITH 18-BIT TRANSCEIVER AND REGISTER**

SCBS131A – AUGUST 1992 – REVISED JANUARY 2002

**timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Note 4 and Figure 2)**

|                    |                 |  | MIN | MAX | UNIT |
|--------------------|-----------------|--|-----|-----|------|
| f <sub>clock</sub> | Clock frequency | TCK  |     | 50  | MHz  |
| t <sub>w</sub>     | Pulse duration  | TCK high or low                                    | 8   |     | ns   |
| t <sub>su</sub>    | Setup time      | A, B, CLK, DIR, $\overline{OE}$ , or S before TCK↑ | 4.5 |     | ns   |
|                    |                 | TDI before TCK↑                                    | 7.5 |     |      |
|                    |                 | TMS before TCK↑                                    | 3   |     |      |
| t <sub>h</sub>     | Hold time       | A or B after TCK↑                                  | 0.5 |     | ns   |
|                    |                 | CLK, DIR, $\overline{OE}$ , or S after TCK↑        | 0   |     |      |
|                    |                 | TDI after TCK↑                                     | 0.5 |     |      |
|                    |                 | TMS after TCK↑                                     | 0.5 |     |      |
| t <sub>d</sub>     | Delay time      | Power up to TCK↑                                   | 50  |     | ns   |
| t <sub>r</sub>     | Rise time       | V <sub>CC</sub> power up                           | 1   |     | μs   |

NOTE 4: Preliminary specifications based on SPICE analysis

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Note 4 and Figure 2)**

| PARAMETER        | FROM (INPUT)    | TO (OUTPUT) | MIN | MAX  | UNIT |
|------------------|-----------------|-------------|-----|------|------|
| f <sub>max</sub> | CLKAB or CLKBA  |             | 100 |      | MHz  |
| t <sub>PLH</sub> | A or B          | B or A      | 2   | 5.4  | ns   |
| t <sub>PHL</sub> |                 |             | 2   | 6.6  |      |
| t <sub>PLH</sub> | CLKAB or CLKBA  | B or A      | 2.5 | 8    | ns   |
| t <sub>PHL</sub> |                 |             | 2.5 | 7.4  |      |
| t <sub>PLH</sub> | SAB or SBA      | B or A      | 2   | 7.5  | ns   |
| t <sub>PHL</sub> |                 |             | 2   | 8    |      |
| t <sub>PZH</sub> | DIR             | B or A      | 2   | 8    | ns   |
| t <sub>PZL</sub> |                 |             | 3   | 9.1  |      |
| t <sub>PZH</sub> | $\overline{OE}$ | B or A      | 2.5 | 8.6  | ns   |
| t <sub>PZL</sub> |                 |             | 3   | 9.3  |      |
| t <sub>PHZ</sub> | DIR             | B or A      | 3.5 | 11.1 | ns   |
| t <sub>PLZ</sub> |                 |             | 3   | 8.8  |      |
| t <sub>PHZ</sub> | $\overline{OE}$ | B or A      | 3.5 | 10.5 | ns   |
| t <sub>PLZ</sub> |                 |             | 2   | 8.5  |      |

NOTE 4: Preliminary specifications based on SPICE analysis





**SN74ABT18646**  
**SCAN TEST DEVICE**  
**WITH 18-BIT TRANSCEIVER AND REGISTER**  
SCBS131A – AUGUST 1992 – REVISED JANUARY 2002

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Note 4 and Figure 2)

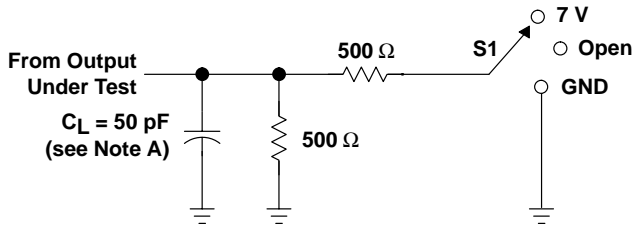
| PARAMETER        | FROM (INPUT) | TO (OUTPUT) | MIN | MAX  | UNIT |
|------------------|--------------|-------------|-----|------|------|
| f <sub>max</sub> | TCK          |             | 50  |      | MHz  |
| t <sub>PLH</sub> | TCK↓         | A or B      | 2.5 | 13.5 | ns   |
| t <sub>PHL</sub> |              |             | 2.5 | 12.5 |      |
| t <sub>PLH</sub> | TCK↓         | TDO         | 2   | 6.5  | ns   |
| t <sub>PHL</sub> |              |             | 2   | 6.5  |      |
| t <sub>PZH</sub> | TCK↓         | A or B      | 4.5 | 13.8 | ns   |
| t <sub>PZL</sub> |              |             | 5   | 14.5 |      |
| t <sub>PZH</sub> | TCK↓         | TDO         | 2   | 7    | ns   |
| t <sub>PZL</sub> |              |             | 3   | 7.5  |      |
| t <sub>PHZ</sub> | TCK↓         | A or B      | 4   | 17   | ns   |
| t <sub>PLZ</sub> |              |             | 3   | 16   |      |
| t <sub>PHZ</sub> | TCK↓         | TDO         | 3   | 9    | ns   |
| t <sub>PLZ</sub> |              |             | 3   | 7.5  |      |

NOTE 4: Preliminary specifications based on SPICE analysis

**SN74ABT18646**  
**SCAN TEST DEVICE**  
**WITH 18-BIT TRANSCEIVER AND REGISTER**

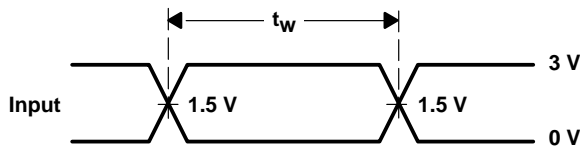
SCBS131A – AUGUST 1992 – REVISED JANUARY 2002

**PARAMETER MEASUREMENT INFORMATION**

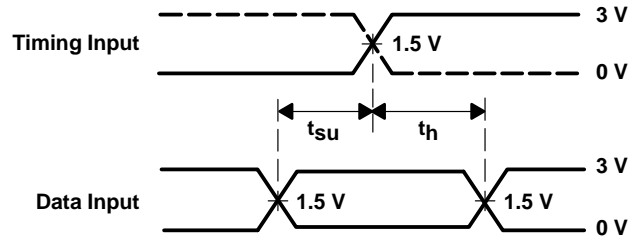


**LOAD CIRCUIT**

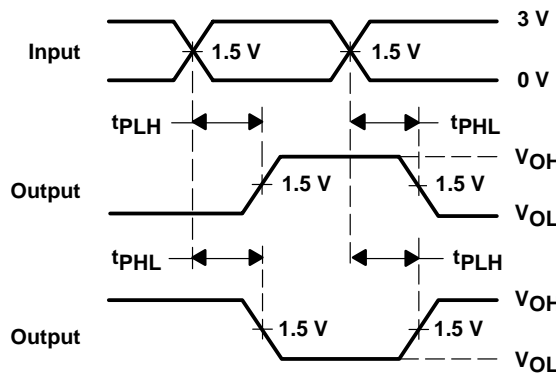
| TEST              | S1   |
|-------------------|------|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V  |
| $t_{PHZ}/t_{PZH}$ | Open |



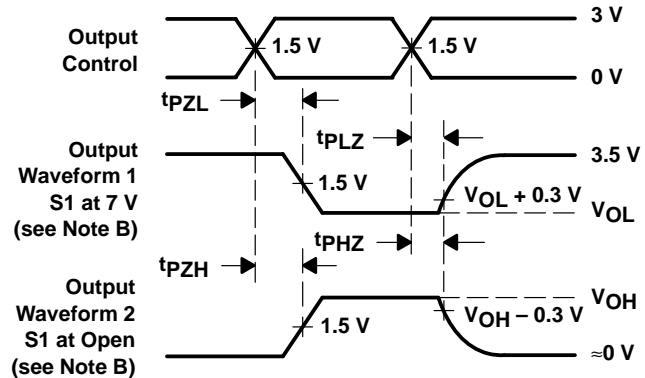
**VOLTAGE WAVEFORMS  
 PULSE DURATION**



**VOLTAGE WAVEFORMS  
 SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS  
 PROPAGATION DELAY TIMES  
 INVERTING AND NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS  
 ENABLE AND DISABLE TIMES  
 LOW- AND HIGH-LEVEL ENABLING**

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.

**Figure 2. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| SN74ABT18646PM   | ACTIVE                | LQFP         | PM              | 64   | 160         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR          |
| SN74ABT18646PMG4 | ACTIVE                | LQFP         | PM              | 64   | 160         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR          |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74ABT18646 :**

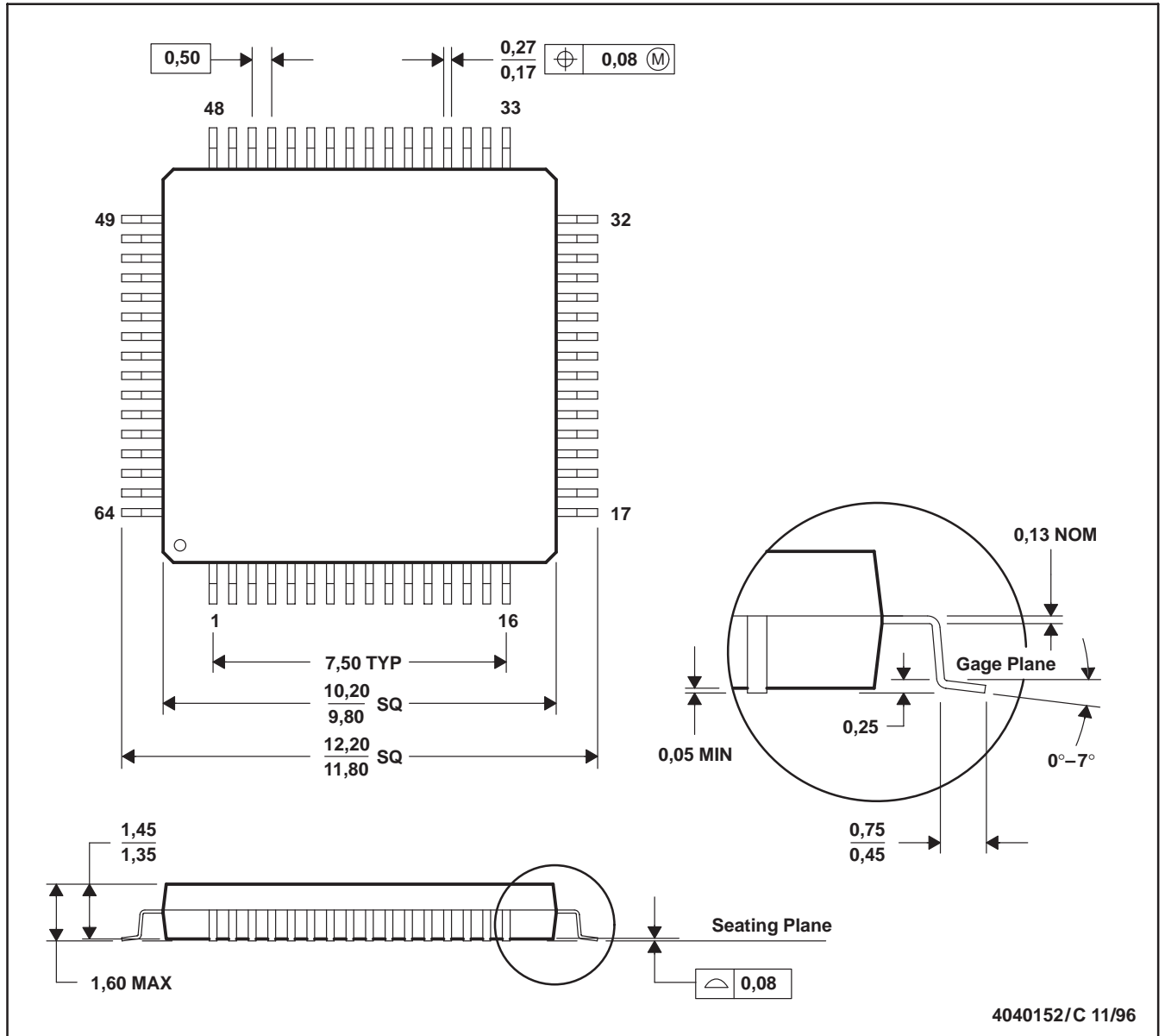
- Military: [SN54ABT18646](#)

NOTE: Qualified Version Definitions:

- Military - QML certified for Military and Defense Applications

PM (S-PQFP-G64)

PLASTIC QUAD FLATPACK



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-026  
 D. May also be thermally enhanced plastic with leads connected to the die pads.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

### Products

|                             |  |
|-----------------------------|--|
| Amplifiers                  | <a href="http://amplifier.ti.com">amplifier.ti.com</a>             |
| Data Converters             | <a href="http://dataconverter.ti.com">dataconverter.ti.com</a>     |
| DSP                         | <a href="http://dsp.ti.com">dsp.ti.com</a>                         |
| Clocks and Timers           | <a href="http://www.ti.com/clocks">www.ti.com/clocks</a>           |
| Interface                   | <a href="http://interface.ti.com">interface.ti.com</a>             |
| Logic                       | <a href="http://logic.ti.com">logic.ti.com</a>                     |
| Power Mgmt                  | <a href="http://power.ti.com">power.ti.com</a>                     |
| Microcontrollers            | <a href="http://microcontroller.ti.com">microcontroller.ti.com</a> |
| RFID                        | <a href="http://www.ti-rfid.com">www.ti-rfid.com</a>               |
| RF/IF and ZigBee® Solutions | <a href="http://www.ti.com/lprf">www.ti.com/lprf</a>               |

### Applications

|                    |  |
|--------------------|--|
| Audio              | <a href="http://www.ti.com/audio">www.ti.com/audio</a>                   |
| Automotive         | <a href="http://www.ti.com/automotive">www.ti.com/automotive</a>         |
| Broadband          | <a href="http://www.ti.com/broadband">www.ti.com/broadband</a>           |
| Digital Control    | <a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a> |
| Medical            | <a href="http://www.ti.com/medical">www.ti.com/medical</a>               |
| Military           | <a href="http://www.ti.com/military">www.ti.com/military</a>             |
| Optical Networking | <a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a> |
| Security           | <a href="http://www.ti.com/security">www.ti.com/security</a>             |
| Telephony          | <a href="http://www.ti.com/telephony">www.ti.com/telephony</a>           |
| Video & Imaging    | <a href="http://www.ti.com/video">www.ti.com/video</a>                   |
| Wireless           | <a href="http://www.ti.com/wireless">www.ti.com/wireless</a>             |

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2008, Texas Instruments Incorporated