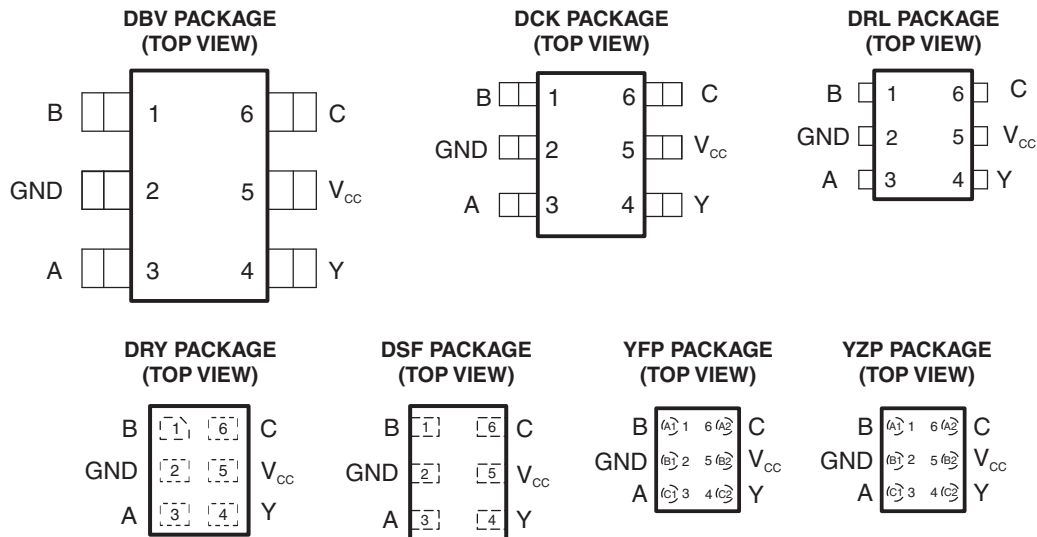


LOW-POWER CONFIGURABLE MULTIPLE-FUNCTION GATE

Check for Samples: [SN74AUP1G97](#)

FEATURES

- Available in the Texas Instruments NanoStar™ Package
- Low Static-Power Consumption ($I_{CC} = 0.9 \mu\text{A Max}$)
- Low Dynamic-Power Consumption ($C_{pd} = 4.8 \text{ pF Typ at } 3.3 \text{ V}$)
- Low Input Capacitance ($C_i = 1.5 \text{ pF Typ}$)
- Low Noise – Overshoot and Undershoot <math><10\%</math> of V_{CC}
- I_{off} Supports Partial-Power-Down Mode Operation
- Includes Schmitt-Trigger Inputs
- Wide Operating V_{CC} Range of 0.8 V to 3.6 V
- Optimized for 3.3-V Operation
- 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- $t_{pd} = 5.6 \text{ ns Max at } 3.3 \text{ V}$
- Suitable for Point-to-Point Applications
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)



See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family ensures a very low static- and dynamic-power consumption across the entire V_{CC} range of 0.8 V to 3.6 V, resulting in increased battery life (see [Figure 1](#)). This product also maintains excellent signal integrity (see the very low undershoot and overshoot characteristics shown in [Figure 2](#)).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

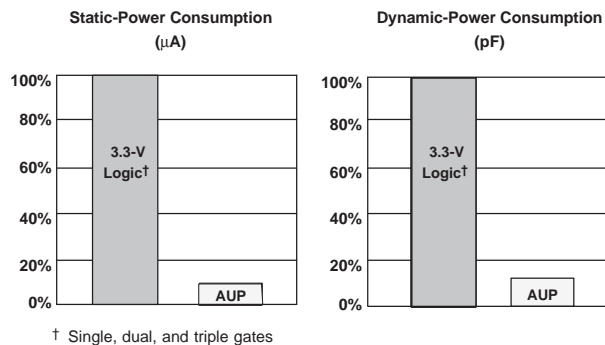


Figure 1. AUP – The Lowest-Power Family

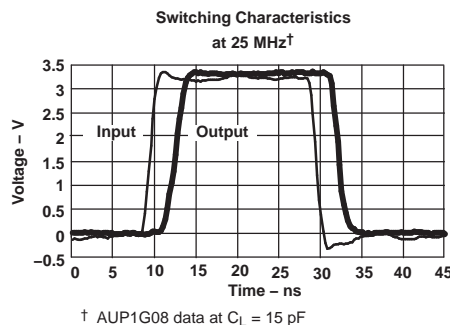


Figure 2. Excellent Signal Integrity

The SN74AUP1G97 features configurable multiple functions. The output state is determined by eight patterns of 3-bit input. The user can choose the logic functions MUX, AND, OR, NAND, NOR, inverter, and noninverter. All inputs can be connected to V_{CC} or GND.

The device functions as an independent gate with Schmitt-trigger inputs, which allows for slow input transition and better switching-noise immunity at the input.

NanoStar™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION⁽¹⁾

T _A	PACKAGE ⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING ⁽³⁾
-40°C to 85°C	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YFP (Pb-free)	Reel of 3000	SN74AUP1G97YFPR	__ _HP_
	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Reel of 3000	SN74AUP1G97YZPR	__ _HP_
	QFN – DRY	Reel of 5000	SN74AUP1G97DRYR	HP
	uQFN – DSF	Reel of 5000	SN74AUP1G97DSFR	HP
	SOT (SOT-23) – DBV	Reel of 3000	SN74AUP1G97DBVR	H97_
	SOT (SC-70) – DCK	Reel of 3000	SN74AUP1G97DCKR	HP_
	SOT (SOT-553) – DRL	Reel of 4000	SN74AUP1G97DRLR	

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

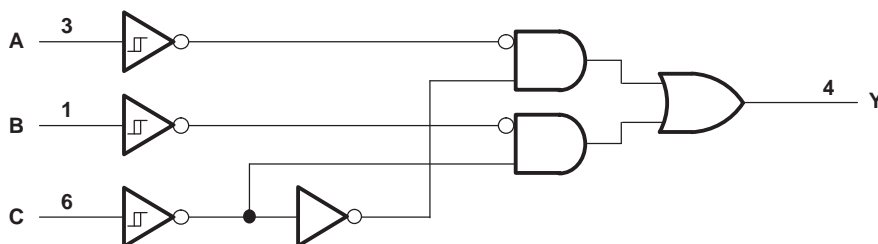
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

(3) DBV/DCK/DRL: The actual top-side marking has one additional character that designates the wafer fab/assembly site.
YFP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the wafer fab/assembly site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, ● = Pb-free).

FUNCTION TABLE

INPUTS			OUTPUT Y
C	B	A	
L	L	L	L
L	L	H	L
L	H	L	H
L	H	H	H
H	L	L	L
H	L	H	H
H	H	L	L
H	H	H	H

LOGIC DIAGRAM (POSITIVE LOGIC)



FUNCTION SELECTION TABLE

LOGIC FUNCTION	FIGURE NO.
2-to-1 data selector	3
2-input AND gate	4
2-input OR gate with one inverted input	5
2-input NAND gate with one inverted input	5
2-input AND gate with one inverted input	6
2-input NOR gate with one inverted input	6
2-input OR gate	7
Inverter	8
Noninverted buffer	9

LOGIC CONFIGURATIONS

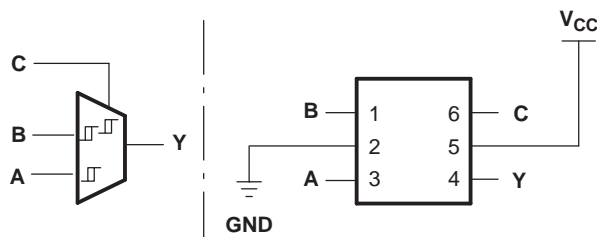


Figure 3. 2-to-1 Data Selector
When C is L, Y = B; When C is H, Y = A

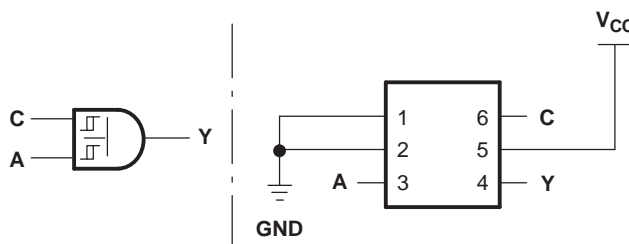


Figure 4. 2-Input AND Gate

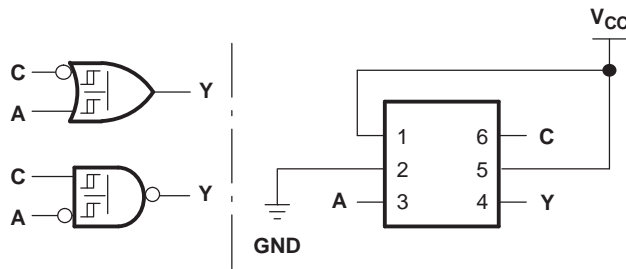


Figure 5. Input OR Gate With One Inverted Input
2-Input NAND Gate With One Inverted Input

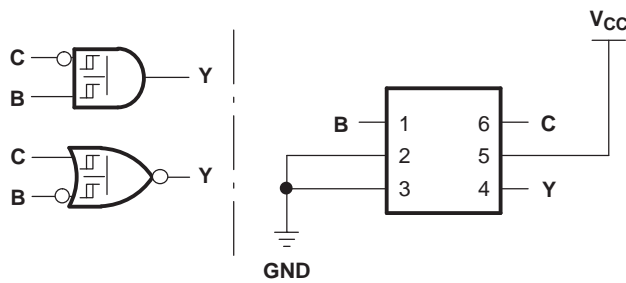


Figure 6. 2-Input AND Gate With One Inverted Input
2-Input NOR Gate With One Inverted Input

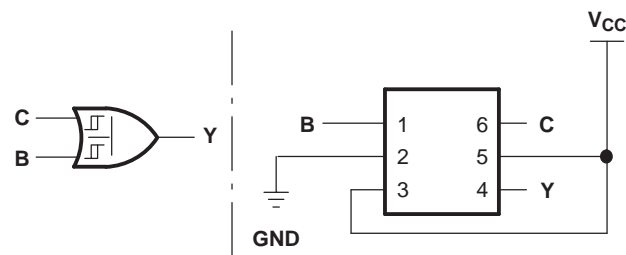


Figure 7. 2-Input OR Gate

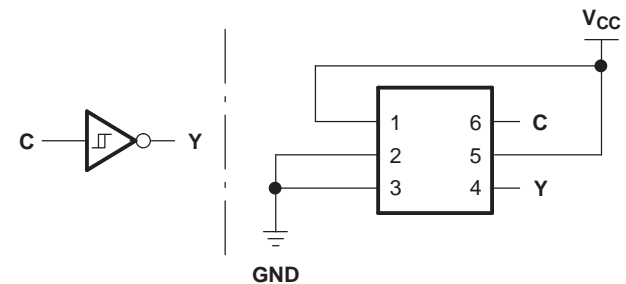


Figure 8. Inverter

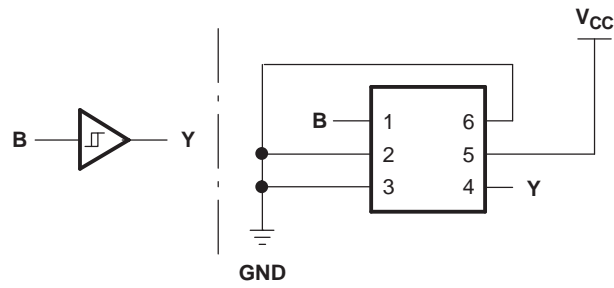


Figure 9. Noninverted Buffer

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	-0.5	4.6	V
V_I	Input voltage range ⁽²⁾	-0.5	4.6	V
V_O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	-0.5	4.6	V
V_O	Output voltage range in the high or low state ⁽²⁾	-0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$	-50	mA
I_{OK}	Output clamp current	$V_O < 0$	-50	mA
I_O	Continuous output current		± 20	mA
	Continuous current through V_{CC} or GND		± 50	mA
θ_{JA}	Package thermal impedance ⁽³⁾	DBV package	165	°C/W
		DCK package	259	
		DRL package	142	
		DSF package	300	
		DRY package	234	
		YFP package	123	
		YZP package	123	
T_{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage	0.8	3.6	V
V_I	Input voltage	0	3.6	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 0.8$ V	-20	μ A
		$V_{CC} = 1.1$ V	-1.1	mA
		$V_{CC} = 1.4$ V	-1.7	
		$V_{CC} = 1.65$	-1.9	
		$V_{CC} = 2.3$ V	-3.1	
		$V_{CC} = 3$ V	-4	
I_{OL}	Low-level output current	$V_{CC} = 0.8$ V	20	μ A
		$V_{CC} = 1.1$ V	1.1	mA
		$V_{CC} = 1.4$ V	1.7	
		$V_{CC} = 1.65$ V	1.9	
		$V_{CC} = 2.3$ V	3.1	
		$V_{CC} = 3$ V	4	
T_A	Operating free-air temperature	-40	85	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			T _A = –40°C to 85°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
V _{T+} Positive-going input threshold voltage		0.8 V	0.3		0.6	0.3	0.6	V
		1.1 V	0.53		0.9	0.53	0.9	
		1.4 V	0.74		1.11	0.74	1.11	
		1.65 V	0.91		1.29	0.91	1.29	
		2.3 V	1.37		1.77	1.37	1.77	
		3 V	1.88		2.29	1.88	2.29	
V _{T–} Negative-going input threshold voltage		0.8 V	0.1		0.6	0.1	0.6	V
		1.1 V	0.26		0.65	0.26	0.65	
		1.4 V	0.39		0.75	0.39	0.75	
		1.65 V	0.47		0.84	0.47	0.84	
		2.3 V	0.69		1.04	0.69	1.04	
		3 V	0.88		1.24	0.88	1.24	
ΔV _T Hysteresis (V _{T+} – V _{T–})		0.8 V	0.07		0.5	0.07	0.5	V
		1.1 V	0.08		0.46	0.08	0.46	
		1.4 V	0.18		0.56	0.18	0.56	
		1.65 V	0.27		0.66	0.27	0.66	
		2.3 V	0.53		0.92	0.53	0.92	
		3 V	0.79		1.31	0.79	1.31	
V _{OH}	I _{OH} = –20 μA	0.8 V to 3.6 V	V _{CC} – 0.1		V _{CC} – 0.1		V	
	I _{OH} = –1.1 mA	1.1 V	0.75 × V _{CC}		0.7 × V _{CC}			
	I _{OH} = –1.7 mA	1.4 V	1.11		1.03			
	I _{OH} = –1.9 mA	1.65 V	1.32		1.3			
	I _{OH} = –2.3 mA	2.3 V	2.05		1.97			
	I _{OH} = –3.1 mA		1.9		1.85			
	I _{OH} = –2.7 mA	3 V	2.72		2.67			
	I _{OH} = –4 mA		2.6		2.55			
V _{OL}	I _{OL} = 20 μA	0.8 V to 3.6 V	0.1		0.1		V	
	I _{OL} = 1.1 mA	1.1 V	0.3 × V _{CC}		0.3 × V _{CC}			
	I _{OL} = 1.7 mA	1.4 V	0.31		0.37			
	I _{OL} = 1.9 mA	1.65 V	0.31		0.35			
	I _{OL} = 2.3 mA	2.3 V	0.31		0.33			
	I _{OL} = 3.1 mA		0.44		0.45			
	I _{OL} = 2.7 mA	3 V	0.31		0.33			
	I _{OL} = 4 mA		0.44		0.45			
I _I	All inputs	V _I = GND to 3.6 V	0 V to 3.6 V		0.1	0.5	μA	
I _{off}		V _I or V _O = 0 V to 3.6 V	0 V		0.2	0.6	μA	
ΔI _{off}		V _I or V _O = 0 V to 3.6 V	0 V to 0.2 V		0.2	0.6	μA	
I _{CC}		V _I = GND or (V _{CC} to 3.6 V), I _O = 0	0.8 V to 3.6 V		0.5	0.9	μA	
ΔI _{CC}		V _I = V _{CC} – 0.6 V ⁽¹⁾ , I _O = 0	3.3 V		40	50	μA	
C _i	V _I = V _{CC} or GND	0 V	1.5				pF	
		3.6 V	1.5					
C _O	V _O = GND	0 V	3				pF	

 (1) One input at V_{CC} – 0.6 V, other inputs at V_{CC} or GND.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $C_L = 5$ pF (unless otherwise noted) (see [Figure 10](#) and [Figure 11](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C to } 85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A, B, or C	Y	0.8 V	23.1					ns
			$1.2\text{ V} \pm 0.1\text{ V}$	3.1	9.1	13.9	2.6	17.6	
			$1.5\text{ V} \pm 0.1\text{ V}$	2.1	6.4	9.4	1.6	11.4	
			$1.8\text{ V} \pm 0.15\text{ V}$	1.6	5.1	7.5	1.1	9.2	
			$2.5\text{ V} \pm 0.2\text{ V}$	1.1	3.6	5.7	0.6	6.8	
			$3.3\text{ V} \pm 0.3\text{ V}$	1	2.8	4.7	0.5	5.6	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $C_L = 10$ pF (unless otherwise noted) (see [Figure 10](#) and [Figure 11](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C to } 85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A, B, or C	Y	0.8 V	26.2					ns
			$1.2\text{ V} \pm 0.1\text{ V}$	5.2	10.4	15.4	4.7	19.2	
			$1.5\text{ V} \pm 0.1\text{ V}$	4	7.4	10.7	3.5	12.7	
			$1.8\text{ V} \pm 0.15\text{ V}$	3.1	6	8.6	2.6	10.5	
			$2.5\text{ V} \pm 0.2\text{ V}$	2.7	4.3	6.5	2.2	7.8	
			$3.3\text{ V} \pm 0.3\text{ V}$	2.5	3.4	5.4	2	6.4	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $C_L = 15$ pF (unless otherwise noted) (see [Figure 10](#) and [Figure 11](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C to } 85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A, B, or C	Y	0.8 V	28.9					ns
			$1.2\text{ V} \pm 0.1\text{ V}$	4.1	11.5	16.8	3.6	21.3	
			$1.5\text{ V} \pm 0.1\text{ V}$	3	8.3	11.8	2.5	14.1	
			$1.8\text{ V} \pm 0.15\text{ V}$	2.3	6.7	9.5	1.8	11.6	
			$2.5\text{ V} \pm 0.2\text{ V}$	1.7	4.8	7.2	1.2	8.6	
			$3.3\text{ V} \pm 0.3\text{ V}$	1.4	3.9	6	0.9	7.1	

SWITCHING CHARACTERISTICS

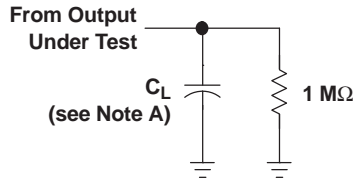
over recommended operating free-air temperature range, $C_L = 30$ pF (unless otherwise noted) (see [Figure 10](#) and [Figure 11](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C to } 85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A, B, or C	Y	0.8 V	36.7					ns
			$1.2\text{ V} \pm 0.1\text{ V}$	5.5	14.6	21.4	5	26.7	
			$1.5\text{ V} \pm 0.1\text{ V}$	4.1	10.5	14.8	3.6	17.7	
			$1.8\text{ V} \pm 0.15\text{ V}$	3.3	8.6	11.8	2.8	14.5	
			$2.5\text{ V} \pm 0.2\text{ V}$	2.5	6.3	8.8	2	10.6	
			$3.3\text{ V} \pm 0.3\text{ V}$	2.1	5.1	7.3	1.6	8.8	

OPERATING CHARACTERISTICS
 $T_A = 25^\circ\text{C}$

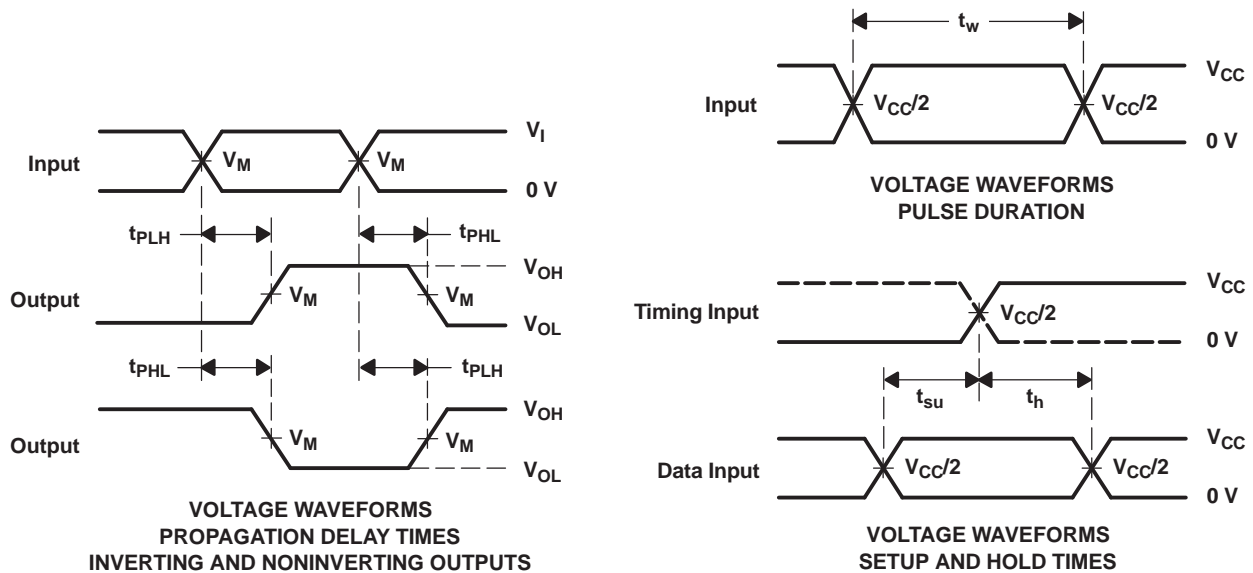
PARAMETER		TEST CONDITIONS	V _{CC}	TYP	UNIT
C _{pd}	Power dissipation capacitance	f = 10 MHz	0.8 V	4	pF
			1.2 V ± 0.1 V	4	
			1.5 V ± 0.1 V	4	
			1.8 V ± 0.15 V	4	
			2.5 V ± 0.2 V	4.4	
			3.3 V ± 0.3 V	4.8	

PARAMETER MEASUREMENT INFORMATION
(Propagation Delays, Setup and Hold Times, and Pulse Duration)



LOAD CIRCUIT

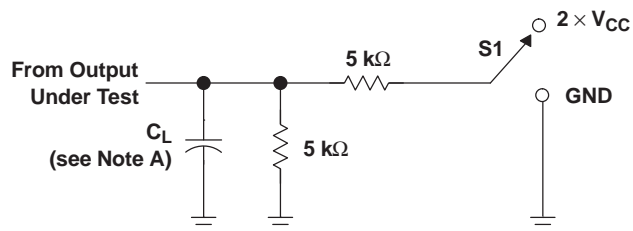
	$V_{CC} = 0.8\text{ V}$	$V_{CC} = 1.2\text{ V}$ $\pm 0.1\text{ V}$	$V_{CC} = 1.5\text{ V}$ $\pm 0.1\text{ V}$	$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}



- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O = 50\ \Omega$, slew rate ≥ 1 V/ns.
 C. The outputs are measured one at a time, with one transition per measurement.
 D. t_{PLH} and t_{PHL} are the same as t_{pd} .
 E. All parameters and waveforms are not applicable to all devices.

Figure 10. Load Circuit and Voltage Waveforms

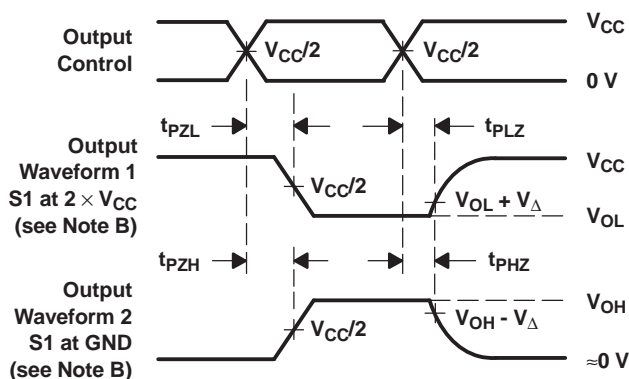
PARAMETER MEASUREMENT INFORMATION
(Enable and Disable Times)



TEST	S1
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PHL}	GND

LOAD CIRCUIT

	$V_{CC} = 0.8 \text{ V}$	$V_{CC} = 1.2 \text{ V} \pm 0.1 \text{ V}$	$V_{CC} = 1.5 \text{ V} \pm 0.1 \text{ V}$	$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$	$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
V_{Δ}	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, slew rate $\geq 1 \text{ V/ns}$.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. All parameters and waveforms are not applicable to all devices.

Figure 11. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN74AUP1G97DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(H97F, H97R)	Samples
SN74AUP1G97DBVRE4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(H97F, H97R)	Samples
SN74AUP1G97DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(H97F, H97R)	Samples
SN74AUP1G97DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	H97R	Samples
SN74AUP1G97DBVTE4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	H97R	Samples
SN74AUP1G97DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	H97R	Samples
SN74AUP1G97DCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HP5, HPF, HPR)	Samples
SN74AUP1G97DCKRE4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HP5, HPF, HPR)	Samples
SN74AUP1G97DCKRG4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HP5, HPF, HPR)	Samples
SN74AUP1G97DCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HP5, HPR)	Samples
SN74AUP1G97DCKTE4	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HP5, HPR)	Samples
SN74AUP1G97DCKTG4	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HP5, HPR)	Samples
SN74AUP1G97DRLR	ACTIVE	SOT	DRL	6	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HP7, HPR)	Samples
SN74AUP1G97DRLRG4	ACTIVE	SOT	DRL	6	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HP7, HPR)	Samples
SN74AUP1G97DRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HP	Samples
SN74AUP1G97DSFR	ACTIVE	SON	DSF	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HP	Samples
SN74AUP1G97YFPR	ACTIVE	DSBGA	YFP	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		(HP2, HP7, HPN)	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN74AUP1G97YZPR	ACTIVE	DSBGA	YZP	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(HP2, HP7, HPN)	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP1G97DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1G97DBVT	SOT-23	DBV	6	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1G97DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74AUP1G97DCKR	SC70	DCK	6	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AUP1G97DCKT	SC70	DCK	6	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AUP1G97DRLR	SOT	DRL	6	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74AUP1G97DRLR	SOT	DRL	6	4000	180.0	9.5	1.78	1.78	0.69	4.0	8.0	Q3
SN74AUP1G97DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74AUP1G97DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74AUP1G97YFPR	DSBGA	YFP	6	3000	178.0	9.2	0.89	1.29	0.62	4.0	8.0	Q1
SN74AUP1G97YZPR	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

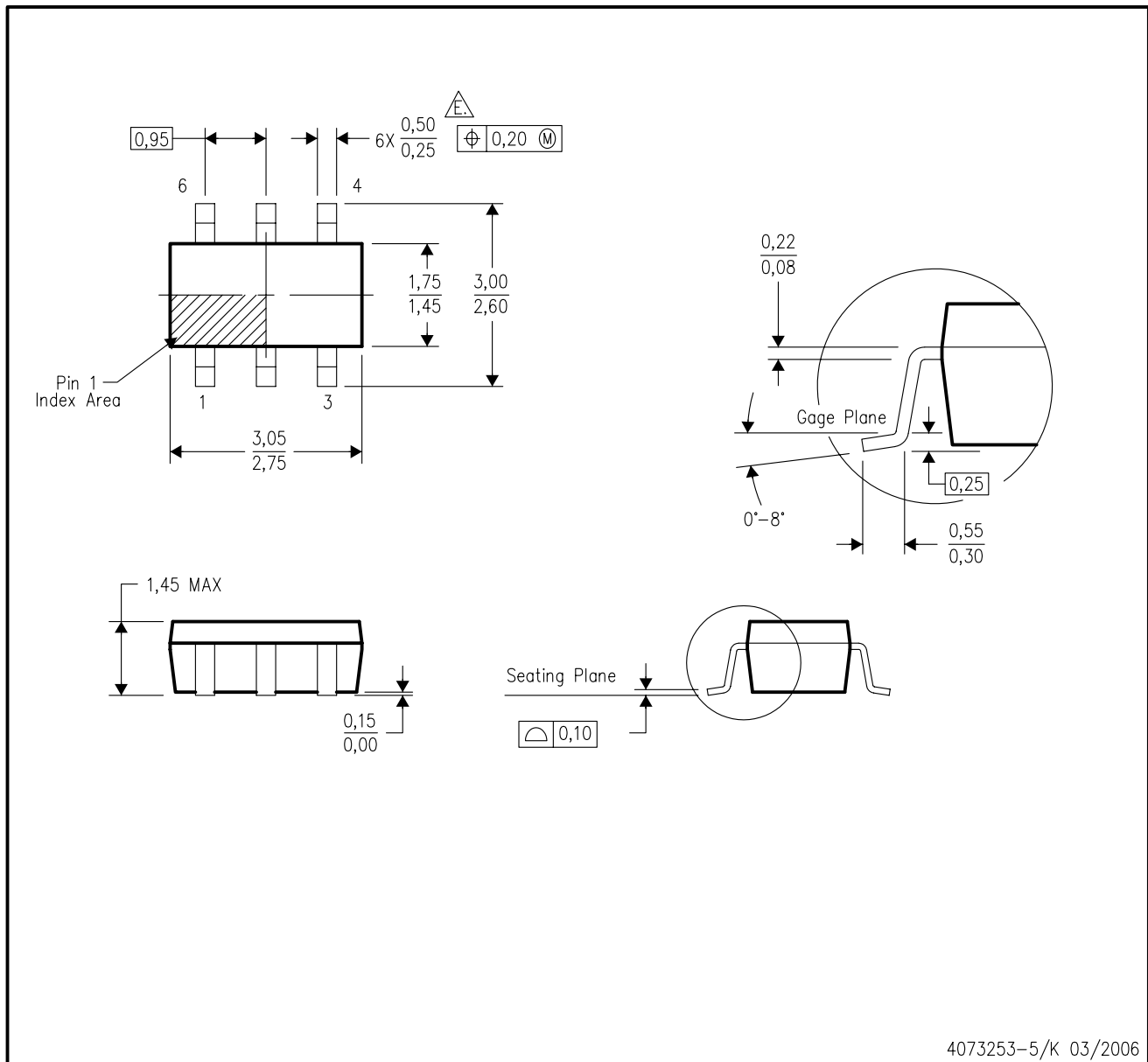
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP1G97DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
SN74AUP1G97DBVT	SOT-23	DBV	6	250	202.0	201.0	28.0
SN74AUP1G97DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
SN74AUP1G97DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
SN74AUP1G97DCKT	SC70	DCK	6	250	180.0	180.0	18.0
SN74AUP1G97DRLR	SOT	DRL	6	4000	202.0	201.0	28.0
SN74AUP1G97DRLR	SOT	DRL	6	4000	180.0	180.0	30.0
SN74AUP1G97DRYR	SON	DRY	6	5000	180.0	180.0	30.0
SN74AUP1G97DSFR	SON	DSF	6	5000	180.0	180.0	30.0
SN74AUP1G97YFPR	DSBGA	YFP	6	3000	220.0	220.0	35.0
SN74AUP1G97YZPR	DSBGA	YZP	6	3000	220.0	220.0	35.0

DBV (R-PDSO-G6)

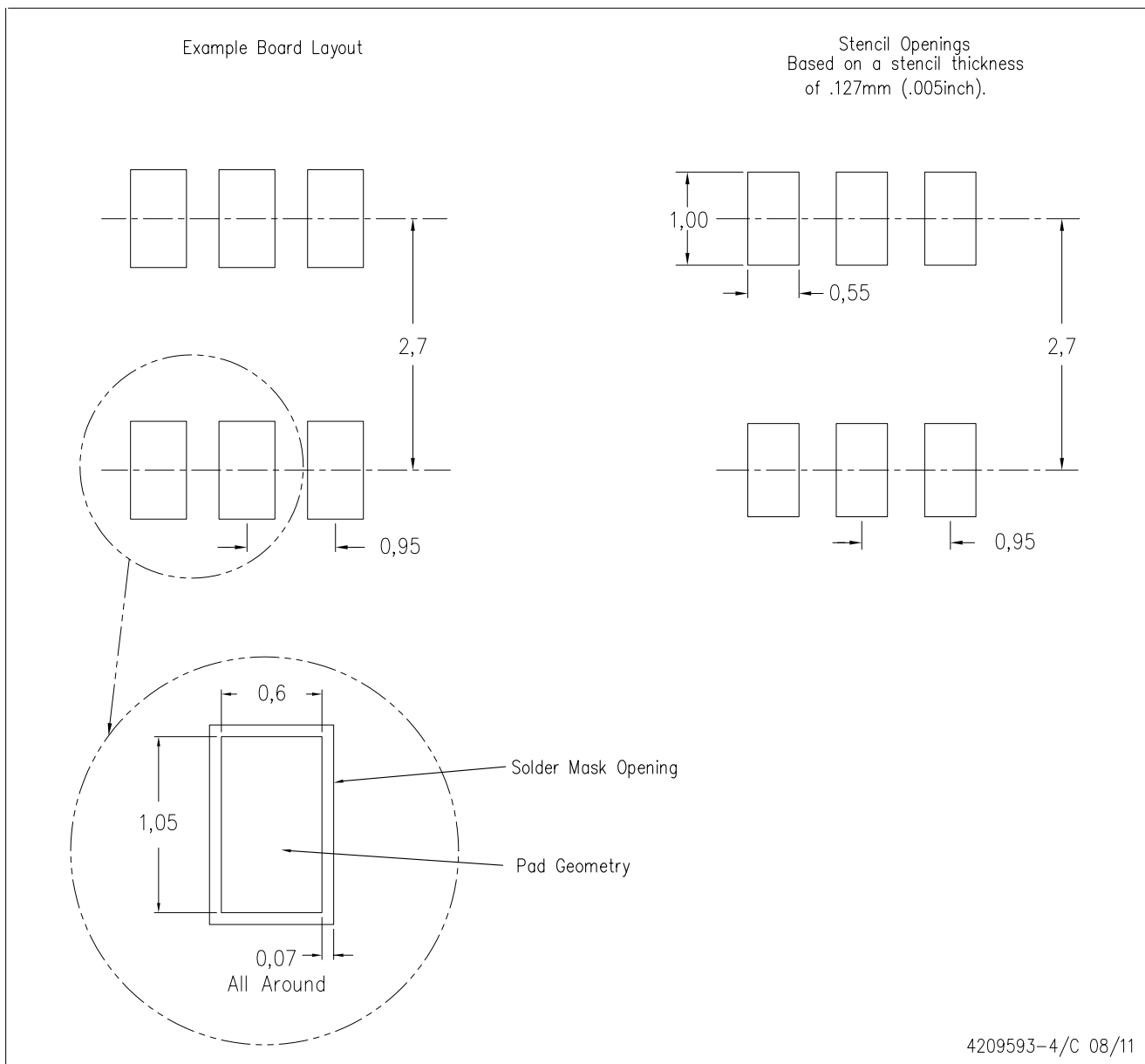
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- \triangle Falls within JEDEC MO-178 Variation AB, except minimum lead width.

DBV (R-PDSO-G6)

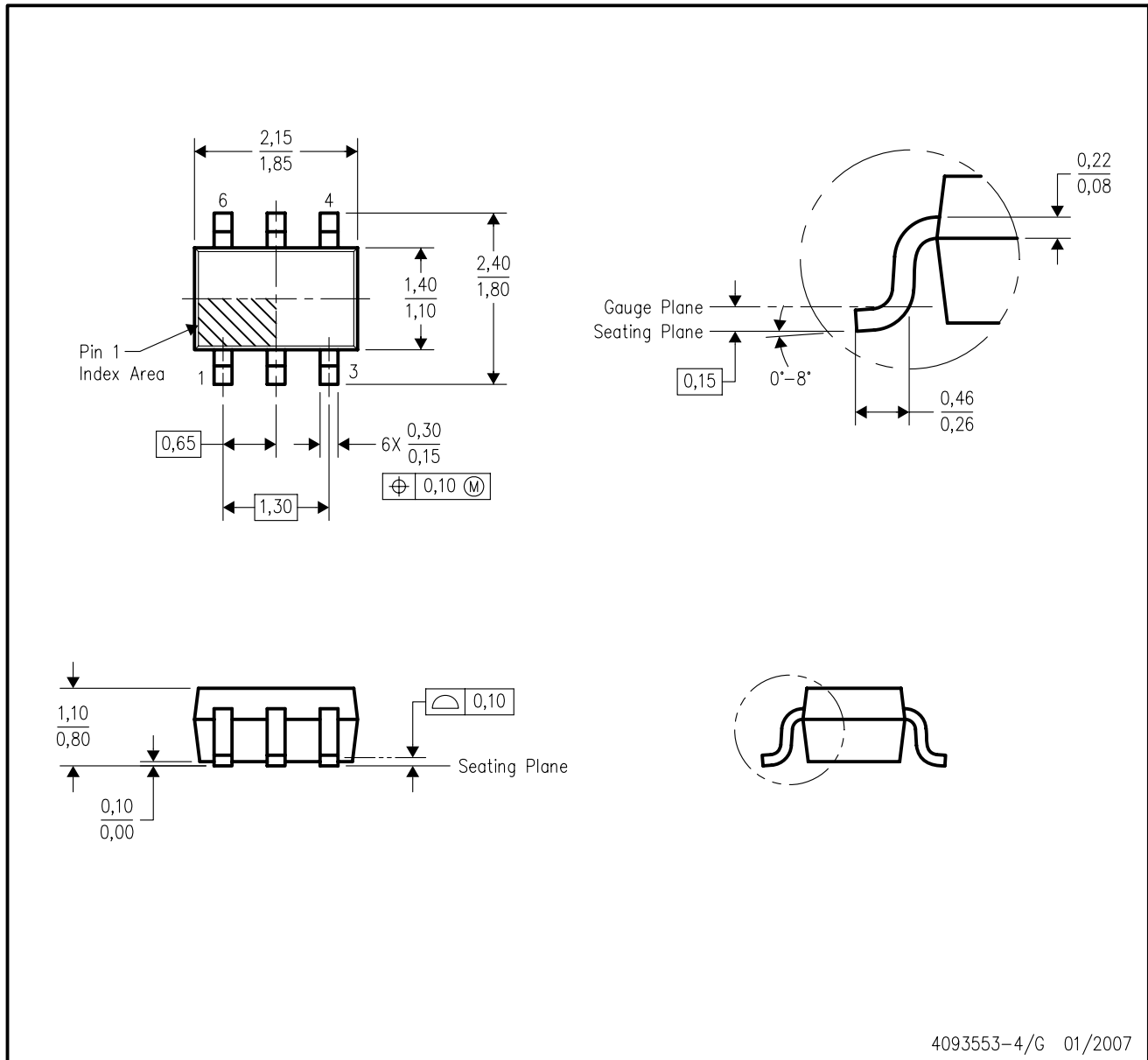
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DCK (R-PDSO-G6)

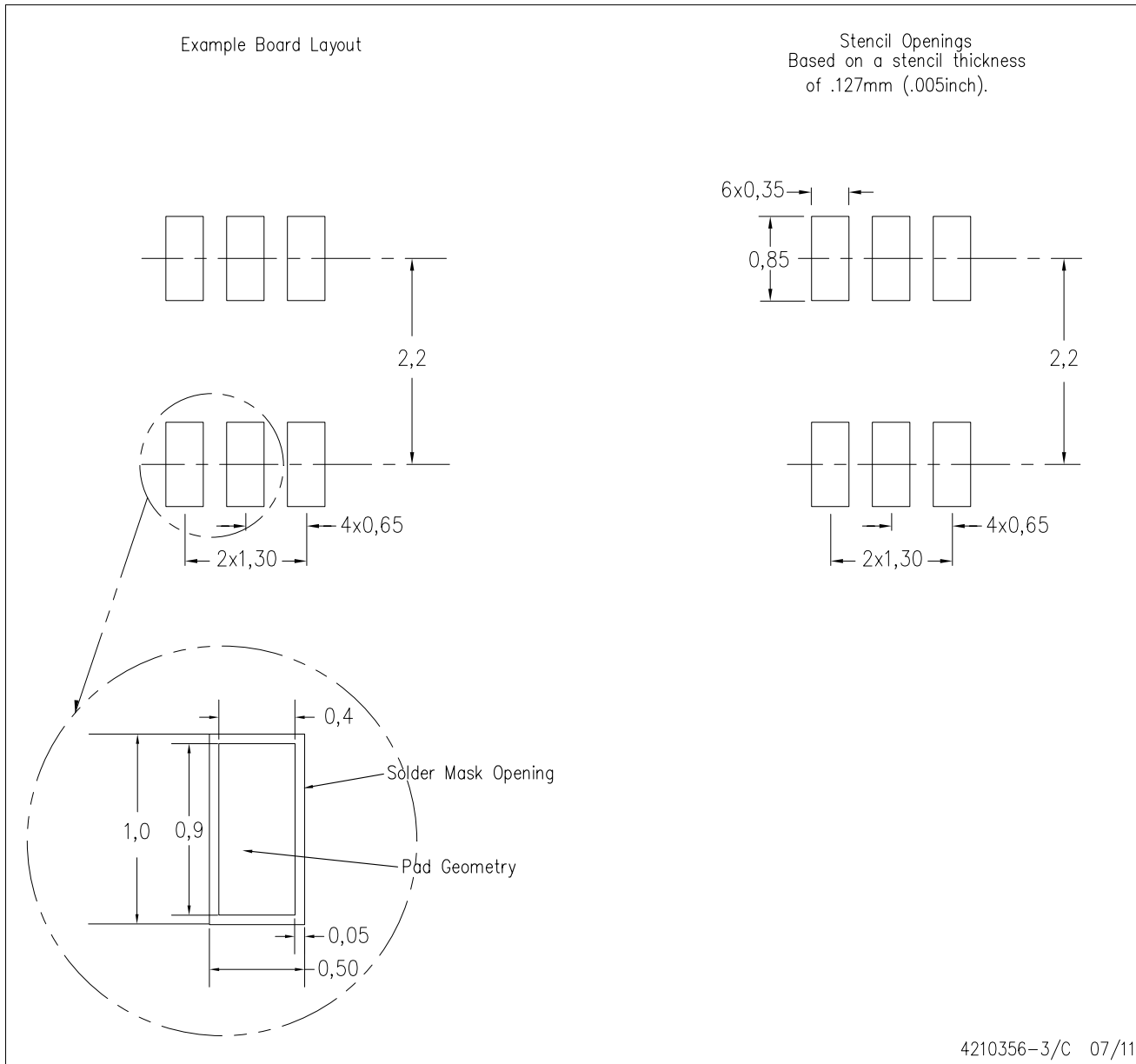
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-203 variation AB.

DCK (R-PDSO-G6)

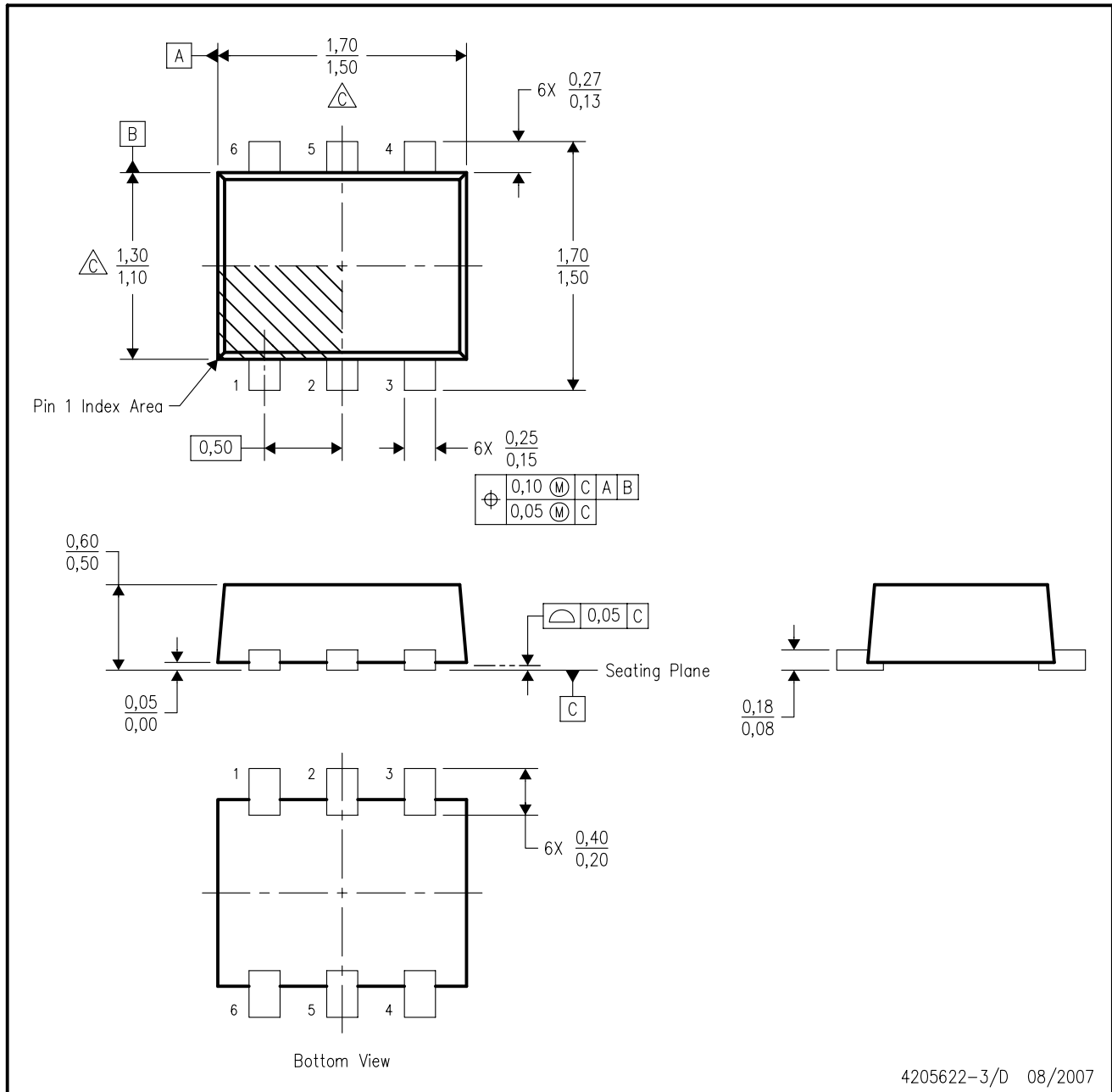
PLASTIC SMALL OUTLINE



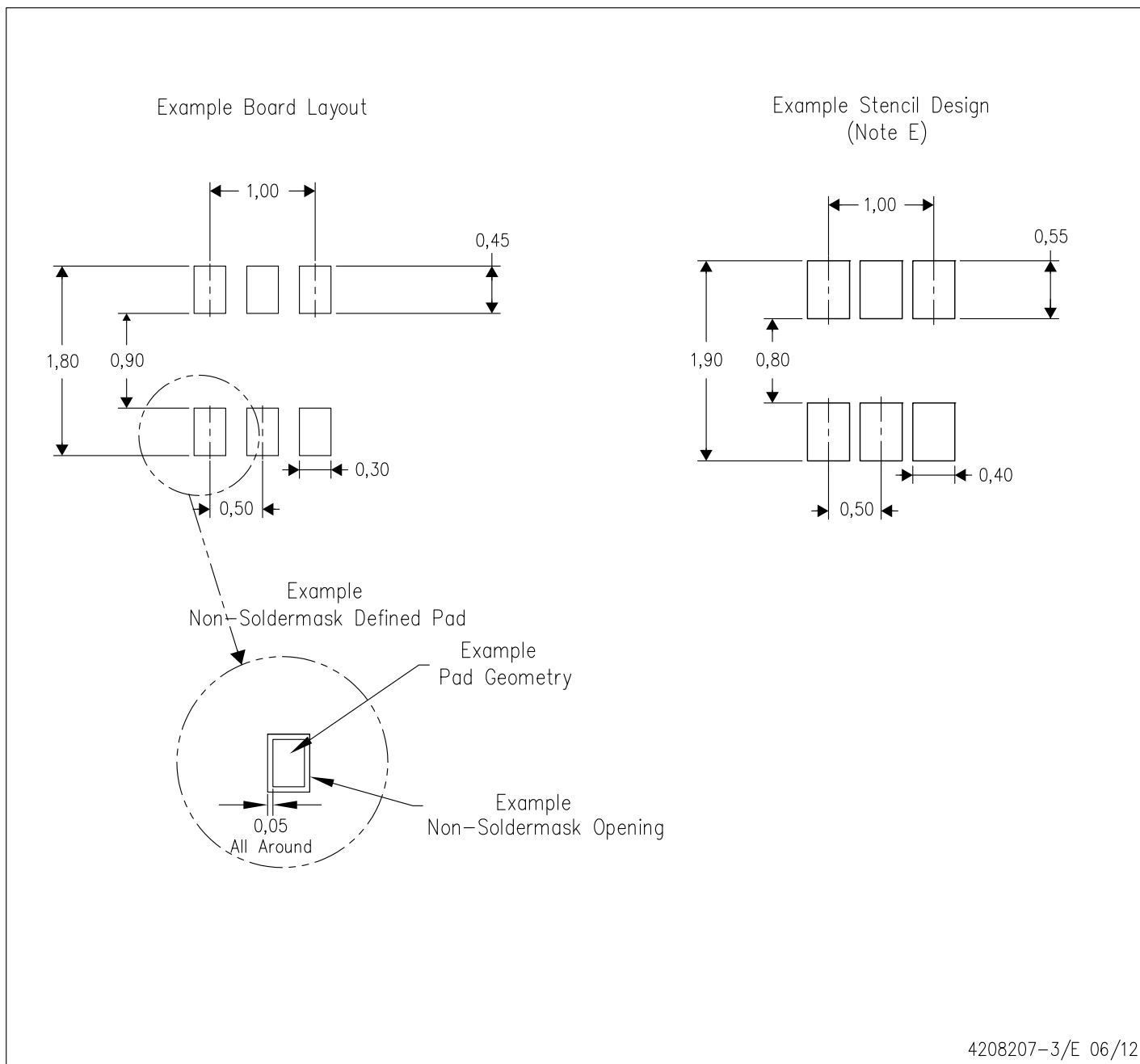
- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DRL (R-PDSO-N6)

PLASTIC SMALL OUTLINE



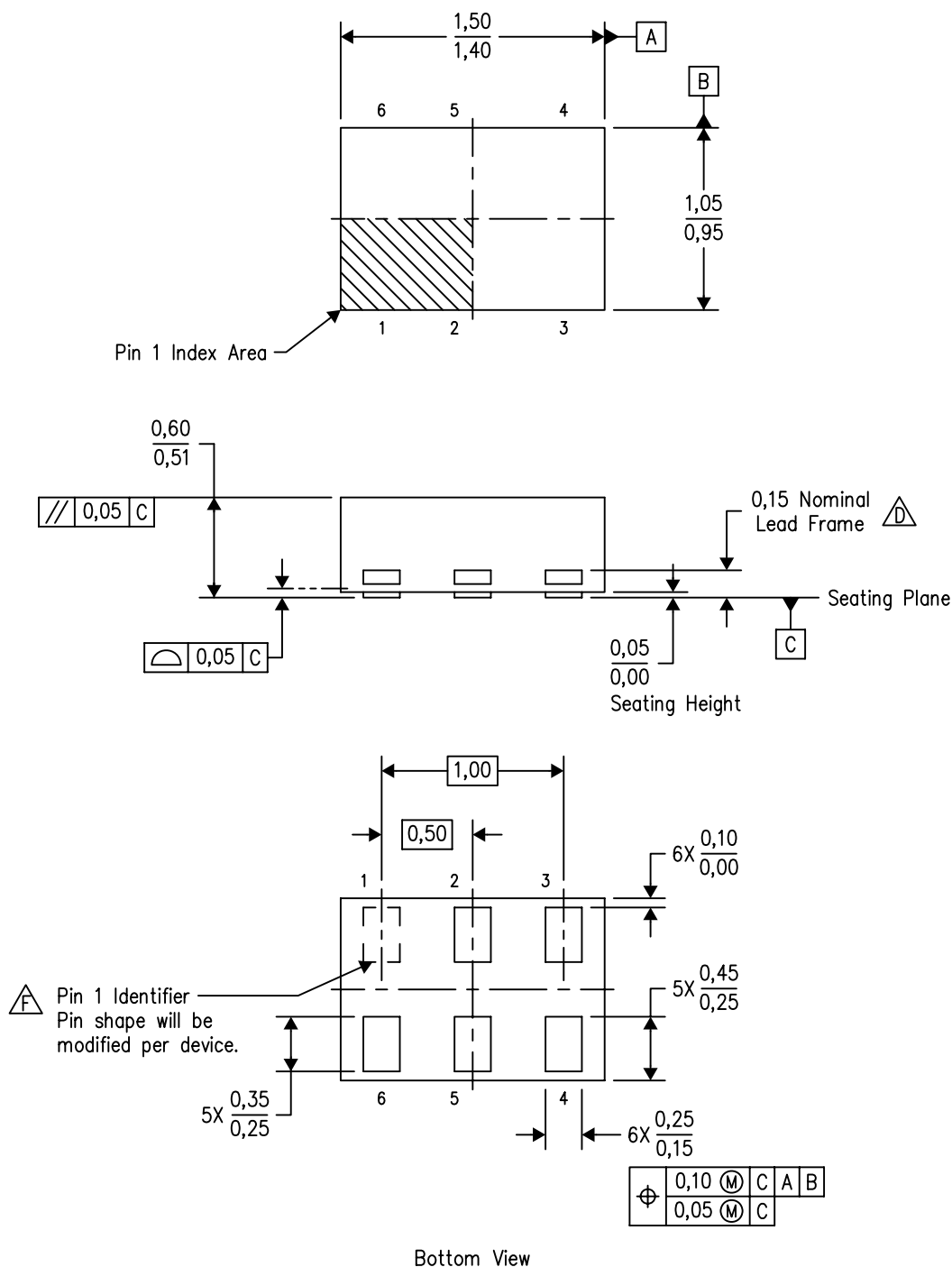
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
 - D. JEDEC package registration is pending.



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
 - Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

DRY (R-PUSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD

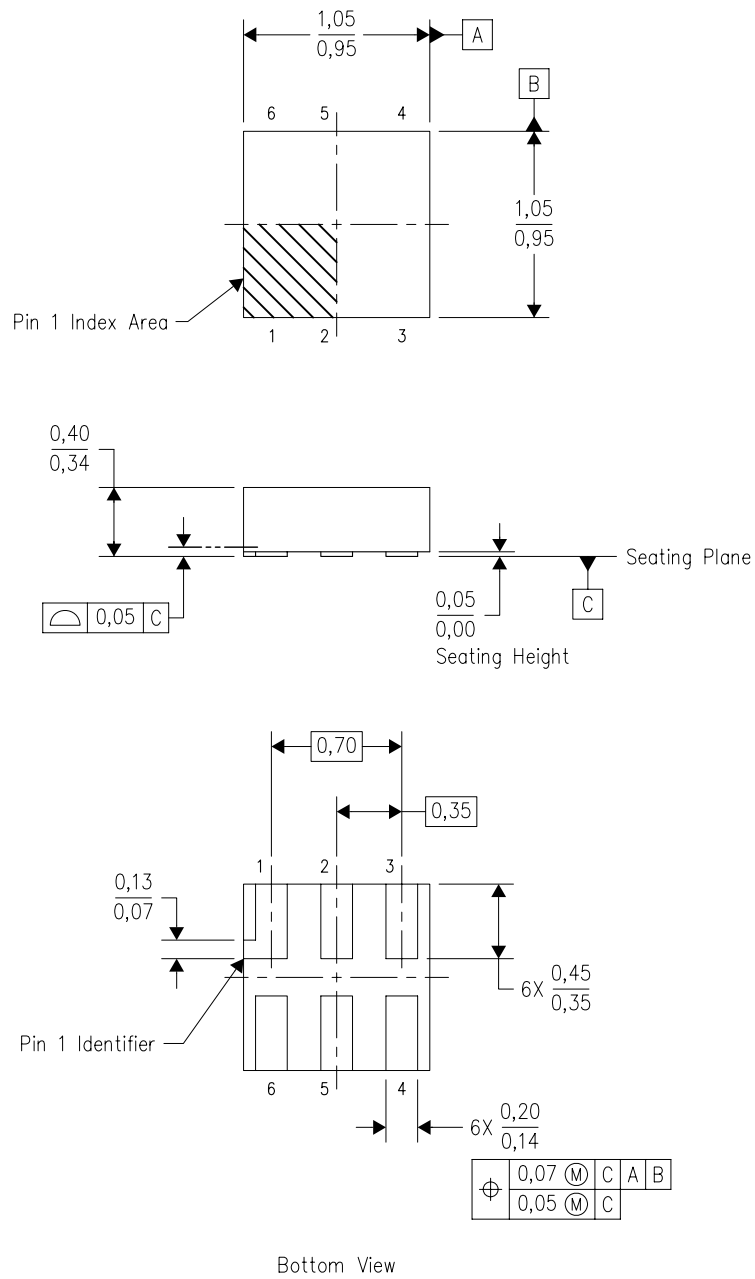


4207181/F 12/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. SON (Small Outline No-Lead) package configuration.
 - $\triangle D$ The exposed lead frame feature on side of package may or may not be present due to alternative lead frame designs.
 - E. This package complies to JEDEC MO-287 variation UFAD.
 - $\triangle F$ See the additional figure in the Product Data Sheet for details regarding the pin 1 identifier shape.

DSF (S-PX2SON-N6)

PLASTIC SMALL OUTLINE NO-LEAD

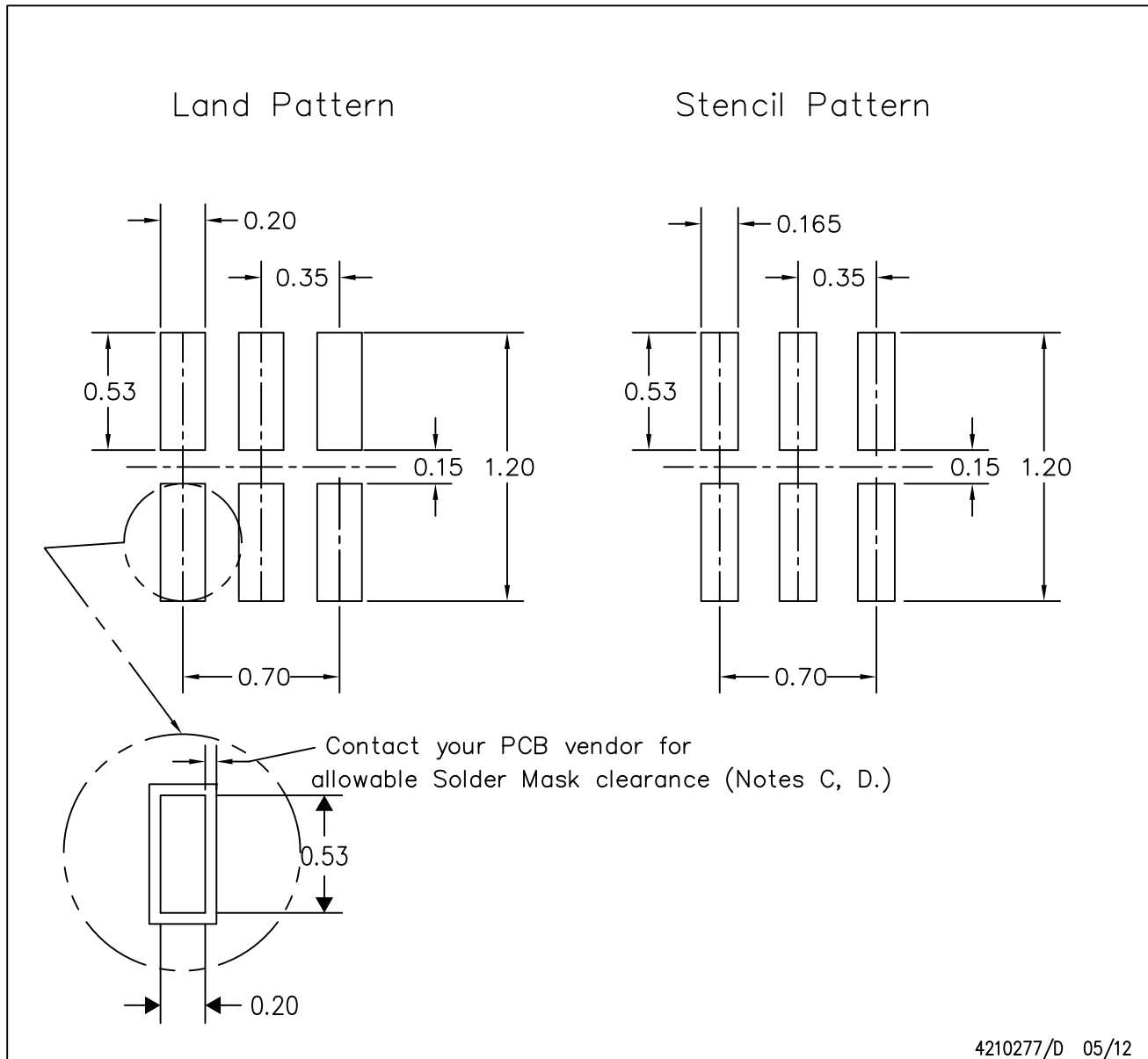


4208186/E 03/11

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - SON (Small Outline No-Lead) package configuration.
 - This package complies to JEDEC MO-287 variation X2AAF.

DSF (S-PX2SON-N6)

PLASTIC SMALL OUTLINE NO-LEAD

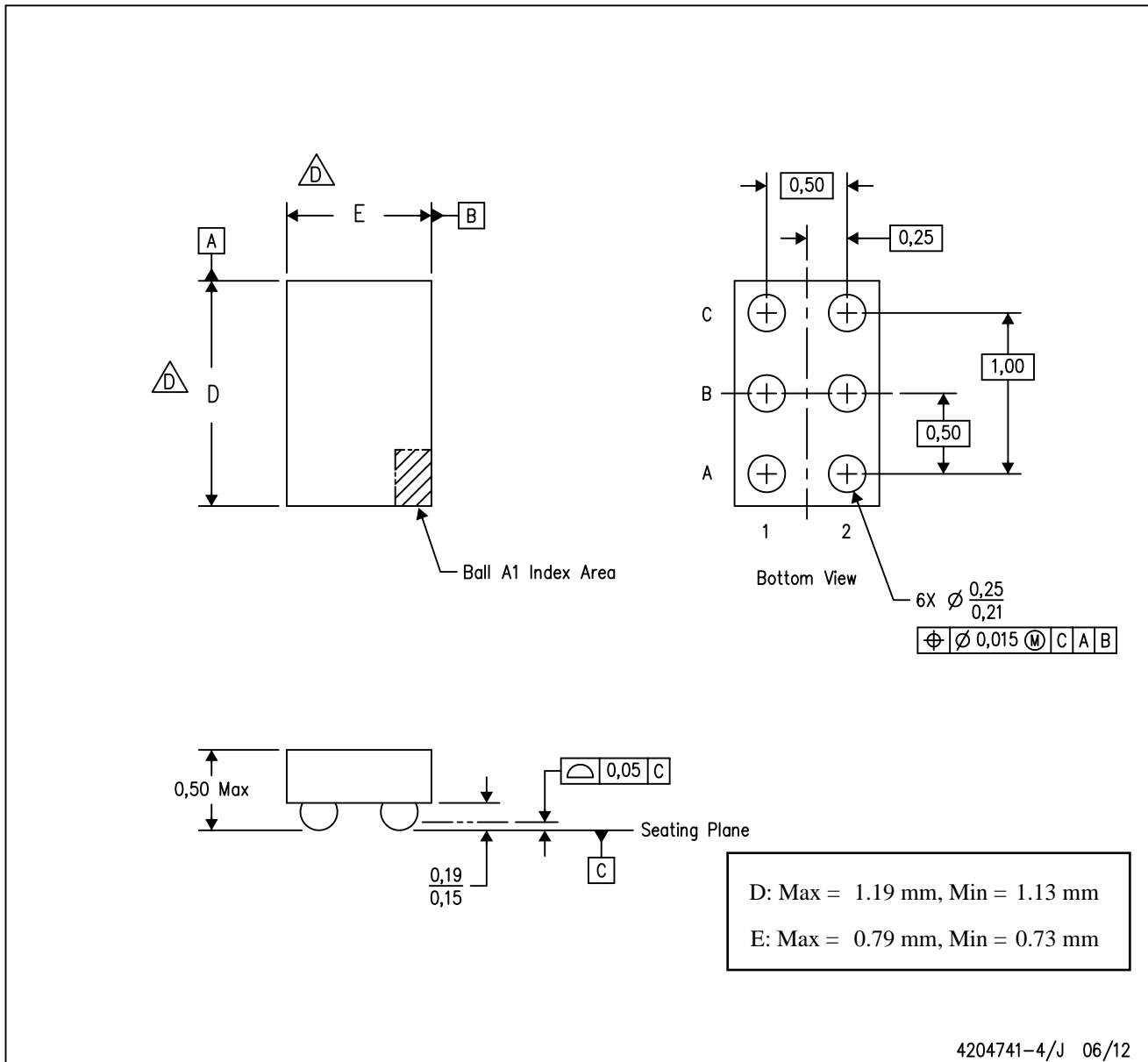


4210277/D 05/12

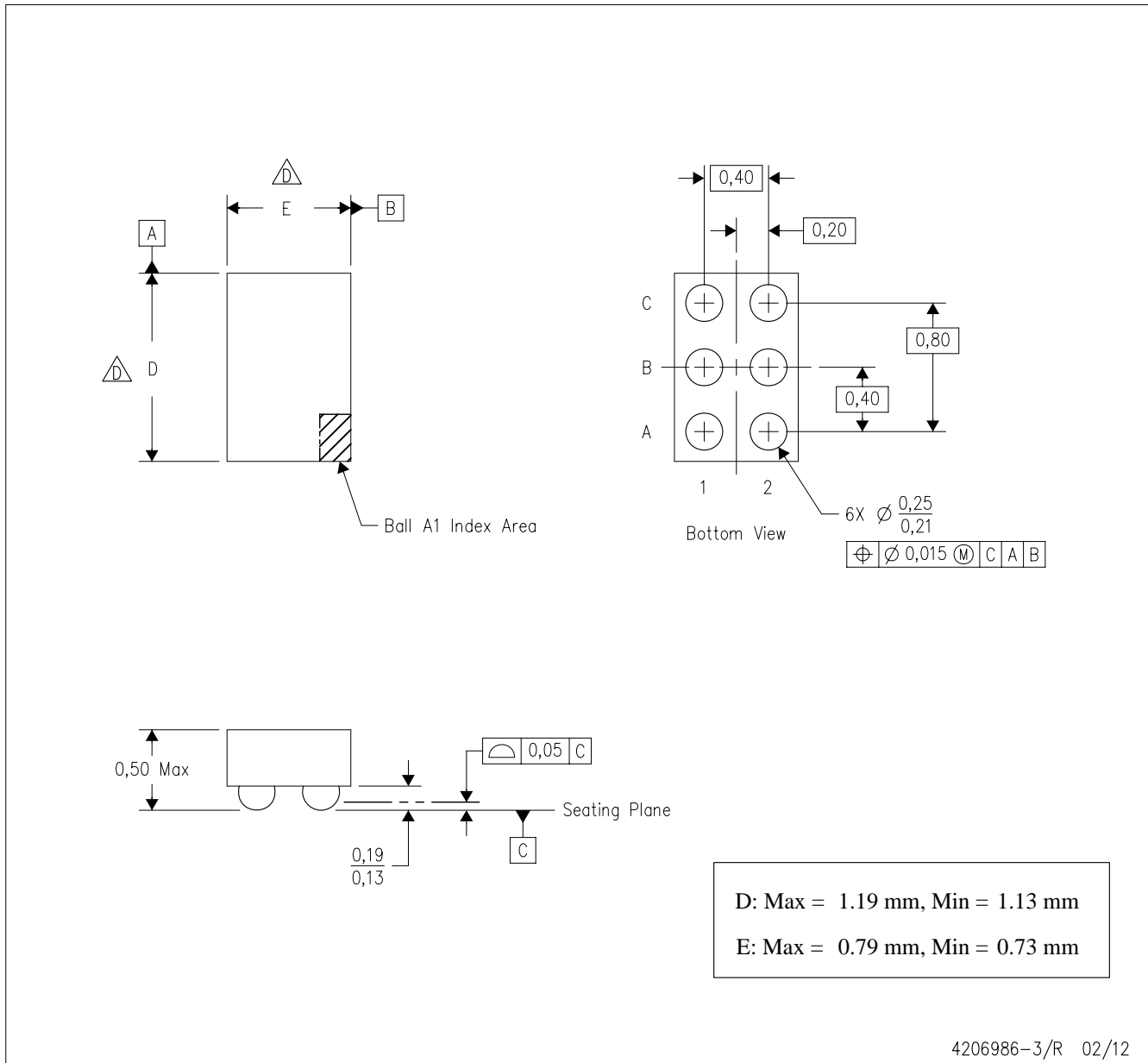
- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads. If 2 mil solder mask is outside PCB vendor capability, it is advised to omit solder mask.
 - E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
 - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - G. Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
 - H. Component placement force should be minimized to prevent excessive paste block deformation.

YZP (R-XBGA-N6)

DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.
 - The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
 - E. This package is a Pb-free solder ball design. Refer to the 6 YEP package (drawing 4204725) for tin-lead (SnPb).



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.
 - \triangle The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
 - E. Reference Product Data Sheet for array population.
2 x 3 matrix pattern is shown for illustration only.
 - F. This package contains Pb-free balls.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com