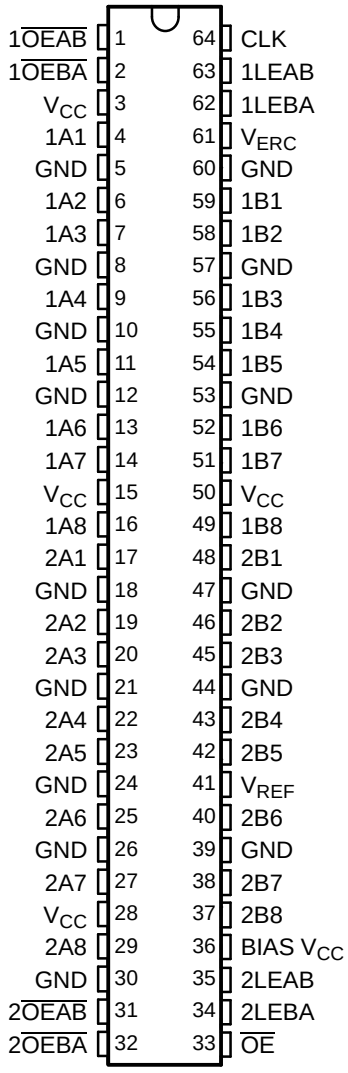
SN74GTL1655
16-BIT LVTTL-TO-GTL/GTL+ UNIVERSAL BUS TRANSCEIVER WITH LIVE INSERTION

SCBS696I – JULY 1997 – REVISED APRIL 2005

FEATURES

- **Member of the Texas Instruments Widebus™ Family**
- **UBT™ Transceiver Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Modes**
- **OEC™ Circuitry Improves Signal Integrity and Reduces Electromagnetic Interference**
- **Translates Between GTL/GTL+ Signal Level and LVTTL Logic Levels**
- **High-Drive (100 mA), Low-Output-Impedance (12 Ω) Bus Transceiver (B Port)**
- **Edge-Rate-Control Input Configures the B-Port Output Rise and Fall Times**
- **I_{off}, Power-Up 3-State, and BIAS V_{CC} Support Live Insertion**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors on A Port**
- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**

DGG PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The SN74GTL1655 is a high-drive (100 mA), low-output-impedance (12 Ω) 16-bit UBT™ transceiver that provides LVTTL-to-GTL/GTL+ and GTL/GTL+-to-LVTTL signal-level translation. This device is partitioned as two 8-bit transceivers and combines D-type flip-flops and D-type latches to allow for transparent, latched, and clocked modes of data transfer similar to the '16501 function. This device provides an interface between cards operating at LVTTL logic levels and a backplane operating at GTL/GTL+ signal levels. Higher-speed operation is a direct result of the reduced output swing (<1 V), reduced input threshold levels, and OEC™ circuitry. The high drive is suitable for driving double-terminated low-impedance backplanes using incident-wave switching.

The user has the flexibility of using this device at either GTL (V_{TT} = 1.2 V and V_{REF} = 0.8 V) or the preferred higher noise margin GTL+ (V_{TT} = 1.5 V and V_{REF} = 1 V) signal levels. GTL+ is the Texas Instruments derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD 8-3. The B port normally operates at GTL or GTL+ signal levels, while the A-port and control inputs are compatible with LVTTL logic levels, but are not 5-V tolerant. V_{REF} is the reference input voltage for the B port.

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DESCRIPTION/ORDERING INFORMATION (CONTINUED)

This device is partitioned uniquely as two 8-bit transceivers with individual latch timing and output signals, but with a common clock and output enable inputs for both transceiver words.

Data flow for each word is determined by the respective latch enables (LEAB and LEBA), output enables ($\overline{\text{OEAB}}$ and $\overline{\text{OEBA}}$), and clock (CLK). The output enables (1$\overline{\text{OEAB}}$, 1$\overline{\text{OEBA}}$, 2$\overline{\text{OEAB}}$, and 2$\overline{\text{OEBA}}$) control byte 1 and byte 2 data for the A-to-B and B-to-A directions, respectively.

For A-to-B data flow, the devices operate in the transparent mode when LEAB is high. When LEAB transitions low, the A data is latched independent of CLK high or low. If LEAB is low, the A data is registered on the CLK low-to-high transition. When $\overline{\text{OEAB}}$ is low, the outputs are active. With $\overline{\text{OEAB}}$ high, the outputs are in the high-impedance state.

Data flow for the B-to-A direction is identical, but uses $\overline{\text{OEBA}}$, LEBA, and CLK. Note that CLK is common to both directions and both 8-bit words. $\overline{\text{OE}}$ also is common and is used to disable all I/O ports simultaneously.

The SN74GTL1655 has adjustable edge-rate control (V_{ERC}). Changing V_{ERC} input voltage between GND and V_{CC} adjusts the B-port output rise and fall times. This allows the designer to optimize for various loading conditions.

This device is fully specified for live-insertion applications using I_{off}, power-up 3-state, and BIAS V_{CC}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict. The BIAS V_{CC} circuitry precharges and preconditions the B-port input/output connections, preventing disturbance of active data on the backplane during card insertion or removal, and permits true live-insertion capability.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry holds unused or undriven LVTTL inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

ORDERING INFORMATION

T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – DGG	Tape and reel	SN74GTL1655DGGR	GTL1655

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLES

FUNCTION(1)

INPUTS				OUTPUT B	MODE
$\overline{OEAB}$	LEAB	CLK	A		
H	X	X	X	Z	Isolation
L	H	X	L	L	Transparent
L	H	X	H	H	Transparent
L	L	↑	L	L	Registered
L	L	↑	H	H	Registered
L	L	H	X	B_0(2)	Previous state
L	L	L	X	B_0(3)	Previous state

(1) A-to-B data flow is shown. B-to-A flow is similar, but uses $\overline{OEBA}$, LEBA, and CLK.
(2) Output level before the indicated steady-state input conditions were established, provided that CLK was high before LEAB went low
(3) Output level before the indicated steady-state input conditions were established

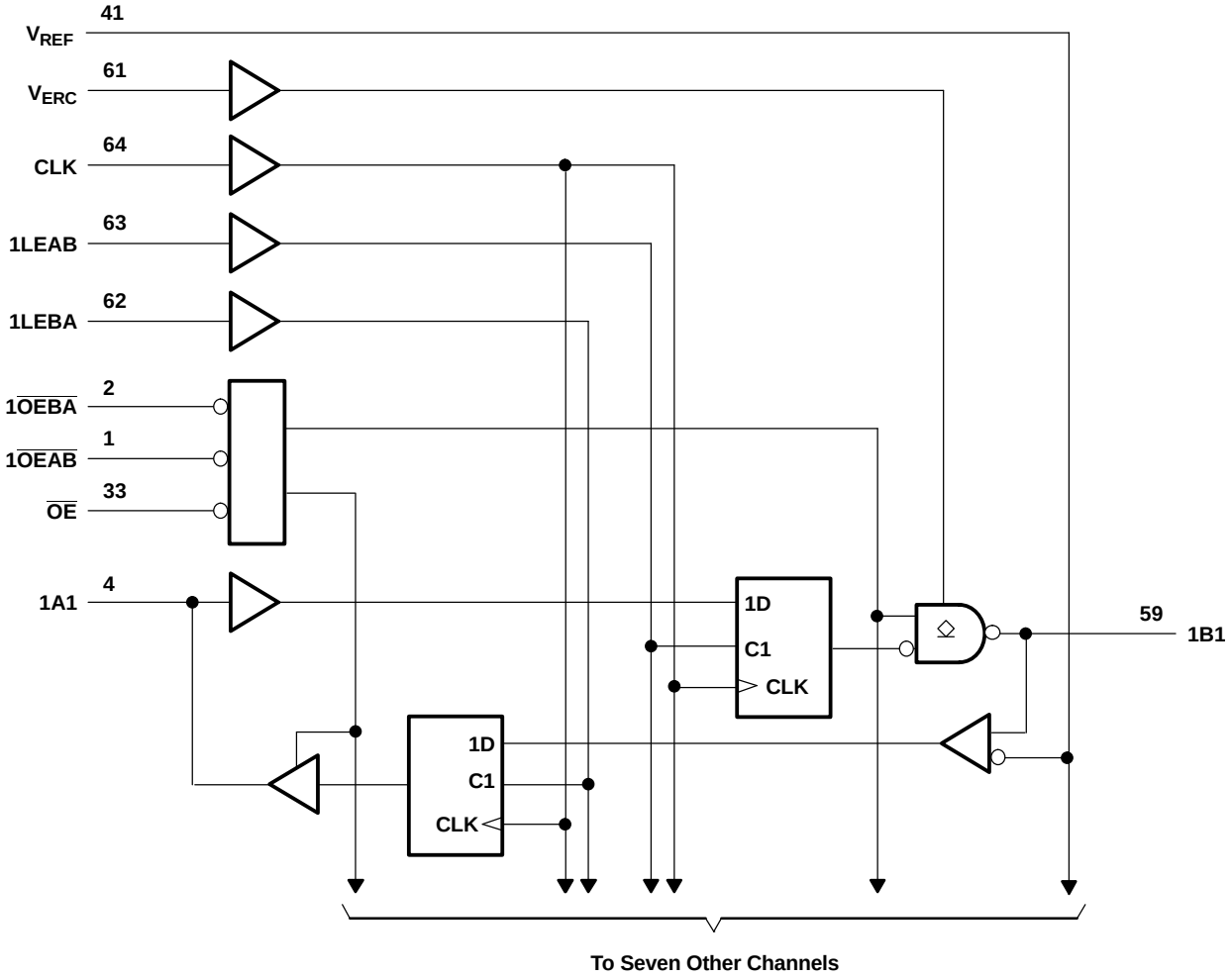
OUTPUT ENABLE

INPUTS			OUTPUTS	
$\overline{OE}$	$\overline{OEAB}$	$\overline{OEBA}$	A PORT	B PORT
L	L	L	Active	Active
L	L	H	Z	Active
L	H	L	Active	Z
L	H	H	Z	Z
H	X	X	Z	Z

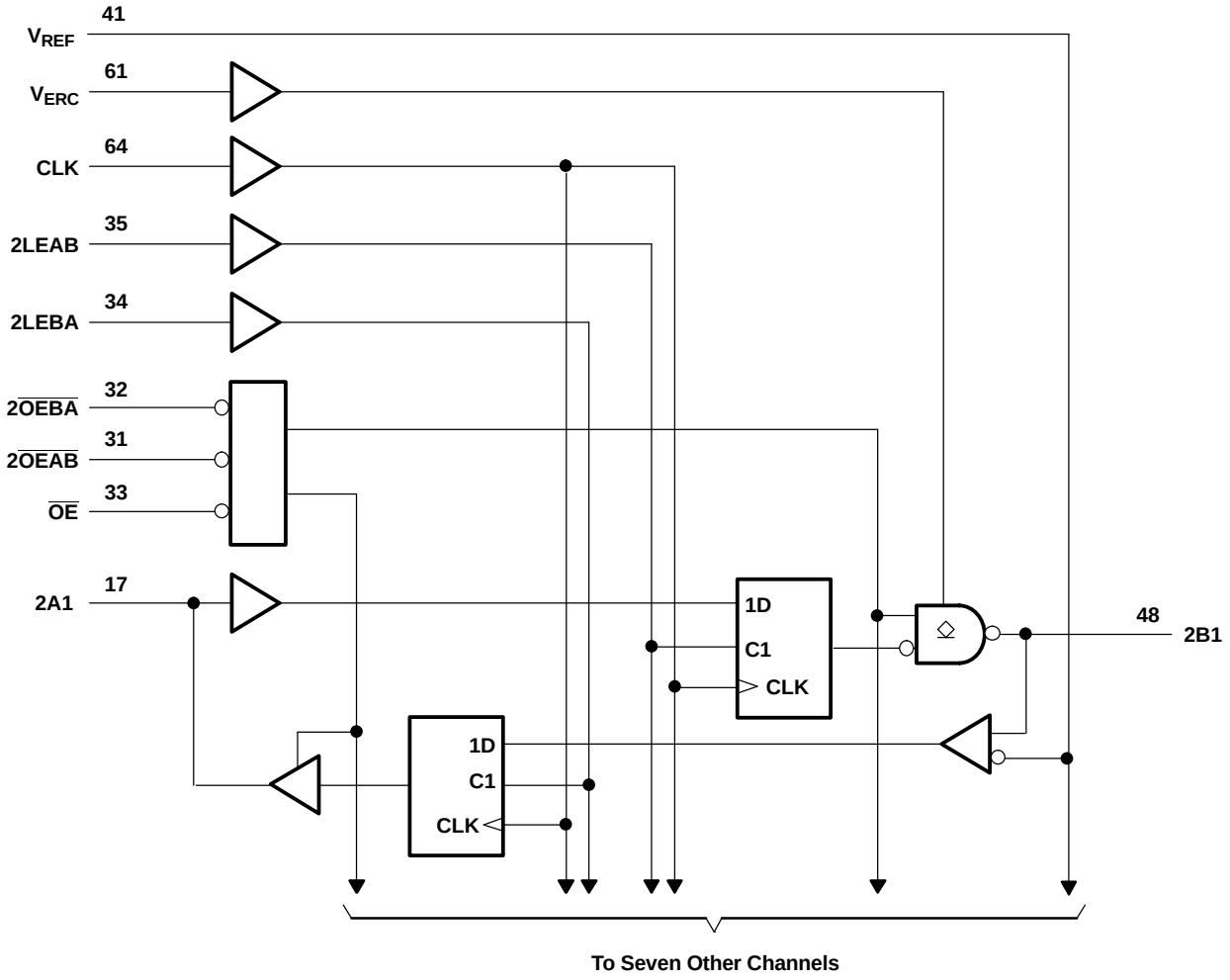
B-PORT EDGE-RATE CONTROL (V_{ERC})

input V_{ERC}		OUTPUT B-PORT EDGE RATE
LOGIC LEVEL	NOMINAL VOLTAGE	
H	V_{CC}	Slow
L	GND	Fast

LOGIC DIAGRAM (POSITIVE LOGIC)



LOGIC DIAGRAM (POSITIVE LOGIC) (CONTINUED)



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC} BIAS V_{CC}	Supply voltage range		–0.5	4.6	V
V_I	Input voltage range(2)	A-port and control inputs	–0.5	4.6	V
		B port, V_{ERC}, and V_{REF}	–0.5	4.6	
V_O	Voltage range applied to any output in the high or power-off state(2)	A port	–0.5	4.6	V
		B port	–0.5	4.6	
I_O	Current into any output in the low state	A port		48	mA
		B port		200	
I_O	Current into any A-port output in the high state(3)			48	mA
	Continuous current through each V_{CC} or GND			±100	mA
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
θ_{JA}	Package thermal impedance(4)			55	°C/W
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) The current flows only when the output is in the high state and $V_O > V_{CC}$.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions(1)(2)(3)(4)

			MIN	NOM	MAX	UNIT
BIAS V_{CC}	Supply voltage		3	3.3	3.6	V
V_{TT}	Termination voltage	GTL	1.14	1.2	1.26	V
		GTL+	1.35	1.5	1.65	
V_{REF}	Reference voltage	GTL	0.74	0.8	0.87	V
		GTL+	0.87	1	1.1	
V_I	Input voltage	B port	0		V_{TT}	V
		Except B port	0		V_{CC}	
V_{IH}	High-level input voltage	B port	V_{REF} + 50 mV			V
		V_{ERC}	V_{CC} – 0.6	V_{CC}		
		Except B port and ERC	2			
V_{IL}	Low-level input voltage	B port			V_{REF} – 50 mV	V
		V_{ERC}		GND	0.6	
		Except B port and ERC			0.8	
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	A port			–24	mA
I_{OL}	Low-level output current	A port			24	mA
		B port			100	
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200			µs/V
T_A	Operating free-air temperature		–40		85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
(2) Normal connection sequence is GND first, BIAS V_{CC} = 3.3 V second, and V_{CC} = 3.3 V, I/O, control inputs, V_{TT} and V_{REF} (any order) last. However, if the B-port I/O precharge is not required, the acceptable connection sequence is GND first and V_{CC} = 3.3 V, BIAS V_{CC} = 3.3 V, I/O, control inputs, V_{TT} and V_{REF} (any order) last. When V_{CC} is connected, the BIAS V_{CC} circuitry is disabled.
(3) V_{TT} and R_{TT} can be adjusted to accommodate backplane impedances if the dc recommended I_{OL} ratings are not exceeded.
(4) V_{REF} can be adjusted to optimize noise margins, but normally is two-thirds V_{TT}.

Electrical Characteristics

over recommended operating free-air temperature range, V_{REF} = 1 V and V_{TT} = 1.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IK}		V_{CC} = 3 V,	I_I = –18 mA			–1.2	V
V_{OH}	A port	V_{CC} = 3 V to 3.6 V,	I_{OH} = –100 µA	V_{CC} – 0.2			V
		V_{CC} = 3 V	I_{OH} = –12 mA	2.4			
			I_{OH} = –24 mA	2.2			
V_{OL}	A port	V_{CC} = 3 V to 3.6 V,	I_{OL} = 100 µA			0.2	V
		V_{CC} = 3 V	I_{OL} = 12 mA			0.4	
			I_{OL} = 24 mA			0.55	
	B port	V_{CC} = 3 V	I_{OL} = 40 mA			0.2	
			I_{OL} = 80 mA			0.4	
			I_{OL} = 100 mA			0.5	
I_I	Control inputs	V_{CC} = 3.6 V	V_I = V_{CC} or GND			±10	µA
	B port		V_I = V_{TT} or GND			±10	
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 3.6 V			±100	µA
$I_{I(hold)}$	A port	V_{CC} = 3 V	V_I = 0.8 V	75			µA
			V_I = 2 V	–75			
		V_{CC} = 3.6 V(2),	V_I = 0 to V_{CC}			±500	
I_{OZH}	B port	V_{CC} = 3.6 V,	V_O = 1.5 V			10	µA
I_{OZL}	B port	V_{CC} = 3.6 V,	V_O = 0.4 V			–10	µA
I_{OZ}(3)	A port	V_{CC} = 3.6 V,	V_O = V_{CC} or GND			±10	µA
I_{OZPU}	A port	V_{CC} = 0 to 3.6 V, V_O = 0.5 V to 3 V, $\overline{OE}$ = low				±50	µA
I_{OZPD}	A port	V_{CC} = 3.6 V to 0, V_O = 0.5 V to 3 V, $\overline{OE}$ = low				±50	µA
I_{CC}	A or B port	V_{CC} = 3.6 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			80	mA
			Outputs low			80	
			Outputs disabled			80	
ΔI_{CC}(4)	Except B port	V_{CC} = 3.6 V, A-port or control inputs at V_{CC} or GND, One input at V_{CC} – 0.6 V				1	mA
C_i	Control inputs	V_I = V_{CC} or 0			3	5	pF
C_{io}	A port	V_O = V_{CC} or 0			5	6	pF
	B port				6	8	

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.
(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.
(4) This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

Live-Insertion Specifications

over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
I_{CC} (BIAS V_{CC})		V_{CC} = 0 to 3 V	V_O (B port) = 0 to 1.2 V,	V_I (BIAS V_{CC}) = 3 V to 3.6 V		5	mA
		V_{CC} = 3 V to 3.6 V				10	µA
V_O	B port	V_{CC} = 0,	V_I (BIAS V_{CC}) = 3.3 V		1	1.2	V
I_O	B port	V_{CC} = 0,	V_O (B port) = 0.4 V,	V_I (BIAS V_{CC}) = 3 V to 3.6 V	–1		µA
		V_{CC} = 0 to 3.6 V,	$\overline{OE}$ = 3.3 V			100	
		V_{CC} = 0 to 1.5 V,	$\overline{OE}$ = 0 to 3.3 V			100	

Timing Requirements

over recommended ranges of supply voltage and operating free-air temperature,
V_{TT} = 1.2 V, V_{REF} = 0.8 V, and V_{ERC} = V_{CC} or GND for GTL (unless otherwise noted)

				MIN	MAX	UNIT
f_{clock}	Clock frequency				160	MHz
t_w	Pulse duration	LE high		3		ns
		CLK high or low		3		
t_{su}	Setup time	Data before CLK↑		2.7		ns
		Data before LE↓	CLK high	2.8		
			CLK low	2.6		
t_h	Hold time	Data after CLK↑		0.4		ns
		Data after LE↓	CLK high or low	0.9		

A-to-B Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature,
V_{TT} = 1.2 V, V_{REF} = 0.8 V, and V_{ERC} = V_{CC} or GND for GTL (see Figure 1)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	UNIT
f_{max}				160			MHz
t_{PLH}		A, V_{ERC} = V_{CC}	B	3.1		5.2	ns
t_{PHL}				2.6		6.2	
t_{PLH}		CLK, V_{ERC} = V_{CC}	B	3.4		5.5	ns
t_{PHL}				2.4		5.8	
t_{PLH}		LEAB, V_{ERC} = V_{CC}	B	3.5		5.8	ns
t_{PHL}				2.6		6.4	
t_{en}		$\overline{OEAB}$ or $\overline{OE}$, V_{ERC} = V_{CC}	B	3.3		5.4	ns
t_{dis}				2.7		5.9	
t_{PLH}		A, V_{ERC} = GND	B	2.3		4.3	ns
t_{PHL}				1.9		4.3	
t_{PLH}		CLK, V_{ERC} = GND	B	2.7		4.8	ns
t_{PHL}				1.8		4.3	
t_{PLH}		LEAB, V_{ERC} = GND	B	2.8		4.9	ns
t_{PHL}				2		4.8	
t_{en}		$\overline{OEAB}$ or $\overline{OE}$, V_{ERC} = GND	B	2.5		4.5	ns
t_{dis}				2		4.2	
t_r	V_{ERC} = GND	Transition time, B outputs (0.6 V to 1 V)			0.6		ns
	V_{ERC} = V_{CC}				1.2		
t_f	V_{ERC} = GND	Transition time, B outputs (1 V to 0.6 V)			1.1		ns
	V_{ERC} = V_{CC}				1.7		
$t_{sk(o)}$ (1)		Skew between drivers in the same package switching in the same direction				1	ns
$t_{sk(o)}$ (2)		Skew between drivers switching in any direction in the same package				1	ns

(1) Skew values are applicable for through mode only.
(2) Skew values are applicable for CLK mode only, with all outputs switching simultaneously.

B-to-A Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature,
V_{TT} = 1.2 V and V_{REF} = 0.8 V for GTL (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f_{max}			160		MHz
t_{PLH}	B	A	1.8	4.7	ns
t_{PHL}			2.3	4.6	
t_{PLH}	CLK	A	1.6	4	ns
t_{PHL}			1.5	3.4	
t_{PLH}	LEBA	A	1.7	4	ns
t_{PHL}			1.4	3.5	
t_{en}	$\overline{OEBA}$ or $\overline{OE}$	A	1.2	4.2	ns
t_{dis}			1.2	6.1	
$t_{sk(o)}$ (1)	Skew between drivers in the same package switching in the same direction			1	ns
$t_{sk(o)}$ (2)	Skew between drivers switching in any direction in the same package			1	ns

(1) Skew values are applicable for through mode only.
(2) Skew values are applicable for CLK mode only, with all outputs switching simultaneously.

Timing Requirements

over recommended ranges of supply voltage and operating free-air temperature,
V_{TT} = 1.5 V, V_{REF} = 1 V, and V_{ERC} = V_{CC} or GND for GTL+ (unless otherwise noted)

				MIN	MAX	UNIT
f_{clock}	Clock frequency				160	MHz
t_w	Pulse duration	LE high		3		ns
		CLK high or low		3		
t_{su}	Setup time	Data before CLK↑		2.7		ns
		Data before LE↓	CLK high	2.8		
			CLK low	2.6		
t_h	Hold time	Data after CLK↑		0.4		ns
		Data after LE↓	CLK high or low	0.9		

A-to-B Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature,
V_{TT} = 1.5 V, V_{REF} = 1 V, and V_{ERC} = V_{CC} or GND for GTL+ (see Figure 1)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	UNIT
f_{max}				160			MHz
t_{PLH}		A, V_{ERC} = V_{CC}	B	3		5.1	ns
t_{PHL}				2.9		6.5	
t_{PLH}		CLK, V_{ERC} = V_{CC}	B	3.4		5.4	ns
t_{PHL}				2.7		6.2	
t_{PLH}		LEAB, V_{ERC} = V_{CC}	B	3.5		5.7	ns
t_{PHL}				2.8		6.7	
t_{en}		$\overline{OEAB}$, V_{ERC} = V_{CC}	B	3.3		5.4	ns
t_{dis}				3		6.3	
t_{en}		$\overline{OE}$, V_{ERC} = V_{CC}	B	3		5.5	ns
t_{dis}				3.6		5.8	
t_{PLH}		A, V_{ERC} = GND	B	2.3		4.3	ns
t_{PHL}				2		4.4	
t_{PLH}		CLK, V_{ERC} = GND	B	2.7		4.8	ns
t_{PHL}				1.9		4.5	
t_{PLH}		LEAB, V_{ERC} = GND	B	2.8		4.9	ns
t_{PHL}				2.1		4.9	
t_{en}		$\overline{OEAB}$, V_{ERC} = GND	B	2.5		4.5	ns
t_{dis}				2.1		4.4	
t_{en}		$\overline{OE}$, V_{ERC} = GND	B	2.5		4.6	ns
t_{dis}				2.9		4.9	
t_r	V_{ERC} = GND	Transition time, B outputs (0.6 V to 1.3 V)			0.9		ns
	V_{ERC} = V_{CC}				1.7		
t_f	V_{ERC} = GND	Transition time, B outputs (1.3 V to 0.6 V)			1.6		ns
	V_{ERC} = V_{CC}				2.4		
$t_{sk(o)}$ (1)		Skew between drivers in the same package switching in the same direction				1	ns
$t_{sk(o)}$ (2)		Skew between drivers switching in any direction in the same package				1	ns

(1) Skew values are applicable for through mode only.
(2) Skew values are applicable for CLK mode only, with all outputs switching simultaneously.

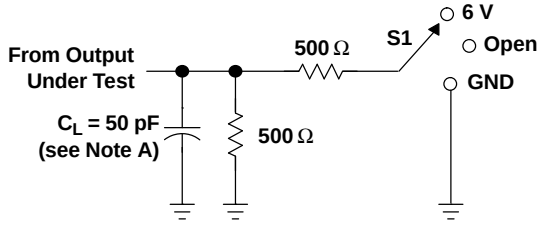
B-to-A Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature,
V_{TT} = 1.5 V and V_{REF} = 1 V for GTL+ (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f_{max}			160		MHz
t_{PLH}	B	A	2	4.8	ns
t_{PHL}			2.4	4.7	
t_{PLH}	CLK	A	1.6	4.4	ns
t_{PHL}			1.5	3.4	
t_{PLH}	LEBA	A	1.7	4	ns
t_{PHL}			1.4	3.5	
t_{en}	$\overline{OEBA}$	A	1.2	4.2	ns
t_{dis}			1.2	6.1	
t_{en}	$\overline{OE}$	A	1.2	4.7	ns
t_{dis}			1.2	6.3	
$t_{sk(o)}$ (1)	Skew between drivers in the same package switching in the same direction			1	ns
$t_{sk(o)}$ (2)	Skew between drivers switching in any direction in the same package			1	ns

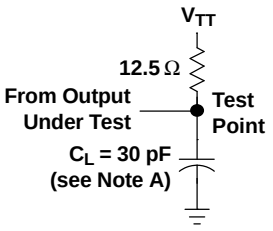
(1) Skew values are applicable for through mode only.
(2) Skew values are applicable for CLK mode only, with all outputs switching simultaneously.

PARAMETER MEASUREMENT INFORMATION

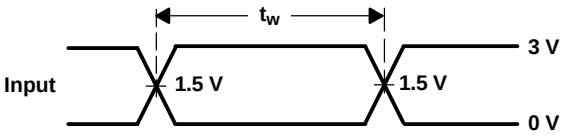


LOAD CIRCUIT FOR A OUTPUTS

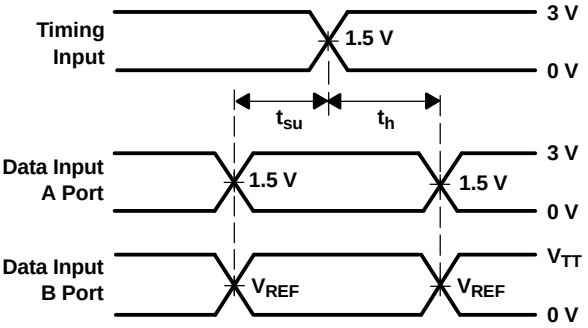
TEST	S1
t_{PLH}/t_{PHL} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 6 V GND



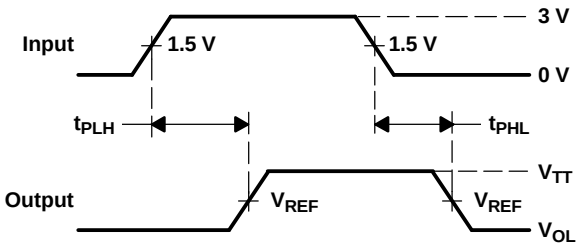
LOAD CIRCUIT FOR B OUTPUTS



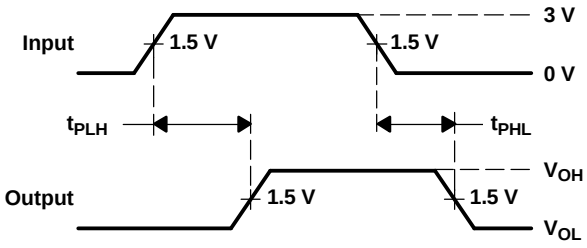
VOLTAGE WAVEFORMS
PULSE DURATION



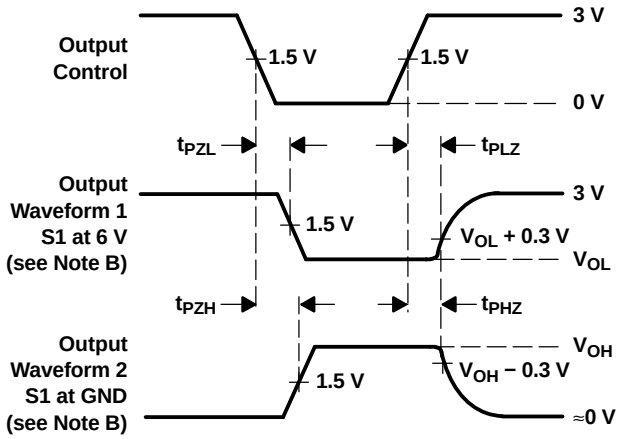
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(CLK to B port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(CLK to A port)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
(A port)

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
SN74GTL1655DGGR	ACTIVE	TSSOP	DGG	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74GTL1655DGGRE4	ACTIVE	TSSOP	DGG	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74GTL1655DGGRG4	ACTIVE	TSSOP	DGG	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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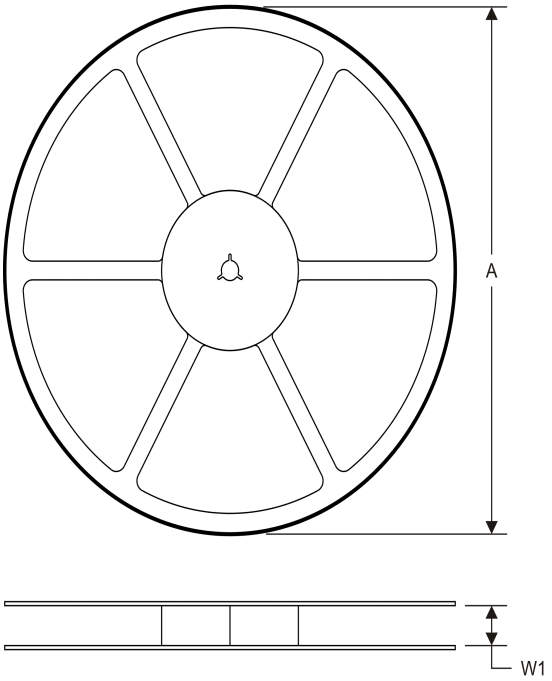
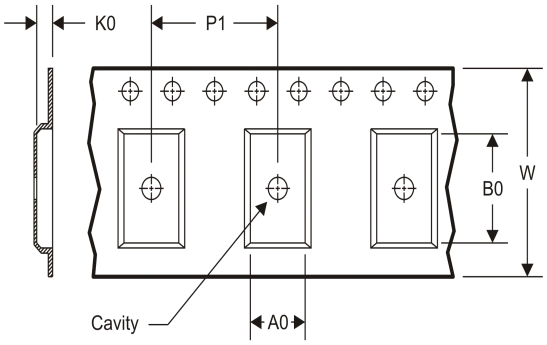
TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



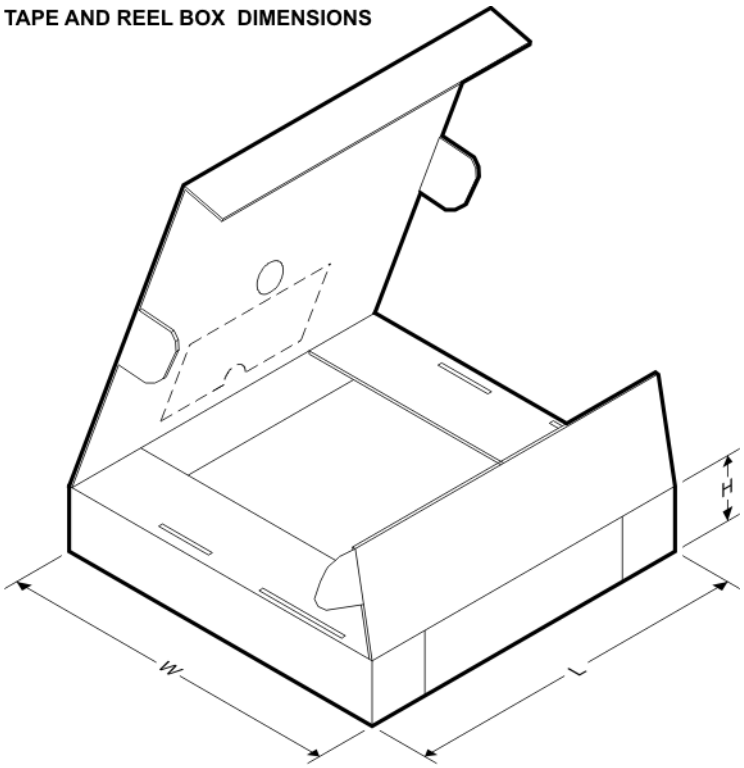
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74GTL1655DGGR	TSSOP	DGG	64	2000	330.0	24.4	8.4	17.3	1.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

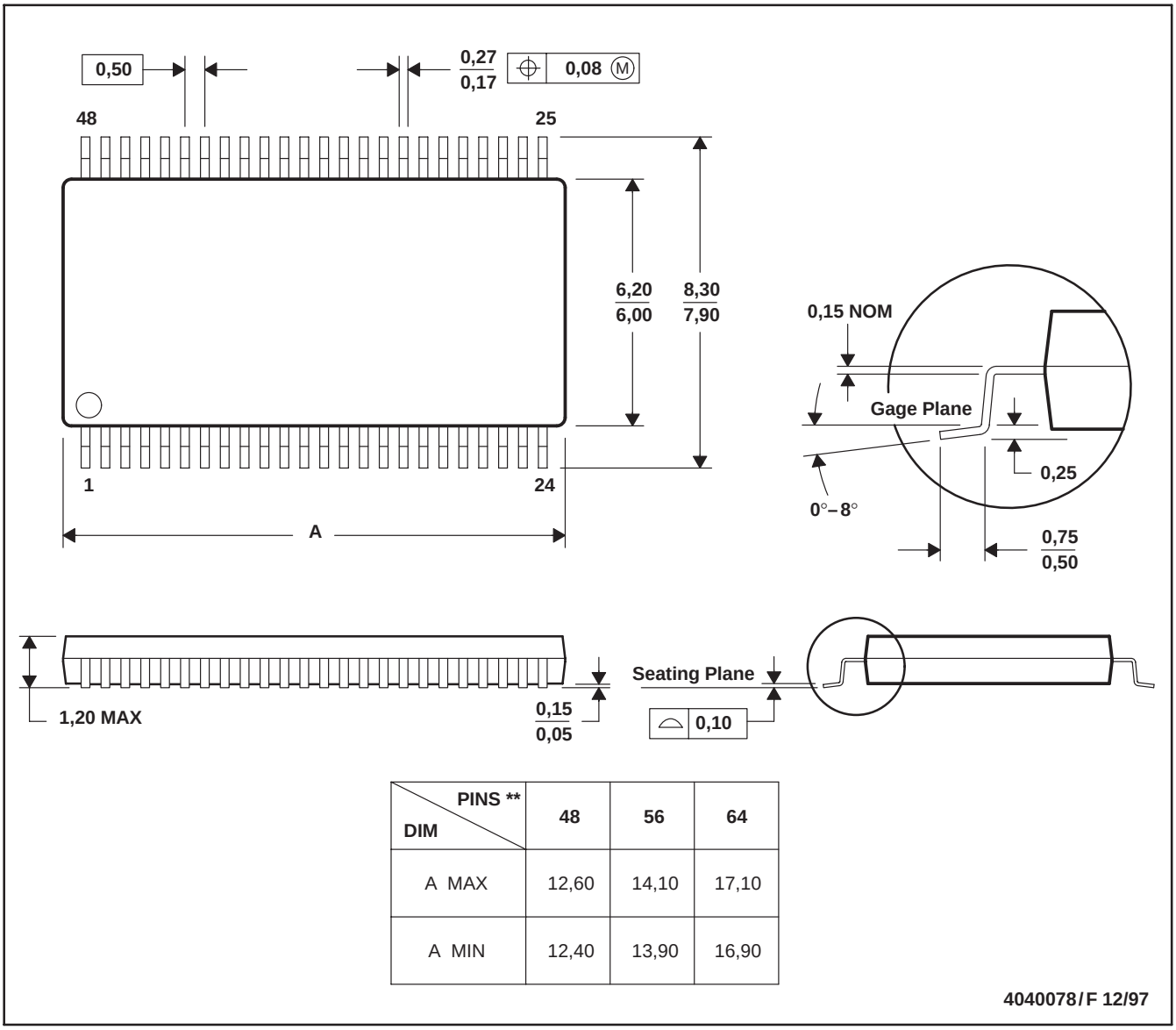


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74GTL1655DGGR	TSSOP	DGG	64	2000	367.0	367.0	45.0

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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