- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs**

- **Dependable Texas Instruments Quality and Reliability**

description

These devices contain two independent D-type positive-edge-triggered flip-flops. A low level at the preset or clear inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the D input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.
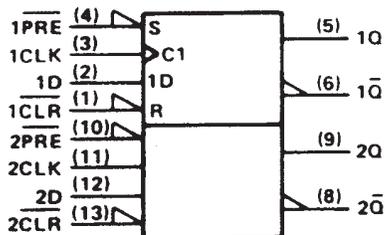
The SN54' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

SN5474 . . . J PACKAGE
SN54LS74A, SN54S74 . . . J OR W PACKAGE
SN7474 . . . N PACKAGE
SN74LS74A, SN74S74 . . . D OR N PACKAGE
(TOP VIEW)


```
1CLR [ 1   U  14 ] VCC
 1D  [ 2      13 ] 2CLR
1CLK [ 3      12 ] 2D
1PRE [ 4      11 ] 2CLK
 1Q  [ 5      10 ] 2PRE
 1Q  [ 6       9 ] 2Q
GND  [ 7       8 ] 2Q
```

SN5474 . . . W PACKAGE
(TOP VIEW)

```
1CLK [ 1   U  14 ] 1PRE
 1D  [ 2      13 ] 1Q
1CLR [ 3      12 ] 1Q
VCC  [ 4      11 ] GND
2CLR [ 5      10 ] 2Q
 2D  [ 6       9 ] 2Q
2CLK [ 7       8 ] 2PRE
```

SN54LS74A, SN54S74 . . . FK PACKAGE
(TOP VIEW)

```
        1D  1CLR  NC  VCC  2CLR
         3    2    1   20   19
1CLK [ 4                    18 ] 2D
 NC  [ 5                    17 ] NC
1PRE [ 6                    16 ] 2CLK
 NC  [ 7                    15 ] NC
 1Q  [ 8                    14 ] 2PRE
         9   10   11   12   13
        1Q  GND  NC   2Q   2Q
```

NC - No internal connection

FUNCTION TABLE

INPUTS				OUTPUTS	
PRE	CLR	CLK	D	Q	Q̄
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

† The output levels in this configuration are not guaranteed to meet the minimum levels in V_{OH} if the lows at preset and clear are near V_{IL} maximum. Furthermore, this configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.
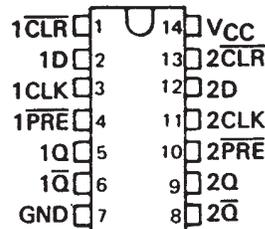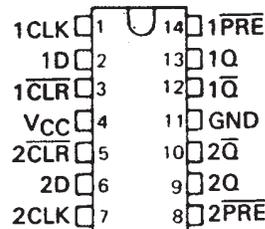
logic symbol‡


```
1PRE  (4)  ⊳ S
1CLK  (3)  ⊳ C1
 1D   (2)    1D
1CLR  (1)  ⊳ R

2PRE  (10) ⊳
2CLK  (11) ⊳
 2D   (12)
2CLR  (13) ⊳
            (5)  1Q
            (6)  1Q
            (9)  2Q
            (8)  2Q
```

‡This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

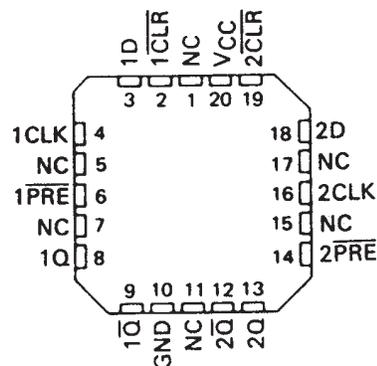## logic diagram (positive logic)
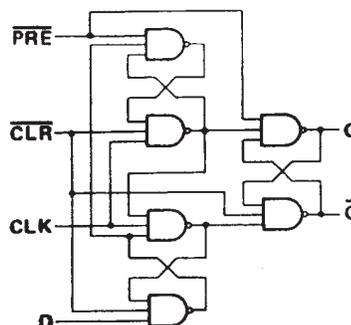
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TEXAS INSTRUMENTS

SN5474, SN54LS74A, SN54S74
SN7474. SN74LS74A, SN74S74
DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

SDLS119 – DECEMBER 1983 – REVISED MARCH 1988

schematics of inputs and outputs

'74

'S74

Tables in images.

For '74 EQUIVALENT OF EACH INPUT:

I_{IL} MAX	R_{eq} NOM
−1.6 mA	4 kΩ
−3.2 mA	2 kΩ

For 'S74 EQUIVALENT OF EACH INPUT:

I_{IL} MAX	R_{eq} NOM
−2 mA	2.8 kΩ
−4 mA	1.4 kΩ
−6 mA	940 Ω

TEXAS
INSTRUMENTS

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schematic
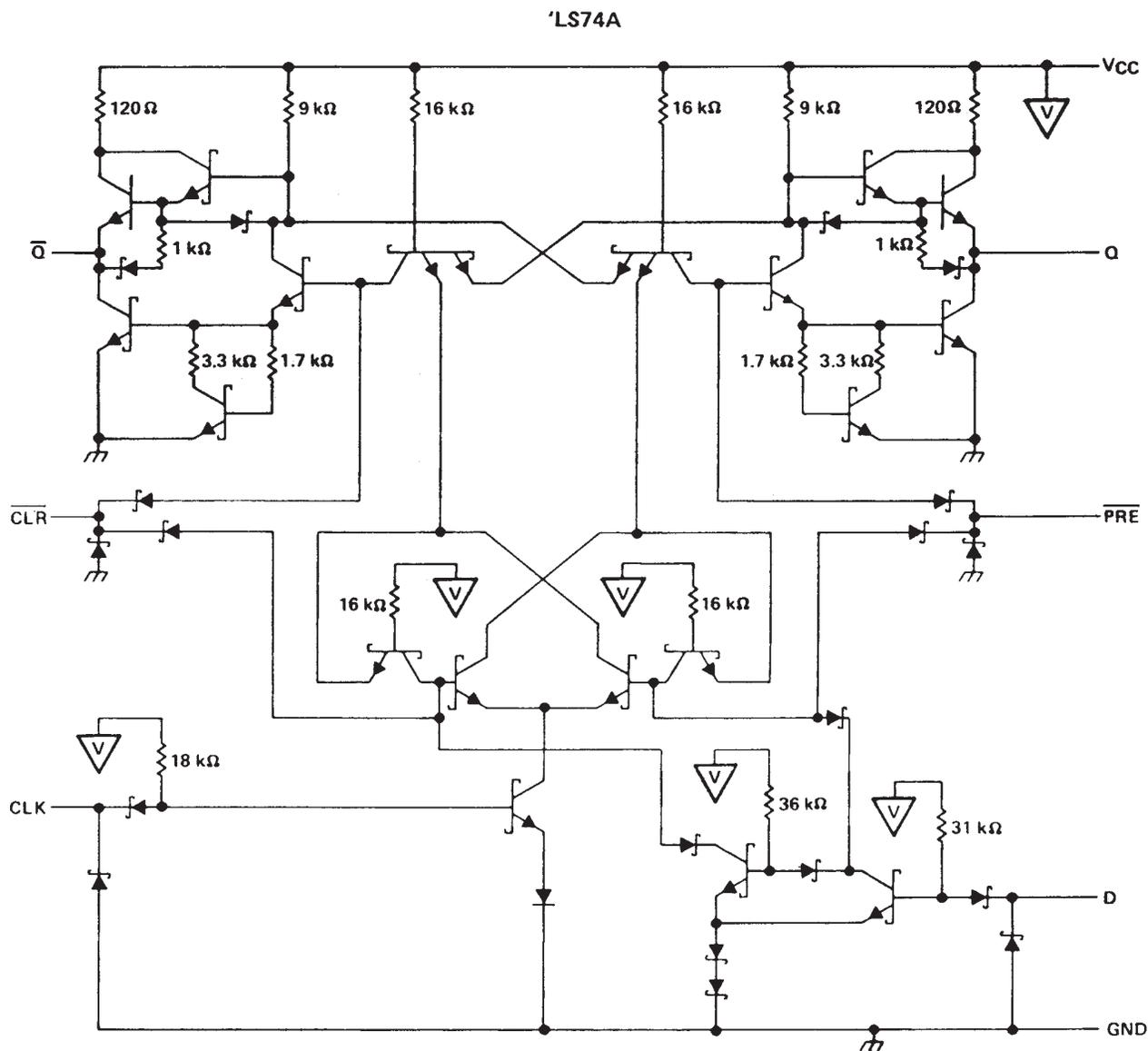
'LS74A

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . 7 V
Input voltage: '74, 'S74 . . . . 5.5 V
            'LS74A . . . . 7 V
Operating free-air temperature range: SN54' . . . . –55°C to 125°C
                                  SN74' . . . . 0°C to 70°C
Storage temperature range . . . . –65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

			SN5474			SN7474			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				− 0.4			− 0.4	mA
I_{OL}	Low-level output current				16			16	mA
t_w	Pulse duration	CLK high	30			30			ns
		CLK low	37			37			
		$\overline{PRE}$ or $\overline{CLR}$ low	30			30			
t_{su}	Input setup time before CLK↑		20			20			ns
t_h	Input hold time-data after CLK↑		5			5			ns
T_A	Operating free-air temperature		− 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS[†]			SN5474			SN7474			UNIT
					MIN	TYP[‡]	MAX	MIN	TYP[‡]	MAX	
V_{IK}		V_{CC} = MIN,	I_I = − 12 mA				− 1.5			− 1.5	V
V_{OH}		V_{CC} = MIN,	V_{IH} = 2 V,	V_{IL} = 0.8 V,	2.4	3.4		2.4	3.4		V
		I_{OH} = − 0.4 mA									
V_{OL}		V_{CC} = MIN,	V_{IH} = 2 V,	V_{IL} = 0.8 V,		0.2	0.4		0.2	0.4	V
		I_{OL} = 16 mA									
I_I		V_{CC} = MAX,	V_I = 5.5 V				1			1	mA
I_{IH}	D						40			40	μA
	$\overline{CLR}$	V_{CC} = MAX,	V_I = 2.4 V				120			120	
	All Other						80			80	
I_{IL}	D						− 1.6			− 1.6	mA
	$\overline{PRE}$[§]	V_{CC} = MAX,	V_I = 0.4 V				− 1.6			− 1.6	
	$\overline{CLR}$[§]						− 3.2			− 3.2	
	CLK						− 3.2			− 3.2	
I_{OS}[¶]		V_{CC} = MAX			− 20		− 57	− 18		− 57	mA
I_{CC}[#]		V_{CC} = MAX,	See Note 2			8.5	15		8.5	15	mA

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
[‡]All typical values are at V_{CC} = 5 V, T_A = 25°C.
[§]Clear is tested with preset high and preset is tested with clear high.
[¶]Not more than one output should be shown at a time.
[#]Average per flip-flop.
NOTE 2: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

switching charateristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}					15	25		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	R_L = 400 Ω,	C_L = 15 pF			25	ns
t_{PHL}							40	ns
t_{PLH}	CLK	Q or $\overline{Q}$				14	25	ns
t_{PHL}						20	40	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

recommended operating conditions

		SN54LS74A			SN74LS74A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
f_{clock}	Clock frequency	0		25	0		25	MHz
t_w	Pulse duration — CLK high	25			25			ns
	Pulse duration — $\overline{PRE}$ or $\overline{CLR}$ low	25			25			
t_{su}	Setup time-before CLK↑ — High-level data	20			20			ns
	Setup time-before CLK↑ — Low-level data	20			20			
t_h	Hold time-data after CLK↑	5			5			ns
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS[†]			SN54LS74A			SN74LS74A			UNIT
					MIN	TYP[‡]	MAX	MIN	TYP[‡]	MAX	
V_{IK}		V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}		V_{CC} = MIN,	V_{IH} = 2 V,	V_{IL} = MAX,	2.5	3.4		2.7	3.4		V
		I_{OH} = −0.4 mA									
V_{OL}		V_{CC} = MIN,	V_{IL} = MAX,	V_{IH} = 2 V,		0.25	0.4		0.25	0.4	V
		I_{OL} = 4 mA									
		V_{CC} = MIN,	V_{IL} = MAX,	V_{IH} = 2 V,					0.35	0.5	
		I_{OL} = 8 mA									
I_I	D or CLK	V_{CC} = MAX,	V_I = 7 V				0.1			0.1	mA
	$\overline{CLR}$ or $\overline{PRE}$						0.2			0.2	
I_{IH}	D or CLK	V_{CC} = MAX,	V_I = 2.7 V				20			20	μA
	$\overline{CLR}$ or $\overline{PRE}$						40			40	
I_{IL}	D or CLK	V_{CC} = MAX,	V_I = 0.4 V				−0.4			−0.4	mA
	$\overline{CLR}$ or $\overline{PRE}$						−0.8			−0.8	
I_{OS}§		V_{CC} = MAX,	See Note 4		−20		−100	−20		−100	mA
I_{CC} (Total)		V_{CC} = MAX,	See Note 2			4	8		4	8	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 2: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.
NOTE 4: For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with V_O = 2.25 V and 2.125 V for the 54 family and the 74 family, respectively, with the minimum and maximum limits reduced to one half of their stated values.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}			R_L = 2 kΩ,	C_L = 15 pF	25	33		MHz
t_{PLH}	$\overline{CLR}$, $\overline{PRE}$ or CLK	Q or $\overline{Q}$				13	25	ns
t_{PHL}						25	40	ns

Note 3: Load circuits and voltage waveforms are shown in Section 1.

TEXAS
INSTRUMENTS

DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

recommended operating conditions

			SN54S74			SN74S74			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				− 1			− 1	mA
I_{OL}	Low-level output current				20			20	mA
t_w	Pulse duration	CLK high	6			6			ns
		CLK low	7.3			7.3			
		$\overline{CLR}$ or $\overline{PRE}$ low	7			7			
t_{su}	Setup time, before CLK ↑	High-level data	3			3			ns
		Low-level data	3			3			
t_h	Input hold time - data after CLK ↑		2			2			ns
T_A	Operating free-air temperature		− 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS[†]	SN54S74			SN74S74			UNIT
			MIN	TYP[‡]	MAX	MIN	TYP[‡]	MAX	
V_{IK}		V_{CC} = MIN, $\quad$ I_I = − 18 mA,			− 1.2			− 1.2	V
V_{OH}		V_{CC} = MIN, $\quad$ V_{IH} = 2 V, $\quad$ V_{IL} = 0.8 V, I_{OH} = − 1 mA	2.5	3.4		2.7	3.4		V
V_{OL}		V_{CC} = MIN, $\quad$ V_{IH} = 2 V, $\quad$ V_{IL} = 0.8 V, I_{OL} = 20 mA			0.5			0.5	V
I_I		V_{CC} = MAX, $\quad$ V_I = 5.5 V			1			1	mA
I_{IH}	D	V_{CC} = MAX, $\quad$ V_I = 2.7 V			50			50	µA
	$\overline{CLR}$				150			150	
	$\overline{PRE}$ or CLK				100			100	
I_{IL}	D	V_{CC} = MAX, $\quad$ V_I = 0.5 V			− 2			− 2	mA
	$\overline{CLR}$[¶]				− 6			− 6	
	$\overline{PRE}$[¶]				− 4			− 4	
	CLK				− 4			− 4	
I_{OS}[§]		V_{CC} = MAX	− 40		− 100	− 40		− 100	mA
I_{CC}[#]		V_{CC} = MAX, $\quad$ See Note 2		15	25		15	25	mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C.
[§] Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
[¶] Clear is tested with preset high and preset is tested with clear high.
[#] Average per flip-flop.
NOTE 2: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}					75	110		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	R_L = 280 Ω,	C_L = 15 pF		4	6	ns
t_{PHL}	$\overline{PRE}$ or $\overline{CLR}$ (CLK high)	$\overline{Q}$ or Q				9	13.5	ns
	$\overline{PRE}$ or $\overline{CLR}$ (CLK low)					5	8	
t_{PLH}	CLK	Q or $\overline{Q}$				6	9	ns
t_{PHL}						6	9	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

TEXAS
INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Peak Temp [3]	Samples (Requires Login)
JM38510/00205BCA	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	
JM38510/00205BDA	OBSOLETE	CFP	W	14		TBD	Call TI	Call TI	
JM38510/00205BDA	OBSOLETE	CFP	W	14		TBD	Call TI	Call TI	
JM38510/07101BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
JM38510/07101BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
JM38510/07101BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	
JM38510/07101BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	
JM38510/30102B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
JM38510/30102B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
JM38510/30102BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
JM38510/30102BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
JM38510/30102BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	
JM38510/30102BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	
JM38510/30102SCA	ACTIVE	CDIP	J	14	25	TBD	A42	N / A for Pkg Type	
JM38510/30102SCA	ACTIVE	CDIP	J	14	25	TBD	A42	N / A for Pkg Type	
JM38510/30102SDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	
JM38510/30102SDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	
M38510/07101BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
M38510/07101BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
M38510/07101BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	
M38510/07101BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	
M38510/30102B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
M38510/30102B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
M38510/30102BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
M38510/30102BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
M38510/30102BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	
M38510/30102BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	
M38510/30102SCA	ACTIVE	CDIP	J	14	25	TBD	A42	N / A for Pkg Type	
M38510/30102SCA	ACTIVE	CDIP	J	14	25	TBD	A42	N / A for Pkg Type	
M38510/30102SDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Peak Temp [3]	Samples (Requires Login)
M38510/30102SDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	
SN5474J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	
SN5474J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	
SN54LS74AJ	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
SN54LS74AJ	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
SN54S74J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
SN54S74J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
SN7474DR	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	
SN7474DR	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	
SN7474N	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	
SN7474N	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	
SN7474N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	
SN7474N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	
SN74LS74AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS74AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS74ADBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS74ADBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS74ADBRE4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS74ADBRE4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS74ADBRG4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS74ADBRG4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS74ADE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS74ADE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Peak Temp [3]	Samples (Requires Login)
SN74LS74ADG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS74ADG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS74ADR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS74ADR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS74ADRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS74ADRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS74ADRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS74ADRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS74AJ	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	
SN74LS74AJ	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	
SN74LS74AN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74LS74AN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74LS74AN3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	
SN74LS74AN3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	
SN74LS74ANE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74LS74ANE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74LS74ANSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS74ANSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS74ANSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS74ANSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74S74D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Peak Temp [3]	Samples (Requires Login)
SN74S74D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74S74DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74S74DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74S74DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74S74DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74S74N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74S74N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74S74N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	
SN74S74N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	
SN74S74NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74S74NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74S74NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74S74NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74S74NSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74S74NSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74S74NSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74S74NSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SNJ5474J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	
SNJ5474J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	
SNJ5474W	OBSOLETE	CFP	W	14		TBD	Call TI	Call TI	
SNJ5474W	OBSOLETE	CFP	W	14		TBD	Call TI	Call TI	
SNJ54LS74AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54LS74AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Peak Temp [3]	Samples (Requires Login)
SNJ54LS74AJ	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
SNJ54LS74AJ	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
SNJ54LS74AW	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	
SNJ54LS74AW	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	
SNJ54S74FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54S74FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54S74J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
SNJ54S74J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
SNJ54S74W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	
SNJ54S74W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN5474, SN54LS74A, SN54LS74A-SP, SN54S74, SN7474, SN74LS74A, SN74S74 :

- Catalog: SN7474, SN74LS74A, SN54LS74A, SN74S74

- Military: SN5474, SN54LS74A, SN54S74

- Space: SN54LS74A-SP

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Military - QML certified for Military and Defense Applications

- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

![Texas Instruments logo] **PACKAGE MATERIALS INFORMATION**

TAPE AND REEL INFORMATION

REEL DIMENSIONS
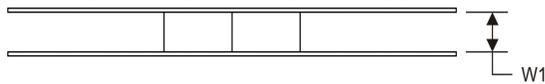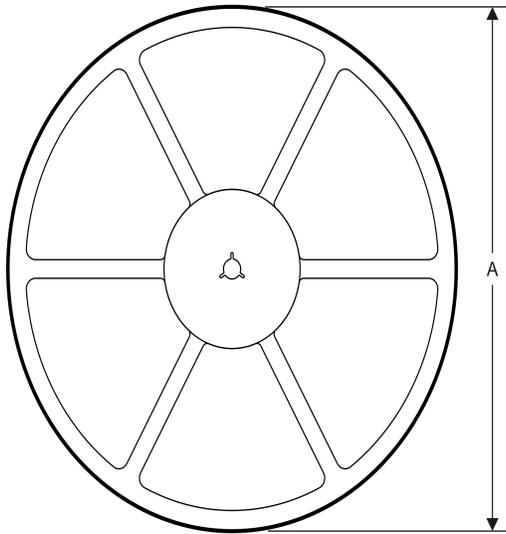
TAPE DIMENSIONS
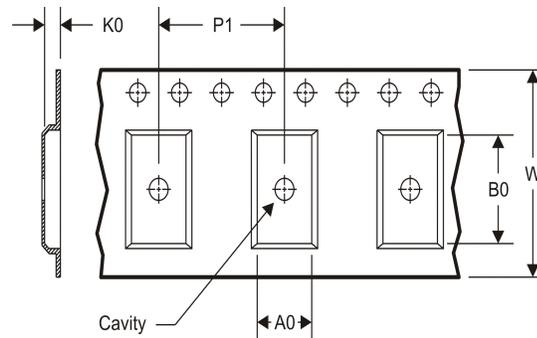
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS74ADBR	SSOP	DB	14	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74LS74ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LS74ANSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74S74NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS
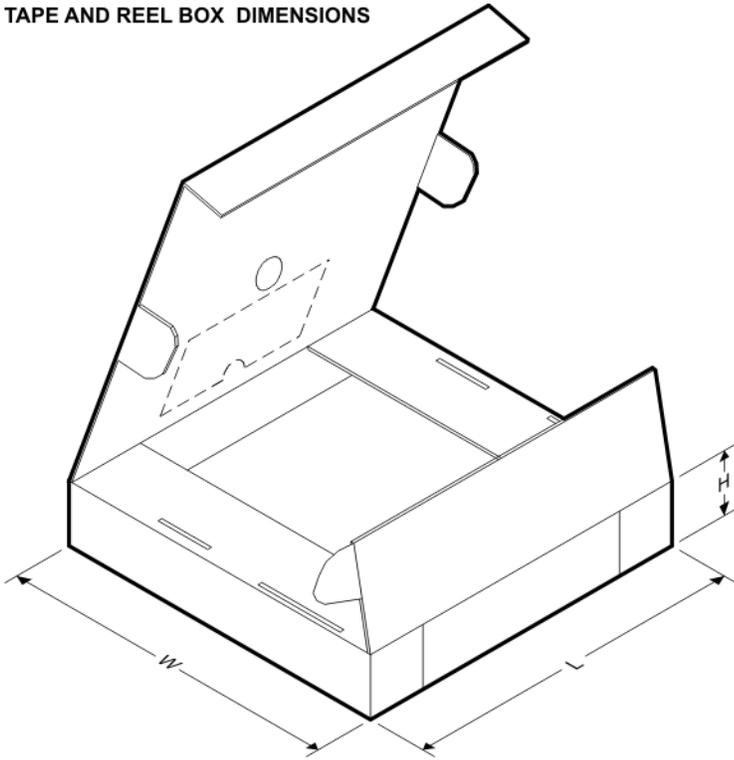
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS74ADBR	SSOP	DB	14	2000	367.0	367.0	38.0
SN74LS74ADR	SOIC	D	14	2500	367.0	367.0	38.0
SN74LS74ANSR	SO	NS	14	2000	367.0	367.0	38.0
SN74S74NSR	SO	NS	14	2000	367.0	367.0	38.0
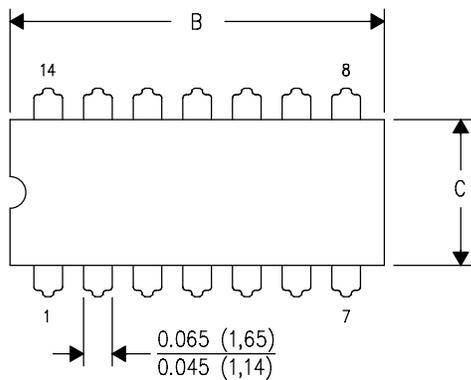
PINS ** DIM	14	16	18	20
[A]	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

C

1   7

$\frac{0.065\ (1,65)}{0.045\ (1,14)}$

0.005 (0,13) MIN

$\frac{0.060\ (1,52)}{0.015\ (0,38)}$

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

$\frac{0.026\ (0,66)}{0.014\ (0,36)}$

0.100 (2,54)

[A]

0°-15°

$\frac{0.014\ (0,36)}{0.008\ (0,20)}$
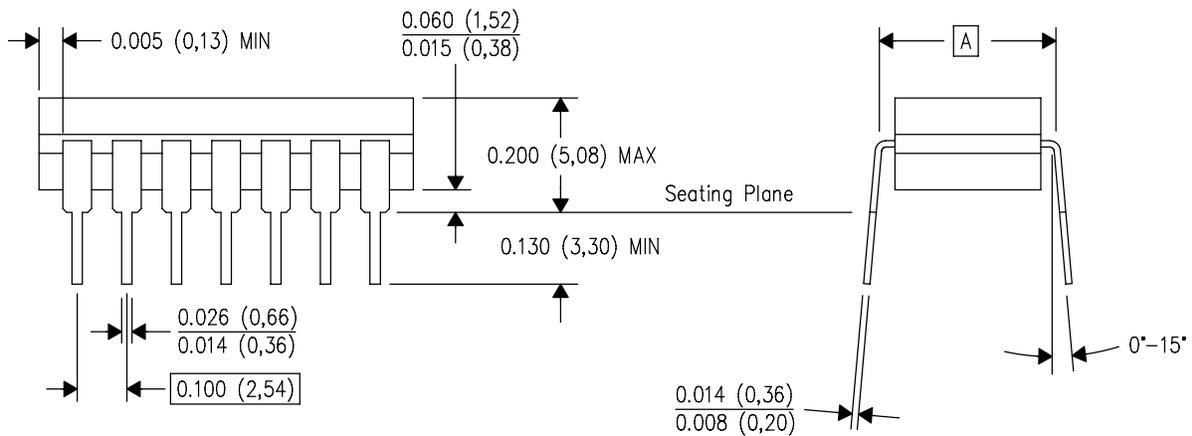
4040083/F 03/03

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   This package is hermetically sealed with a ceramic lid using glass frit.
         D.   Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
         E.   Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R–GDFP–F14)   CERAMIC DUAL FLATPACK
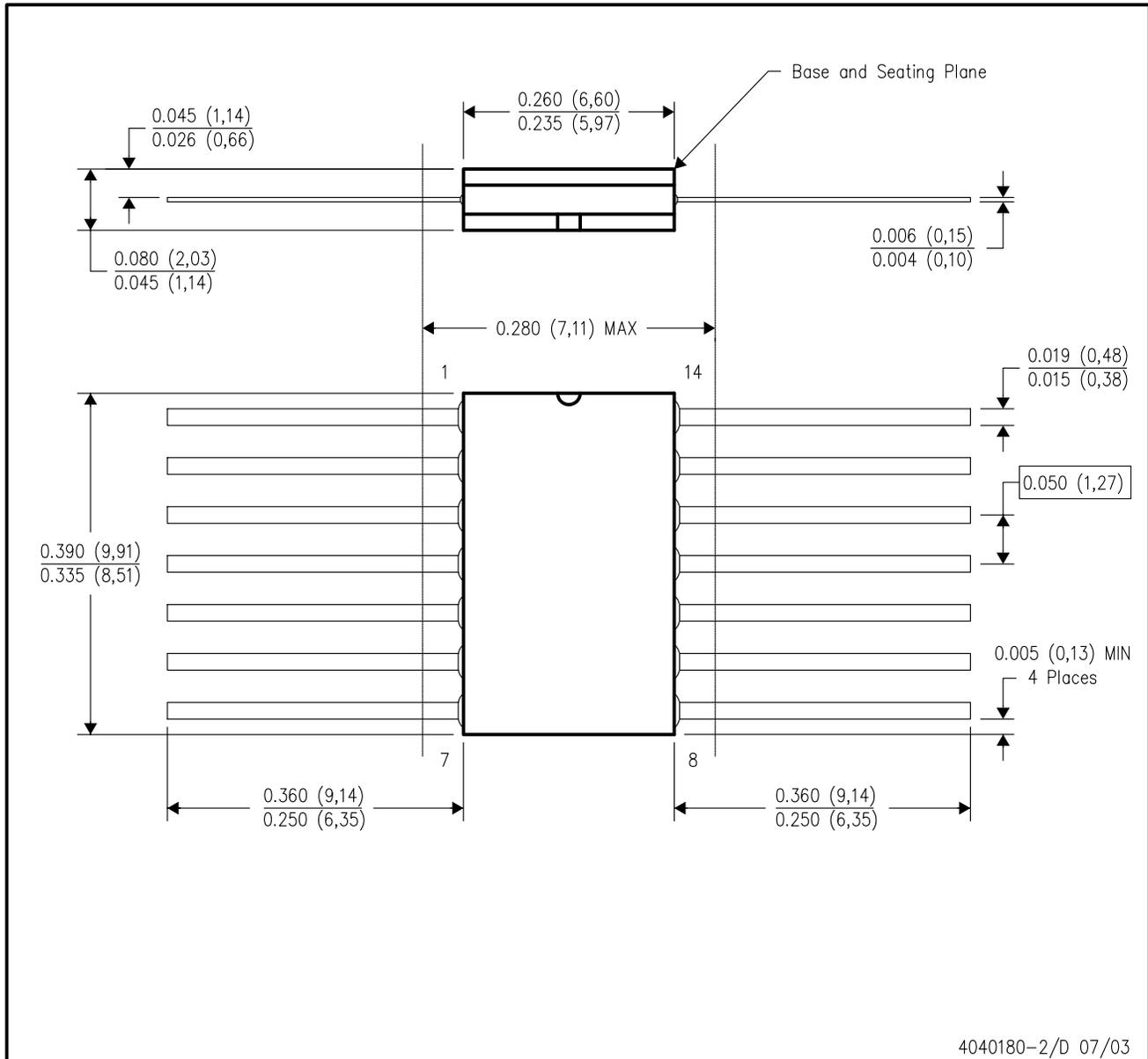
Base and Seating Plane

0.045 (1,14)
0.026 (0,66)

0.260 (6,60)
0.235 (5,97)

0.080 (2,03)
0.045 (1,14)

0.006 (0,15)
0.004 (0,10)

0.280 (7,11) MAX

0.019 (0,48)
0.015 (0,38)

1   14

0.050 (1,27)

0.390 (9,91)
0.335 (8,51)

0.005 (0,13) MIN
4 Places

7   8

0.360 (9,14)
0.250 (6,35)

0.360 (9,14)
0.250 (6,35)

4040180–2/D 07/03

NOTES: A.   All linear dimensions are in inches (millimeters).
          B.   This drawing is subject to change without notice.
          C.   This package can be hermetically sealed with a ceramic lid using glass frit.
          D.   Index point is provided on cap for terminal identification only.
          E.   Falls within MIL STD 1835 GDFP1–F14 and JEDEC MO–092AB

FK (S−CQCC−N**)   LEADLESS CERAMIC CHIP CARRIER
28 TERMINAL SHOWN
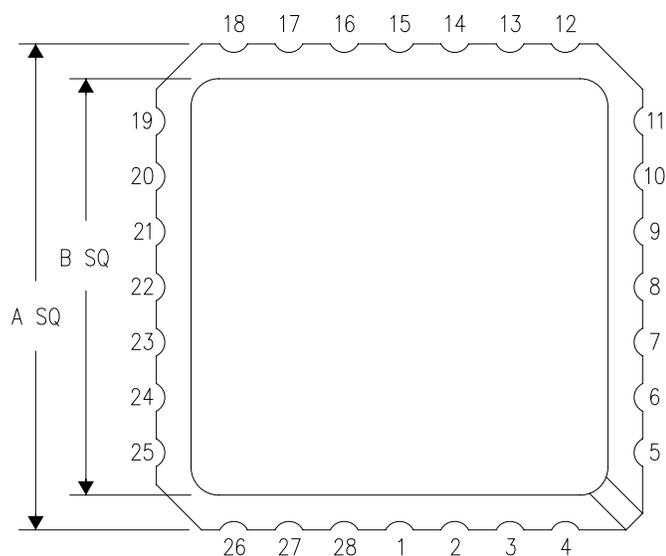
NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

$\frac{0.020\ (0,51)}{0.010\ (0,25)}$

$\frac{0.020\ (0,51)}{0.010\ (0,25)}$

$\frac{0.080\ (2,03)}{0.064\ (1,63)}$

$\frac{0.055\ (1,40)}{0.045\ (1,14)}$

$\frac{0.045\ (1,14)}{0.035\ (0,89)}$

$\frac{0.028\ (0,71)}{0.022\ (0,54)}$

0.050 (1,27)

$\frac{0.045\ (1,14)}{0.035\ (0,89)}$
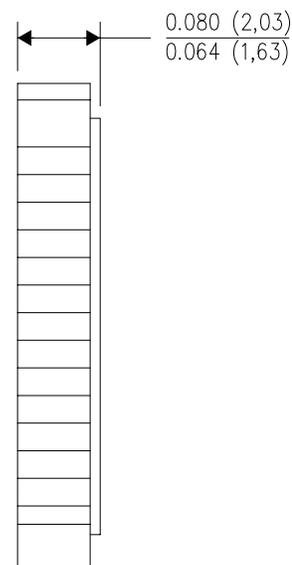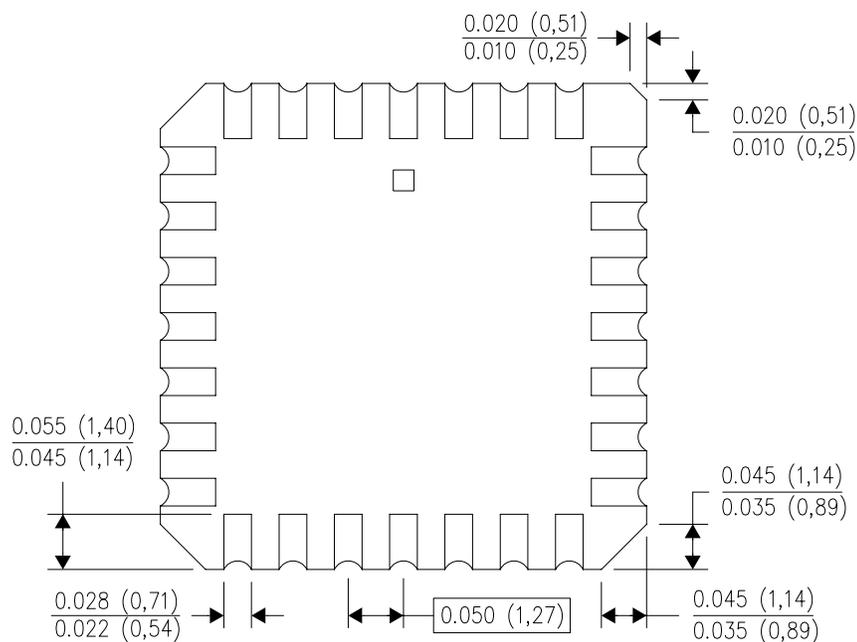
4040140/D 01/11

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   This package can be hermetically sealed with a metal lid.
         D.   Falls within JEDEC MS−004

N (R−PDIP−T**) PLASTIC DUAL−IN−LINE PACKAGE

16 PINS SHOWN

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
△C MS−001 VARIATION	AA	BB	AC	AD

A

16   9

0.260 (6,60)
0.240 (6,10)

1   8

0.070 (1,78)
0.045 (1,14) △D

0.045 (1,14)
0.030 (0,76) △D

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

14/18 Pin Only
20 Pin vendor option △D

4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
   B. This drawing is subject to change without notice.
   △C Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
   △D The 20 pin end lead shoulder width is a vendor option, either half or full width.
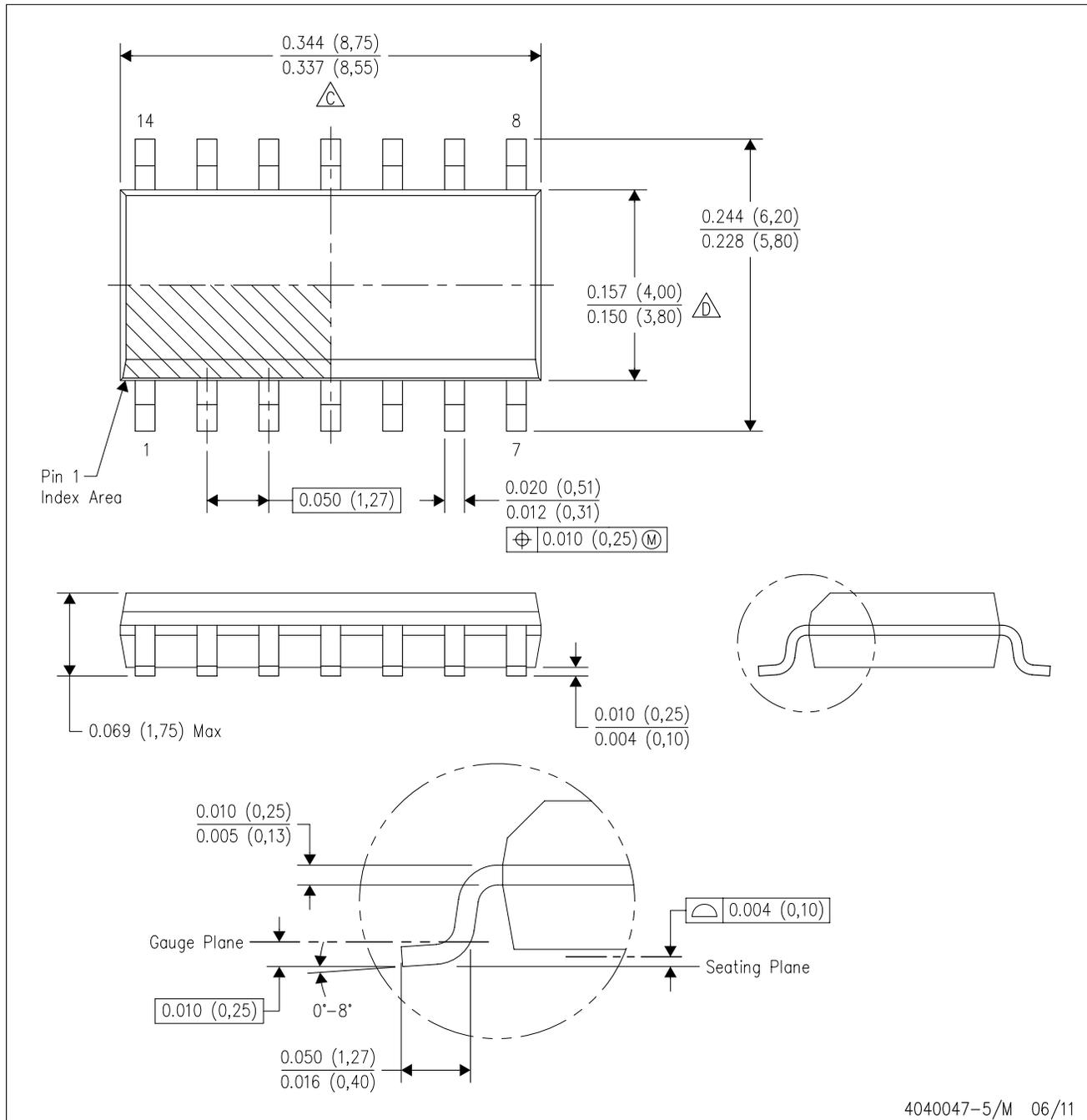
TEXAS
INSTRUMENTS
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D (R–PDSO–G14)   PLASTIC SMALL OUTLINE

0.344 (8,75)
0.337 (8,55)
C

14   8

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80) D

Pin 1
Index Area

1   7

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) M

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°–8°

0.050 (1,27)
0.016 (0,40)

4040047–5/M   06/11

NOTES: A.   All linear dimensions are in inches (millimeters).
          B.   This drawing is subject to change without notice.
          C.   Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
               not exceed 0.006 (0,15) each side.
          D.   Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
          E.   Reference JEDEC MS–012 variation AB.

TEXAS INSTRUMENTS
www.ti.com

D (R−PDSO−G14)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

|←12x1,27

5,40

Stencil Openings
(Note D)

|←14x0,55

14x1,50

|←12x1,27

5,40

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

←0,60

1,55

Example
Solder Mask Opening
(See Note E)

0.07
All Around
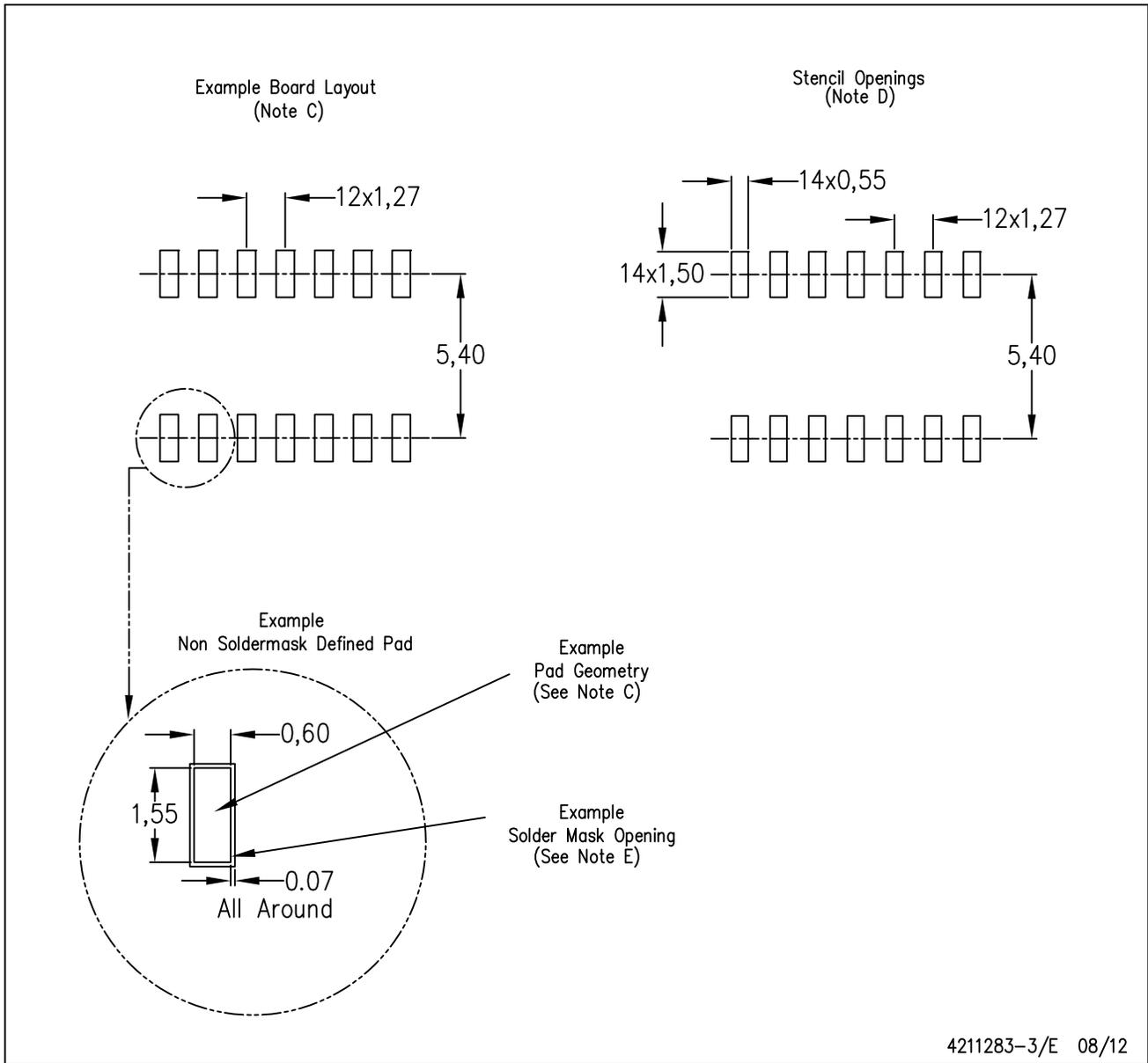
4211283−3/E 08/12

NOTES: A. All linear dimensions are in millimeters.
          B. This drawing is subject to change without notice.
          C. Publication IPC−7351 is recommended for alternate designs.
          D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
          E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

NS (R-PDSO-G**)   PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN
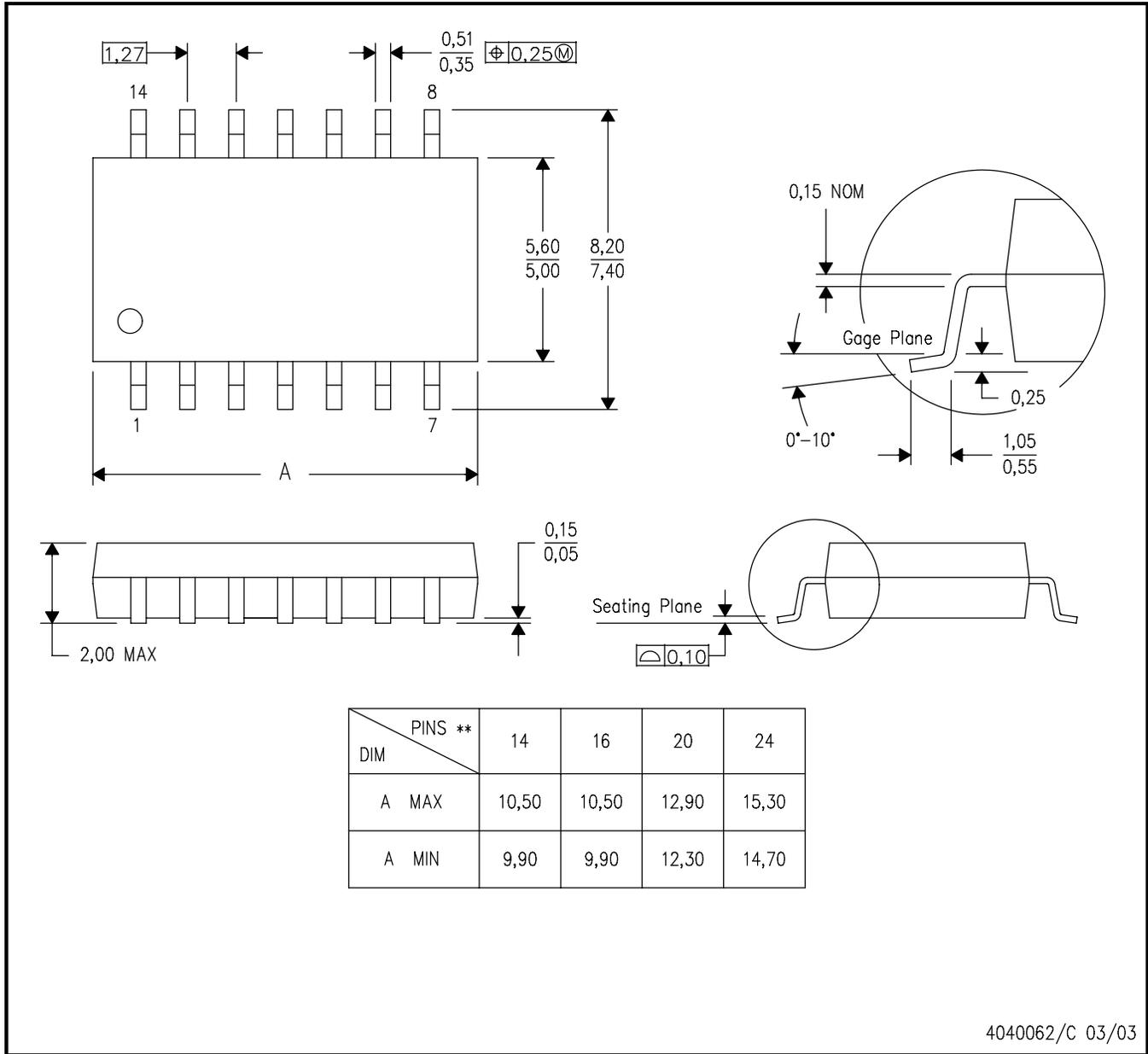
PINS ** DIM	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A.   All linear dimensions are in millimeters.
          B.   This drawing is subject to change without notice.
          C.   Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN
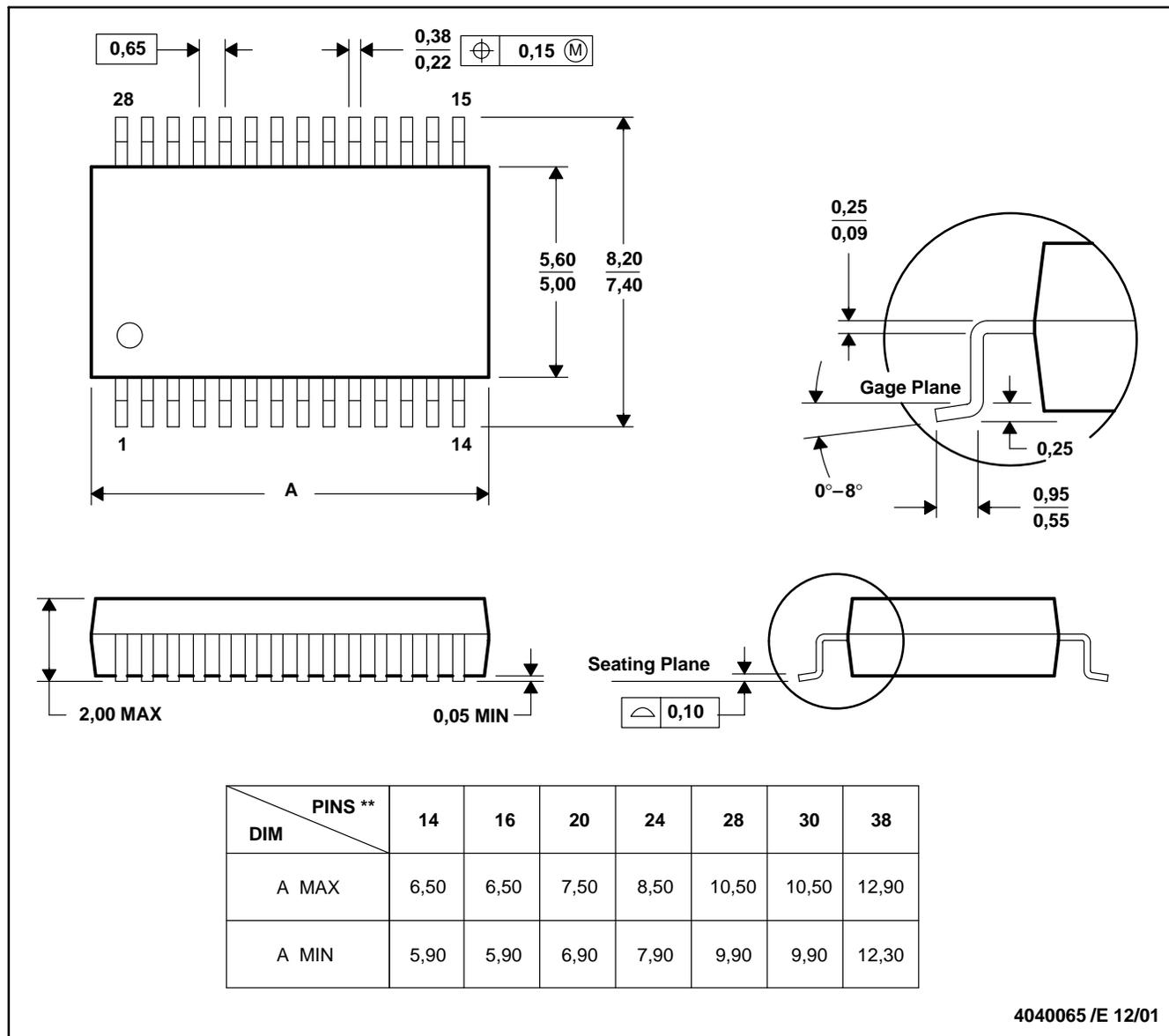
PINS ** DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
          B. This drawing is subject to change without notice.
          C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
          D. Falls within JEDEC MO-150

IMPORTANT NOTICE

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DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
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RFID	www.ti-rfid.com		
OMAP Mobile Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		