

## FEATURES

- **Controlled Baseline**
    - One Assembly/Test Site, One Fabrication Site
  - **Extended Temperature Performance of –40°C to 85°C**
  - **Enhanced Diminishing Manufacturing Sources (DMS) Support**
  - **Enhanced Product Change Notification**
  - **Qualification Pedigree <sup>(1)</sup>**
  - **Member of the Texas Instruments Widebus+™ Family**
- (1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.
- **Output Edge-Control Circuitry Minimizes Switching Noise in an Unterminated DIMM Load**
  - **Supports SSTL\_2 Data Inputs**
  - **Differential Clock (CLK and  $\overline{\text{CLK}}$ ) Inputs**
  - **Supports LVCMOS Switching Levels on the  $\overline{\text{RESET}}$  Input**
  - **$\overline{\text{RESET}}$  Input Disables Differential Input Receivers, Resets All Registers, and Forces All Outputs Low**
  - **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
  - **ESD Protection Exceeds JESD 22**
    - 2000-V Human-Body Model (A114-A)
    - 200-V Machine Model (A115-A)
    - 1000-V Charged-Device Model (C101)

## DESCRIPTION/ORDERING INFORMATION

This 26-bit registered buffer is designed for 2.3-V to 2.7-V  $V_{CC}$  operation.

All inputs are SSTL\_2, except the LVCMOS reset ( $\overline{\text{RESET}}$ ) input. All outputs are edge-controlled LVCMOS circuits optimized for unterminated DIMM loads.

The SN74SSTV32867-EP operates from a differential clock (CLK and  $\overline{\text{CLK}}$ ). Data are registered at the crossing of CLK going high and  $\overline{\text{CLK}}$  going low.

The device supports low-power standby operation. When  $\overline{\text{RESET}}$  is low, the differential input receivers are disabled, and undriven (floating) data, clock, and reference voltage ( $V_{REF}$ ) inputs are allowed. In addition, when  $\overline{\text{RESET}}$  is low, all registers are reset and all outputs are forced low. The LVCMOS  $\overline{\text{RESET}}$  always must be held at a valid logic high or low level.

To ensure defined outputs from the register before a stable clock has been supplied,  $\overline{\text{RESET}}$  must be held in the low state during power up.

## ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	LFBGA – GKE	Tape and reel	CSSTV32867SGKEREP	S867EP

- (1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

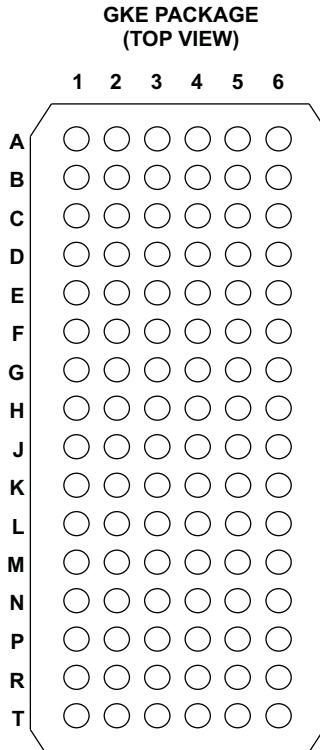


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# SN74SSTV32867-EP 26-BIT REGISTERED BUFFER WITH SSTL\_2 INPUTS AND LVCMOS OUTPUTS

SCES664-SEPTEMBER 2006



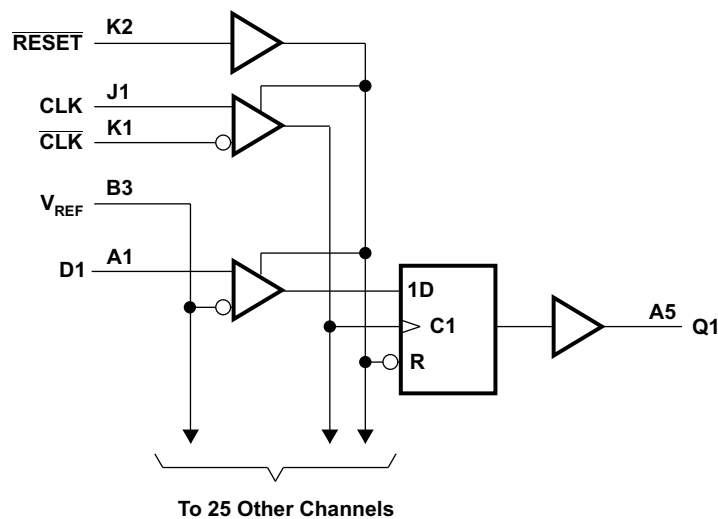
## TERMINAL ASSIGNMENTS

	1	2	3	4	5	6
A	D1	V <sub>CC</sub>	GND	V <sub>DDQ</sub>	Q1	Q2
B	D3	D2	V <sub>REF</sub>	GND	Q3	Q4
C	D5	D4	NC	GND	Q5	Q6
D	D7	D6	GND	V <sub>DDQ</sub>	Q7	Q8
E	D9	D8	V <sub>CC</sub>	GND	Q9	V <sub>DDQ</sub>
F	D11	D10	GND	V <sub>DDQ</sub>	Q10	GND
G	D13	D12	V <sub>CC</sub>	V <sub>DDQ</sub>	Q12	Q11
H	D15	D14	GND	GND	GND	Q13
J	CLK	NC	GND	GND	GND	Q14
K	$\overline{\text{CLK}}$	RESET	V <sub>CC</sub>	V <sub>DDQ</sub>	Q15	Q16
L	D16	D17	GND	V <sub>DDQ</sub>	Q17	GND
M	D18	D19	V <sub>CC</sub>	GND	Q18	V <sub>DDQ</sub>
N	D20	D21	GND	V <sub>DDQ</sub>	Q20	Q19
P	D22	D23	NC	GND	Q22	Q21
R	D24	D25	NC	GND	Q24	Q23
T	D26	V <sub>CC</sub>	GND	V <sub>DDQ</sub>	Q26	Q25

## FUNCTION TABLE

INPUTS				OUTPUT Q
$\overline{\text{RESET}}$	CLK	$\overline{\text{CLK}}$	D	
H	↑	↓	H	H
H	↑	↓	L	L
H	L or H	L or H	X	Q <sub>0</sub>
L	X or floating	X or floating	X or floating	L

## LOGIC DIAGRAM (POSITIVE LOGIC)



### Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$ or $V_{DDQ}$	Supply voltage range	-0.5	3.6	V
$V_I$	Input voltage range <sup>(2)</sup>	-0.5	$V_{CC} + 0.5$	V
$V_O$	Output voltage range <sup>(2)(3)</sup>	-0.5	$V_{DDQ} + 0.5$	V
$I_{IK}$	Input clamp current	$V_I < 0$		-50 mA
$I_{OK}$	Output clamp current	$V_O < 0$ or $V_O > V_{DDQ}$		±50 mA
$I_O$	Continuous output current	$V_O = 0$ to $V_{DDQ}$		±50 mA
	Continuous current through each $V_{CC}$ , $V_{DDQ}$ , or GND			±100 mA
$\theta_{JA}$	Package thermal impedance <sup>(4)</sup>			40 °C/W
$T_{stg}$	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) This value is limited to 3.6 V maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

### Recommended Operating Conditions<sup>(1)</sup>

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	$V_{DDQ}$		2.7	V
$V_{DDQ}$	Output supply voltage	2.3		2.7	V
$V_{REF}$	Reference voltage ( $V_{REF} = V_{DDQ}/2$ )	1.15	1.25	1.35	V
$V_{TT}$	Termination voltage	$V_{REF} - 40$ mV	$V_{REF}$	$V_{REF} + 40$ mV	V
$V_I$	Input voltage	0		$V_{CC}$	V
$V_{IH}$	AC high-level input voltage	Data input	$V_{REF} + 310$ mV		V
$V_{IL}$	AC low-level input voltage	Data input	$V_{REF} - 310$ mV		V
$V_{IH}$	DC high-level input voltage	Data input	$V_{REF} + 150$ mV		V
$V_{IL}$	DC low-level input voltage	Data input	$V_{REF} - 150$ mV		V
$V_{IH}$	High-level input voltage	RESET	1.7		V
$V_{IL}$	Low-level input voltage	RESET	0.7		V
$V_{ICR}$	Common-mode input voltage range	CLK, $\overline{CLK}$	0.97		1.53 V
$V_{I(PP)}$	Peak-to-peak input voltage	CLK, $\overline{CLK}$	360		mV
$I_{OH}$	High-level output current			-8	mA
$I_{OL}$	Low-level output current			8	mA
$T_A$	Operating free-air temperature			-40	85 °C

- (1) The RESET input of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. The differential inputs must not be floating unless RESET is low. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN74SSTV32867-EP

## 26-BIT REGISTERED BUFFER

### WITH SSTL\_2 INPUTS AND LVCMOS OUTPUTS

SCES664–SEPTEMBER 2006

## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT	
V <sub>IK</sub>		I <sub>I</sub> = -18 mA		2.3 V			-1.5	V	
V <sub>OH</sub>		I <sub>OH</sub> = -100 μA		2.3 V to 2.7 V	V <sub>DDQ</sub> - 0.2			V	
		I <sub>OH</sub> = -8 mA		2.3 V	1.7				
V <sub>OL</sub>		I <sub>OL</sub> = 100 μA		2.3 V to 2.7 V	0.2			V	
		I <sub>OL</sub> = 8 mA		2.3 V	0.45				
I <sub>I</sub>	All inputs	V <sub>I</sub> = V <sub>CC</sub> or GND		2.7 V			±5	μA	
I <sub>CC</sub>	Static standby	RESET = GND		2.7 V			40	μA	
	Static operating	RESET = V <sub>CC</sub> , V <sub>I</sub> = V <sub>IH(AC)</sub> or V <sub>IL(AC)</sub>			I <sub>O</sub> = 0			95	mA
I <sub>CCD</sub>	Dynamic operating – clock only	RESET = V <sub>CC</sub> , V <sub>I</sub> = V <sub>IH(AC)</sub> or V <sub>IL(AC)</sub> , CLK and CLK switching, 50% duty cycle		2.5 V		44		μA/MHZ	
	Dynamic operating – per each data input	RESET = V <sub>CC</sub> , V <sub>I</sub> = V <sub>IH(AC)</sub> or V <sub>IL(AC)</sub> , CLK and CLK switching, 50% duty cycle, One data input switching at one-half clock frequency, 50% duty cycle			I <sub>O</sub> = 0		5		μA/clock MHZ/ D input
C <sub>I</sub> <sup>(2)</sup>	Data inputs	V <sub>I</sub> = V <sub>REF</sub> ± 310 mV		2.5 V		3.5		pF	
	CLK, CLK	V <sub>ICR</sub> = 1.25 V, V <sub>I(PP)</sub> = 360 mV					4.5		
	RESET	V <sub>I</sub> = V <sub>CC</sub> or GND					5		

- (1) All typical values are at V<sub>CC</sub> = 2.5 V, T<sub>A</sub> = 25°C.  
(2) Measured with 50-MHz input frequency

## Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

				V <sub>CC</sub> = 2.5 ± 0.2 V			UNIT
				MIN	TYP	MAX	
f <sub>clock</sub>	Clock frequency					200	MHz
t <sub>w</sub>	Pulse duration		CLK, CLK high or low	2.5			ns
t <sub>act</sub>	Differential inputs active time <sup>(1)</sup>				22		ns
t <sub>inact</sub>	Differential inputs inactive time <sup>(2)</sup>				22		ns
t <sub>su</sub>	Setup time	Fast slew rate <sup>(3)(4)</sup>	Data before CLK↑, CLK↓	1.0			ns
		Slow slew rate <sup>(4)(5)</sup>		1.5			
t <sub>h</sub>	Hold time	Fast slew rate <sup>(3)(4)</sup>	Data after CLK↑, CLK↓	1.0			ns
		Slow slew rate <sup>(4)(5)</sup>		1.5			

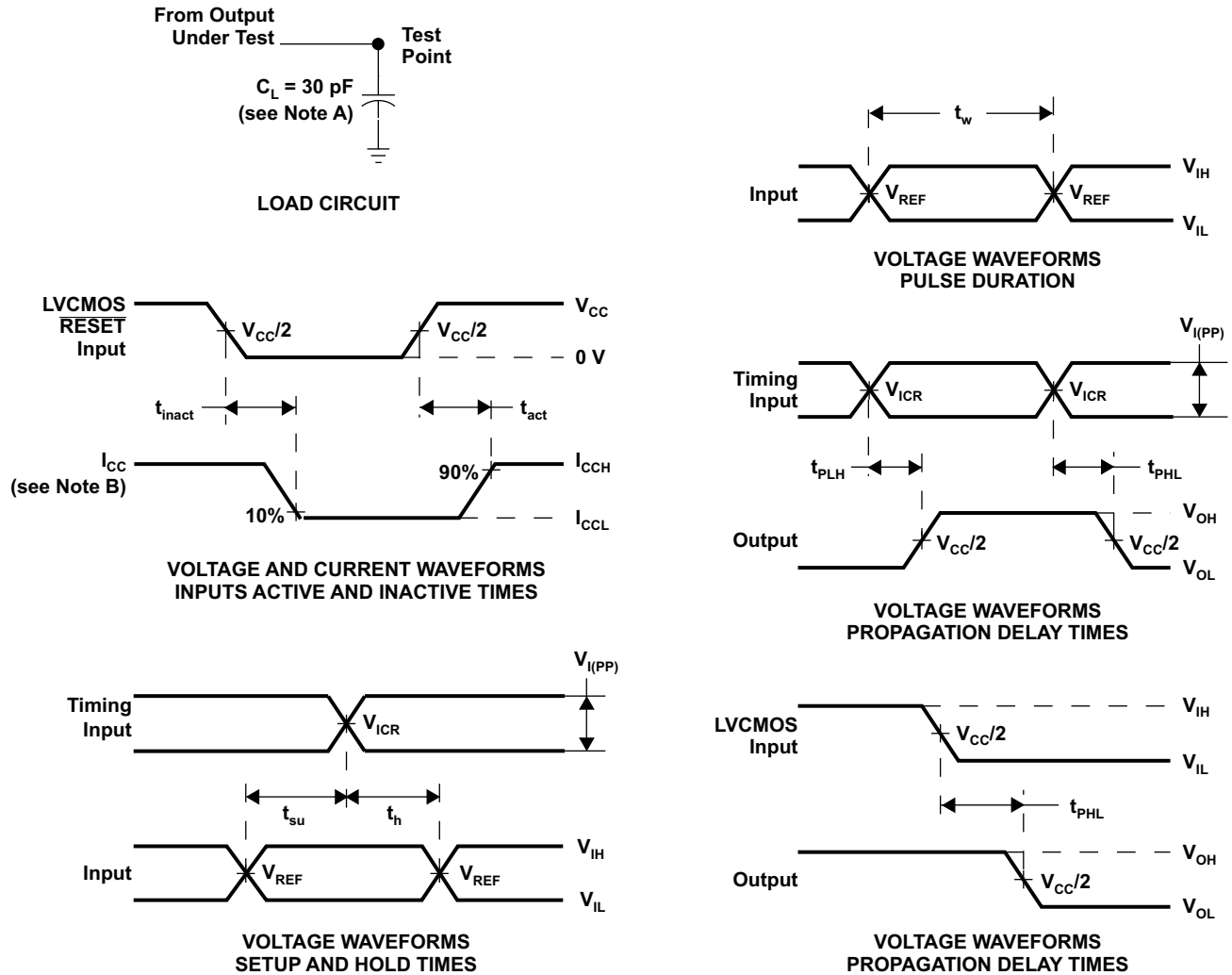
- (1) Data inputs must be low a minimum time of t<sub>act</sub> min, after RESET is taken high.  
(2) Data and clock inputs must be held at valid levels (not floating) a minimum time of t<sub>inact</sub> min, after RESET is taken low.  
(3) Data signal input slew rate ≥ 1 V/ns  
(4) CLK, CLK input slew rates are ≥ 1 V/ns.  
(5) Data signal input slew rate ≥ 0.5 V/ns and < 1 V/ns

### Switching Characteristics

over recommended operating free-air temperature range,  $V_{REF} = V_{DDQ}/2$  and  $C_L = 30$  pF (unless otherwise noted)  
 (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		UNIT
			MIN	MAX	
$f_{max}$			200		MHz
$t_{pd}$	CLK and $\overline{\text{CLK}}$	Q		5.5	ns
$t_{PHL}$	$\overline{\text{RESET}}$	Q		5.2	ns

PARAMETER MEASUREMENT INFORMATION



- A.  $C_L$  includes probe and jig capacitance.
- B.  $I_{CC}$  tested with clock and data inputs held at  $V_{CC}$  or GND, and  $I_O = 0$  mA.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ , input slew rate =  $1$  V/ns  $\pm 20\%$  (unless otherwise noted).
- D. The outputs are measured one at a time, with one transition per measurement.
- E.  $V_{REF} = V_{DDQ}/2$
- F.  $V_{IH} = V_{REF} + 310$  mV (ac voltage levels) for differential inputs.  $V_{IH} = V_{CC}$  for LVCMOS input.
- G.  $V_{IL} = V_{REF} - 310$  mV (ac voltage levels) for differential inputs.  $V_{IL} = GND$  for LVCMOS input.
- H.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
CSSTV32867SGKEREP	ACTIVE	LFBGA	GKE	96	1000	TBD	SNPB	N / A for Pkg Type
V62/06676-01XE	ACTIVE	LFBGA	GKE	96	1000	TBD	SNPB	N / A for Pkg Type

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**OTHER QUALIFIED VERSIONS OF SN74SSTV32867-EP :**

- Catalog: [SN74SSTV32867](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

**TAPE AND REEL INFORMATION**



**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSSTV32867SGKEREP	LFBGA	GKE	96	1000	330.0	24.4	5.7	13.7	2.0	8.0	24.0	Q1



**TAPE AND REEL BOX DIMENSIONS**

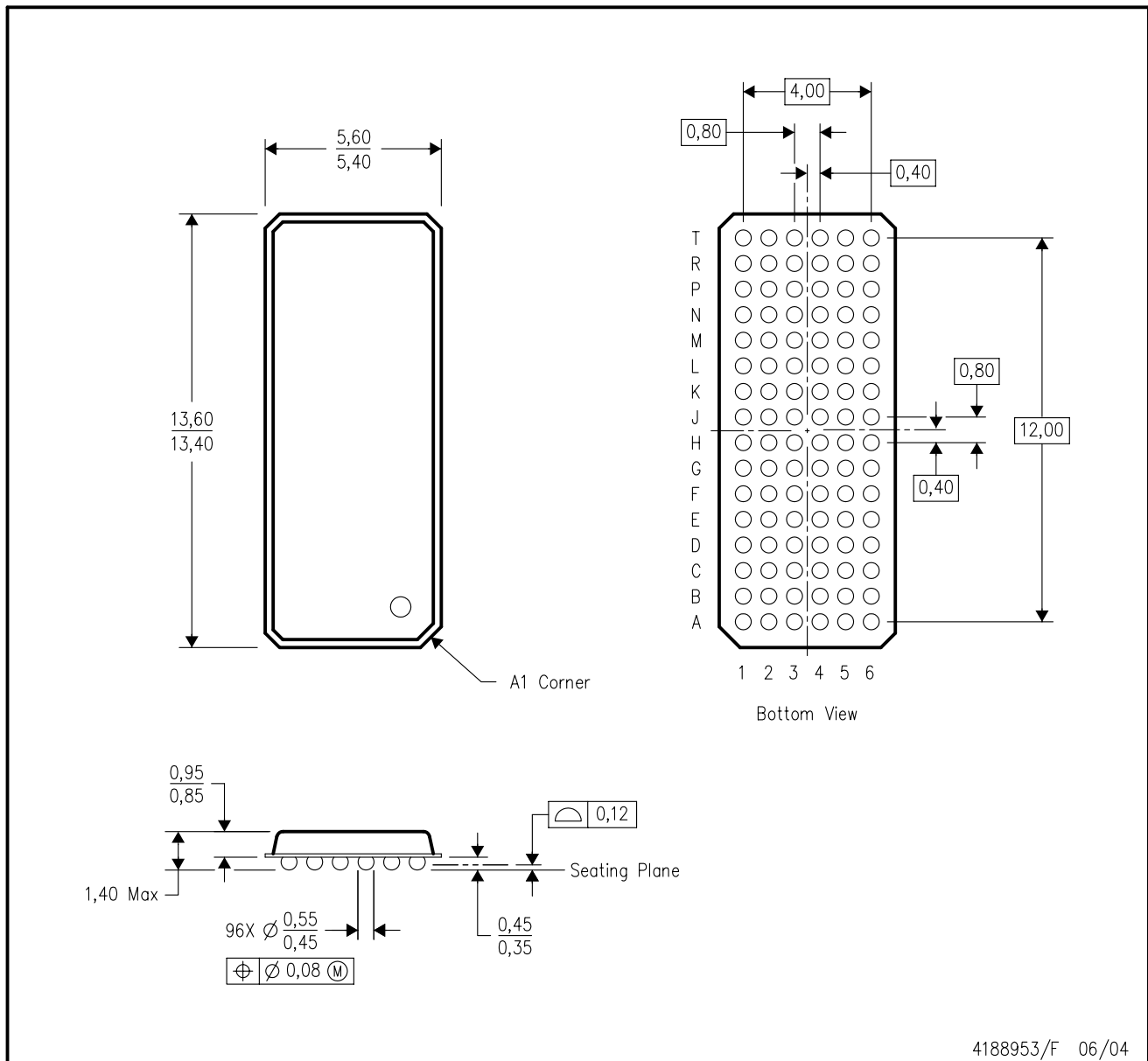


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSSTV32867SGKEREP	LFBGA	GKE	96	1000	346.0	346.0	41.0

GKE (R-PBGA-N96)

PLASTIC BALL GRID ARRAY



4188953/F 06/04

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MO-205 variation CC.
  - D. This package is tin-lead (SnPb). Refer to the 96 ZKE package (drawing 4204493) for lead-free.

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