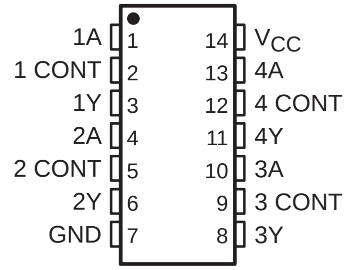
- **Meet or Exceed the Requirements of TIA/EIA-232-F and ITU Recommendation V.28**
- **Low Supply Current . . . 420 μA Typ**
- **Preset On-Chip Input Noise Filter**
- **Built-in Input Hysteresis**
- **Response and Threshold Control Inputs**
- **Push-Pull Outputs**
- **Functionally Interchangeable and Pin-to-Pin Compatible With Texas Instruments SN75189/SN75189A and Motorola MC1489/MC1489A**
- **Package Options Include Plastic Small-Outline (D) and Shrink Small-Outline (DB) Packages, and Standard Plastic (N) DIP**

D, DB, OR N PACKAGE
(TOP VIEW)



description

The SN75C189 and SN75C189A are low-power, bipolar, quadruple line receivers that are used to interface data terminal equipment (DTE) with data circuit-terminating equipment (DCE). These devices have been designed to conform to TIA/EIA-232-F.

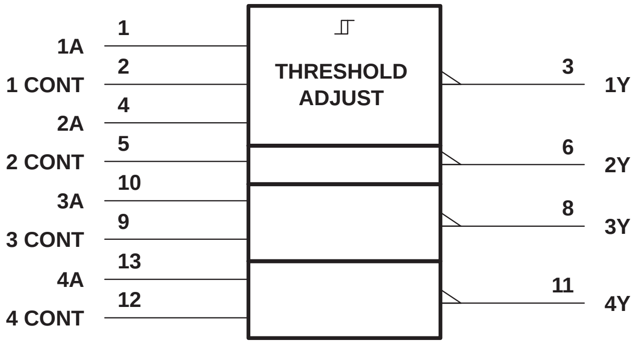
The SN75C189 has a 0.33-V typical hysteresis, compared with 0.97 V for the SN75C189A. Each receiver has provision for adjustment of the overall input threshold levels. This is achieved by choosing external series resistors and voltages to provide bias levels for the response-control pins. The output is in the high logic state if the input is open circuit or shorted to ground.

These devices have an on-chip filter that rejects input pulses of less than 1-μs duration. An external capacitor can be connected from the control pins to ground to provide further input noise filtering for each receiver.

The SN75C189 and SN75C189A have been designed using low-power techniques in a bipolar technology. In most applications, these receivers interface to single inputs of peripheral devices such as UARTs, ACEs, or microprocessors. By using sampling, such peripheral devices usually are insensitive to the transition times of the input signals. If this is not the case, or for other uses, it is recommended that the SN75C189 and SN75C189A outputs be buffered by single Schmitt input gates or single gates of the HCMOS, ALS, or 74F logic families.

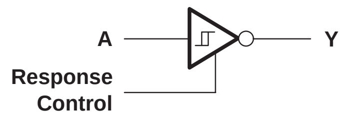
The SN75C189 and SN75C189A are characterized for operation from 0°C to 70°C.

logic symbol†



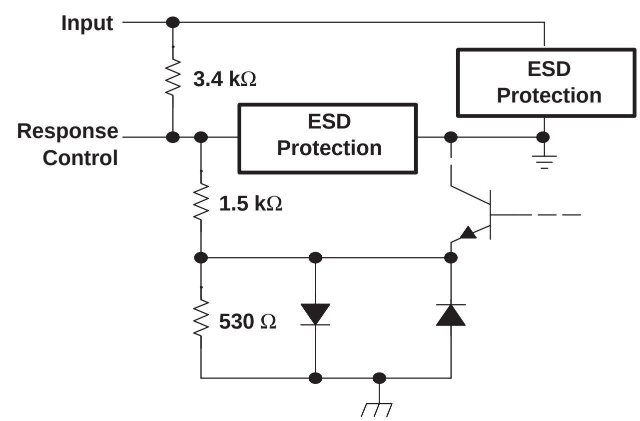
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (each receiver)



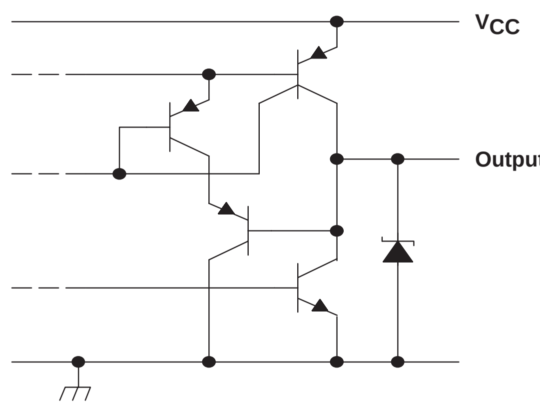
schematic of inputs and outputs

EQUIVALENT OF EACH INPUT‡



‡ All resistor values shown are nominal.

EQUIVALENT OF EACH OUTPUT



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage range, V_I	–30 V to 30 V
Output voltage range, V_O	–0.3 V to V_{CC}+ 0.3 V
Package thermal impedance, θ_{JA} (see Note 2): D package	86°C/W
DB package	96°C/W
N package	80°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, T_{stg}	–65°C to 150°C

§ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to network GND.
2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	6	V
V_I	Input voltage (see Note 3)	–25		25	V
I_{OH}	High-level output current			–3.2	mA
I_{OL}	Low-level output current			3.2	mA
	Response-control current			±1	mA
T_A	Operating free-air temperature	0		70	°C

NOTE 3: The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only, e.g., if –10 V is a maximum, the typical value is a more negative voltage.

electrical characteristics over recommended free-air temperature range, V_{CC} = 5 V ±10% (unless otherwise noted) (see Note 4)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	’C189	See Figure 1		1		1.5	V
		’C189A			1.6		2.25	
V_{IT-}	Negative-going input threshold voltage	’C189	See Figure 1		0.75		1.25	V
		’C189A			0.75	1	1.25	
V_{hys}	Input hysteresis voltage ($V_{IT+} – V_{IT–}$)	’C189	See Figure 1		0.15	0.33		V
		’C189A			0.65	0.97		
V_{OH}	High-level output voltage		V_{CC} = 4.5 V to 6 V, I_{OH} = –20 µA	V_I = 0.75 V,	3.5			V
			V_{CC} = 4.5 V to 6 V, I_{OH} = –3.2 mA	V_I = 0.75 V,	2.5			
V_{OL}	Low-level output voltage		V_{CC} = 4.5 V to 6 V, I_{OL} = 3.2 mA	V_I = 3 V,			0.4	V
I_{IH}	High-level input current		See Figure 2	V_I = 25 V	3.6		8.3	mA
				V_I = 3 V	0.43		1	
I_{IL}	Low-level input current		See Figure 2	V_I = –25 V	–3.6		–8.3	mA
				V_I = –3 V	–0.43		–1	
I_{OS}	Short-circuit output current		See Figure 3				–35	mA
I_{CC}	Supply current		V_I = 5 V, See Figure 2	No load,		420	700	µA

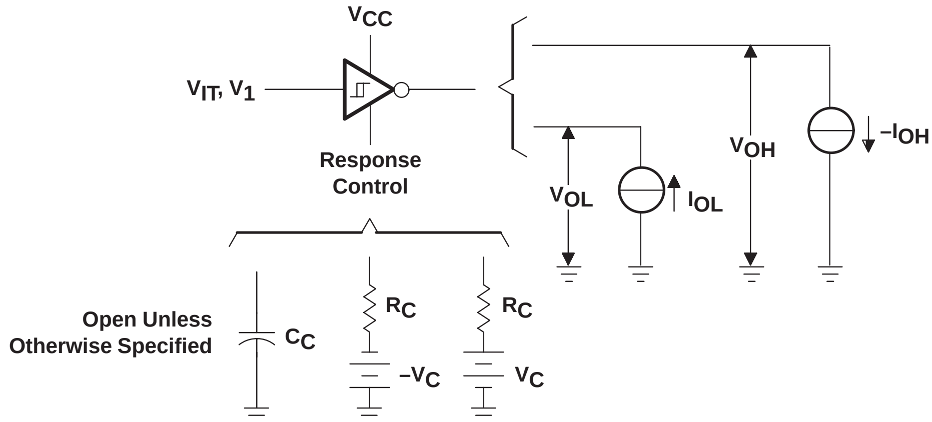
† All typical values are at T_A = 25°C.
NOTE 4: All characteristics are measured with response-control terminal open.

switching characteristics, V_{CC} = 5 V ±10%, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	R_L = 5 kΩ, C_L = 50 pF, See Figure 4			6	µs
t_{PHL}	Propagation delay time, high- to low-level output				6	µs
t_{TLH}	Transition time, low- to high-level output‡				500	ns
t_{THL}	Transition time, high- to low-level output‡				300	ns
$t_{w(N)}$	Duration of longest pulse rejected as noise§		1		6	µs

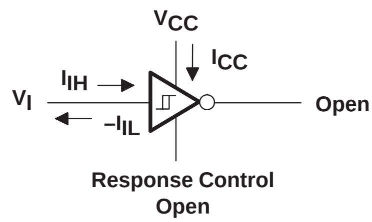
‡ Measured between 10% and 90% points of output waveform
§ The receiver ignores any positive- or negative-going pulse that is less than the minimum value of $t_{w(N)}$ and accepts any postive- or negative-going pulse greater than the maximum of $t_{w(N)}$.

PARAMETER MEASUREMENT INFORMATION



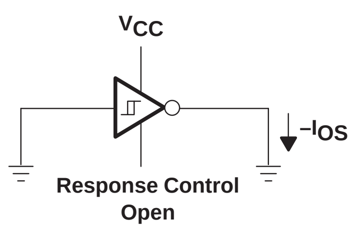
NOTE A: Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

Figure 1. V_{T+}, V_{IT-}, V_{OH}, V_{OL}



NOTE A: Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

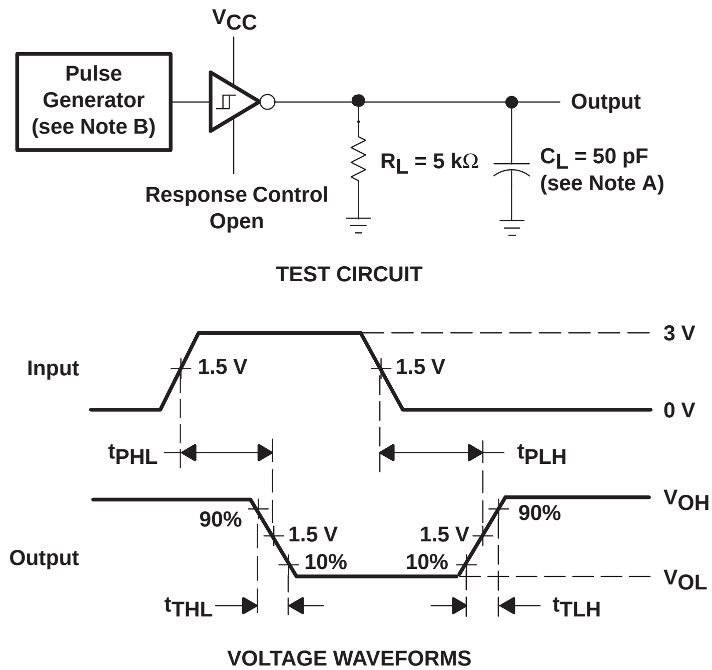
Figure 2. I_{IH}, I_{IL}, I_{CC}



NOTE A: Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

Figure 3. I_{OS}

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitances.
B. The pulse generator has the following characteristics: Z_O = 50 Ω, t_W = 25 µs.

Figure 4. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

SN75C189
INPUT THRESHOLD VOLTAGE (POSITIVE GOING)
vs
FREE-AIR TEMPERATURE

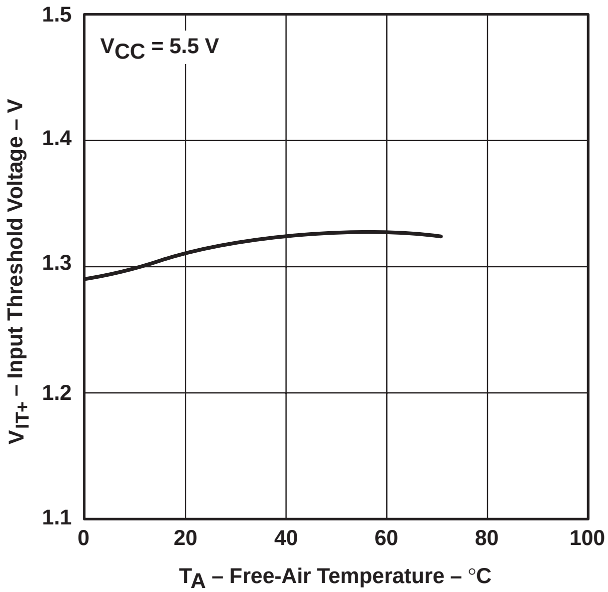


Figure 5

SN75C189A
INPUT THRESHOLD VOLTAGE (POSITIVE GOING)
vs
FREE-AIR TEMPERATURE

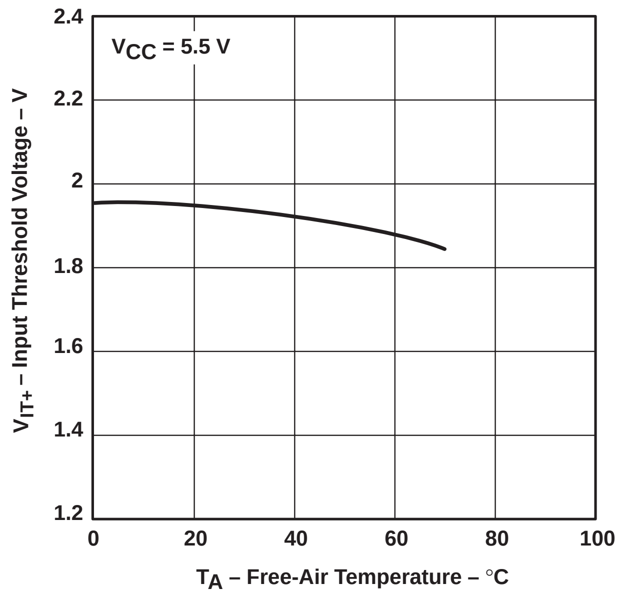


Figure 6

SN75C189
INPUT THRESHOLD VOLTAGE (NEGATIVE GOING)
vs
FREE-AIR TEMPERATURE

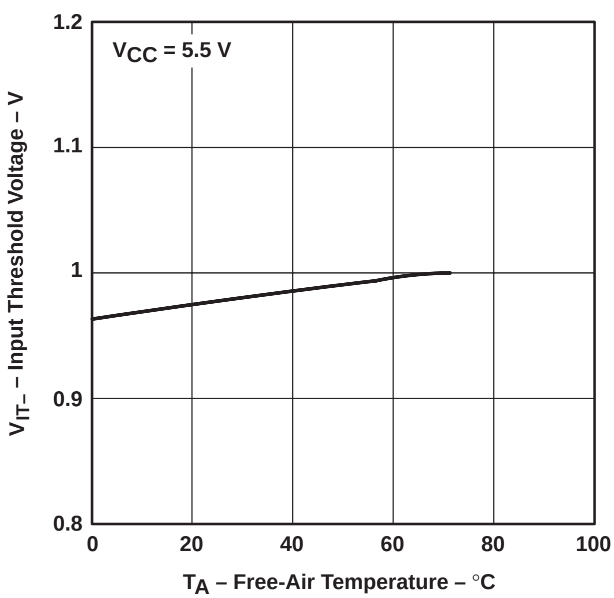


Figure 7

SN75C189A
INPUT THRESHOLD VOLTAGE (NEGATIVE GOING)
vs
FREE-AIR TEMPERATURE

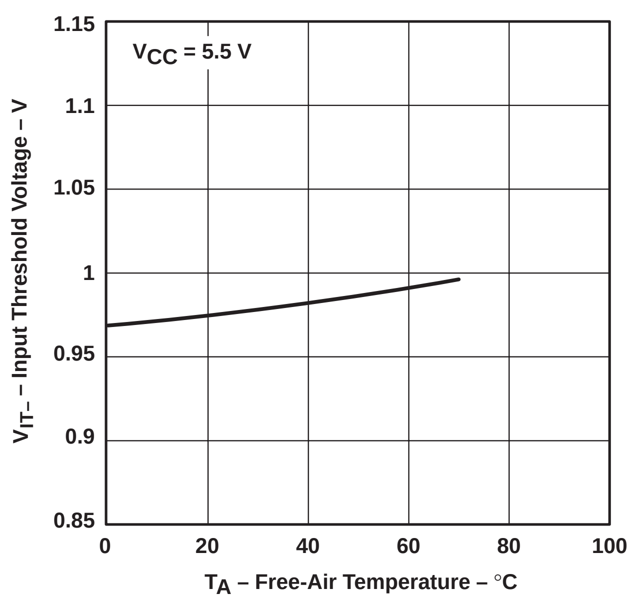


Figure 8

TYPICAL CHARACTERISTICS

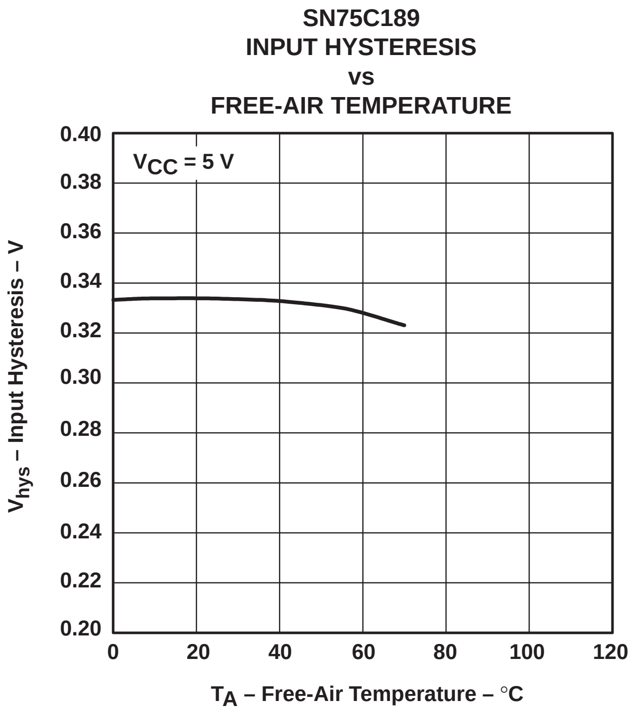


Figure 9

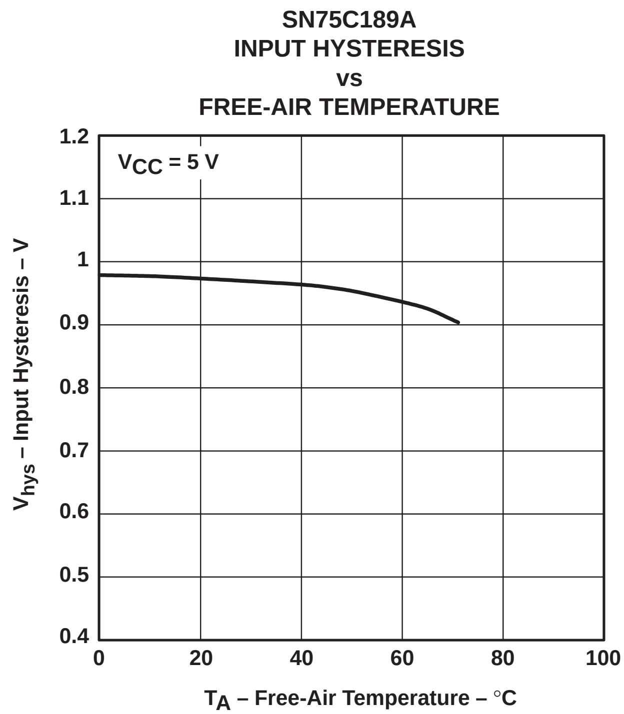


Figure 10

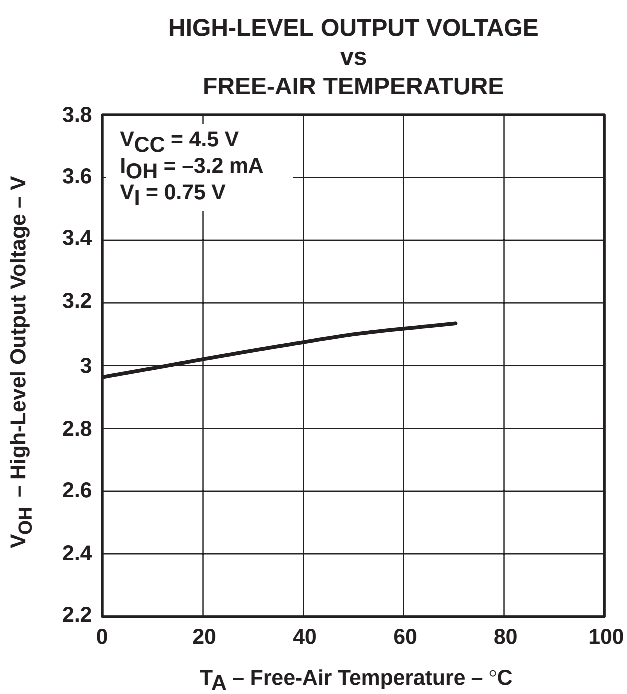


Figure 11

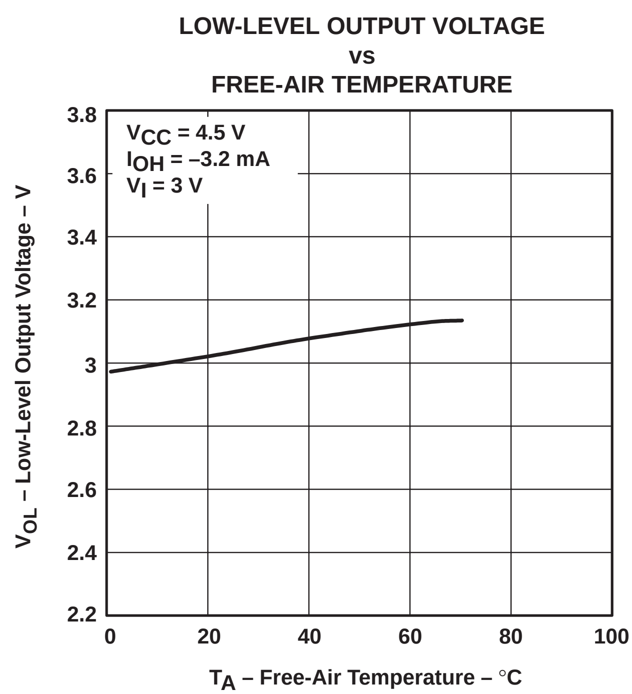


Figure 12

TYPICAL CHARACTERISTICS

SN75C189
HIGH-LEVEL INPUT CURRENT
vs
FREE-AIR TEMPERATURE

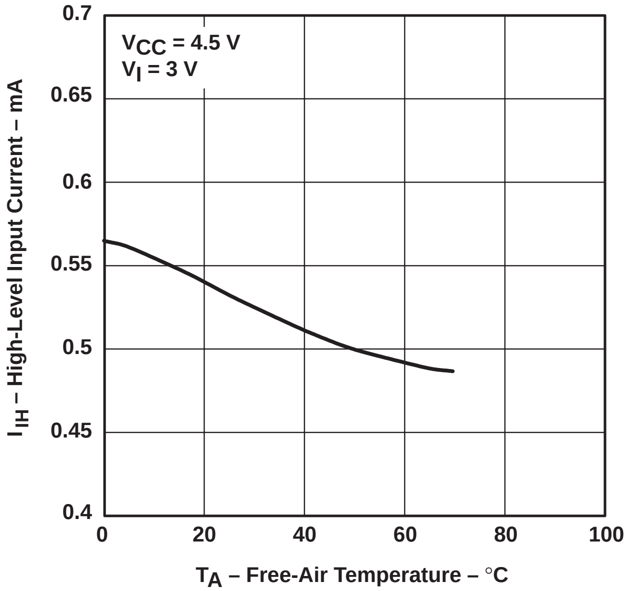


Figure 13

SN75C189A
HIGH-LEVEL INPUT CURRENT
vs
FREE-AIR TEMPERATURE

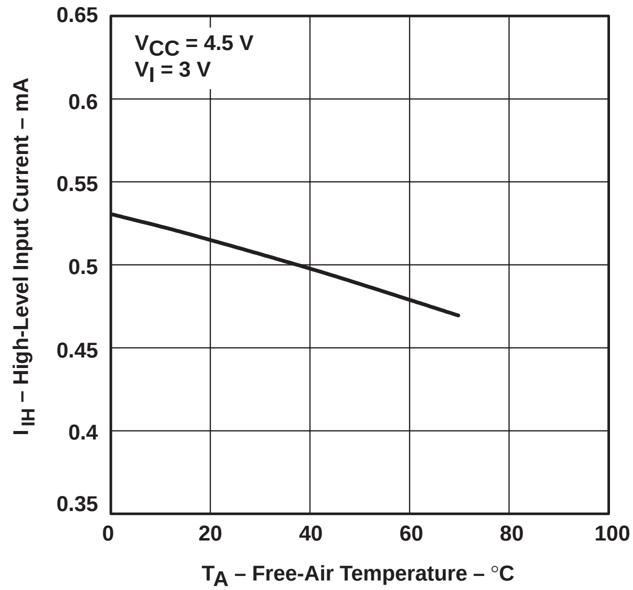


Figure 14

SN75C189
LOW-LEVEL INPUT CURRENT
vs
FREE-AIR TEMPERATURE

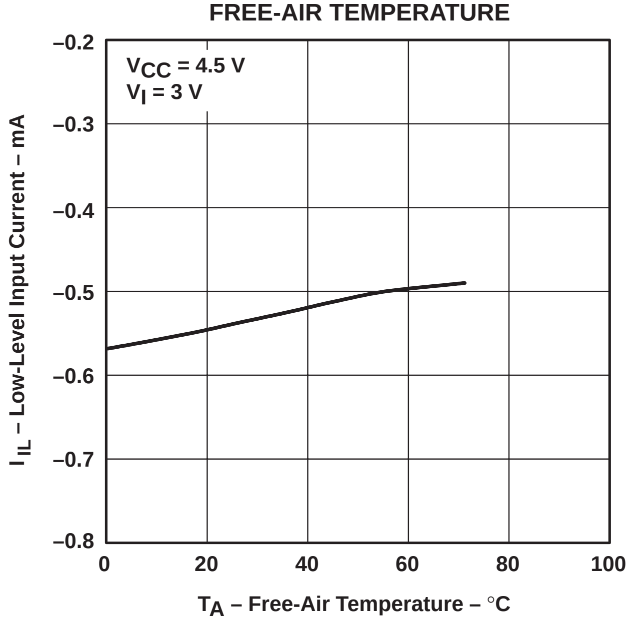


Figure 15

SN75C189A
LOW-LEVEL INPUT CURRENT
vs
FREE-AIR TEMPERATURE

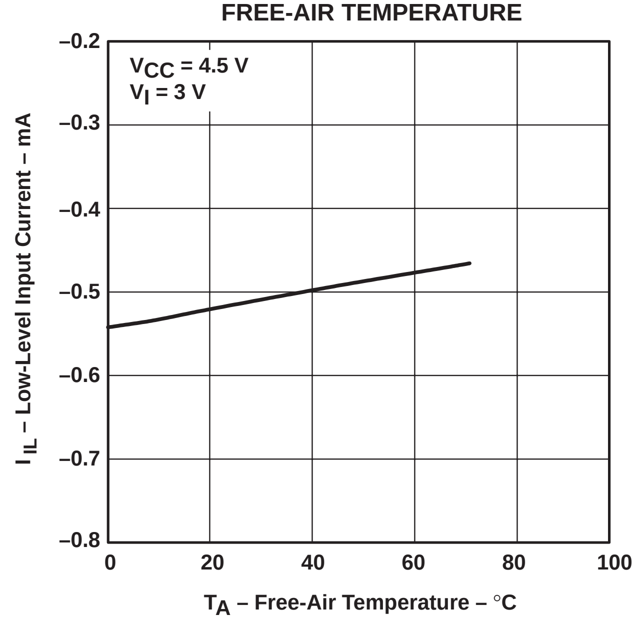


Figure 16

TYPICAL CHARACTERISTICS

HIGH-LEVEL SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

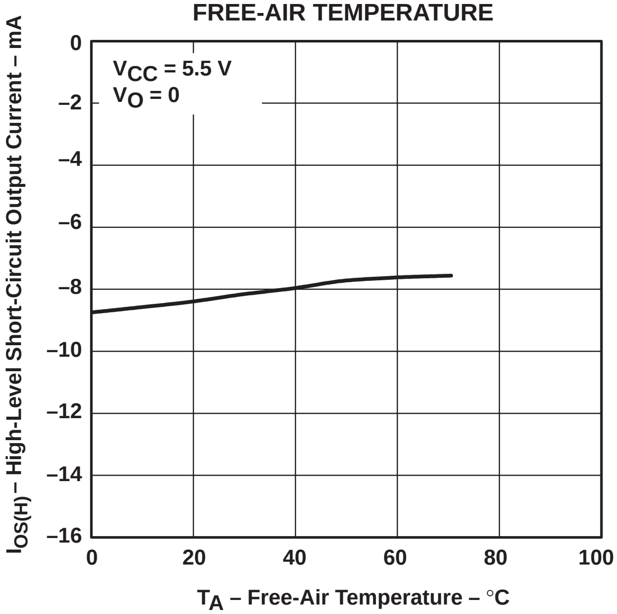


Figure 17

LOW-LEVEL SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

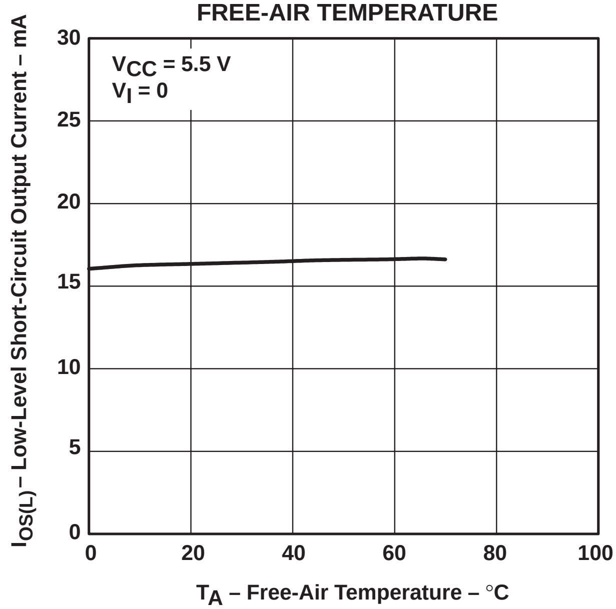


Figure 18

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

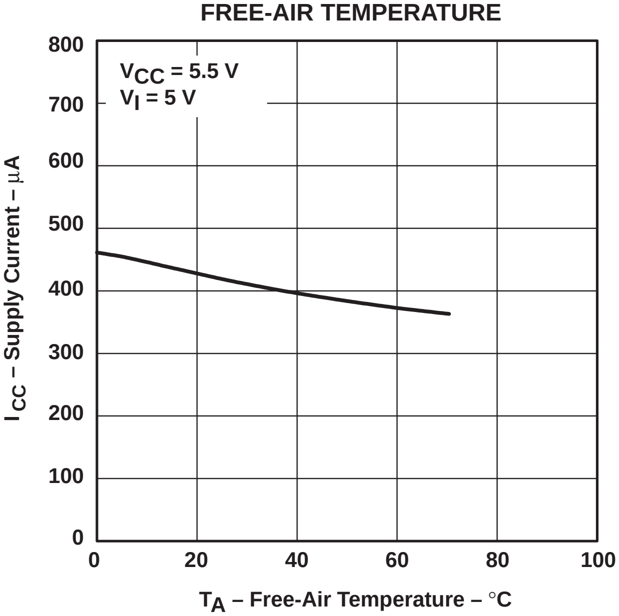


Figure 19

PROPAGATION DELAY TIME,
LOW- TO HIGH-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

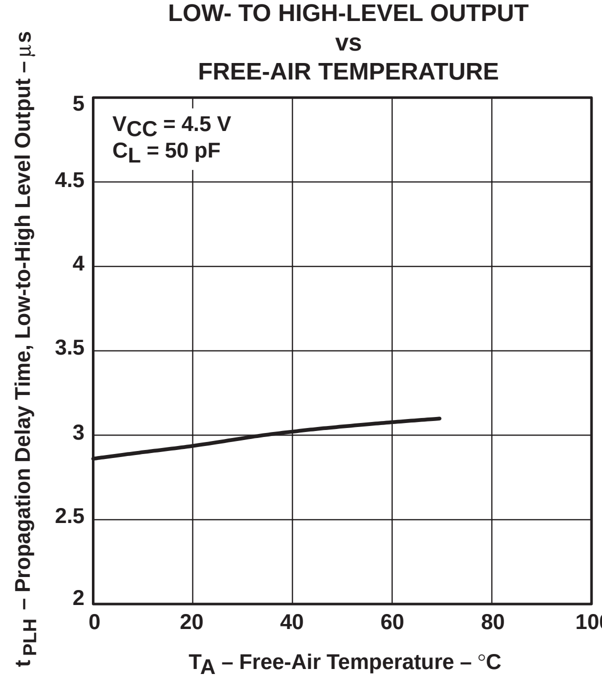


Figure 20

TYPICAL CHARACTERISTICS

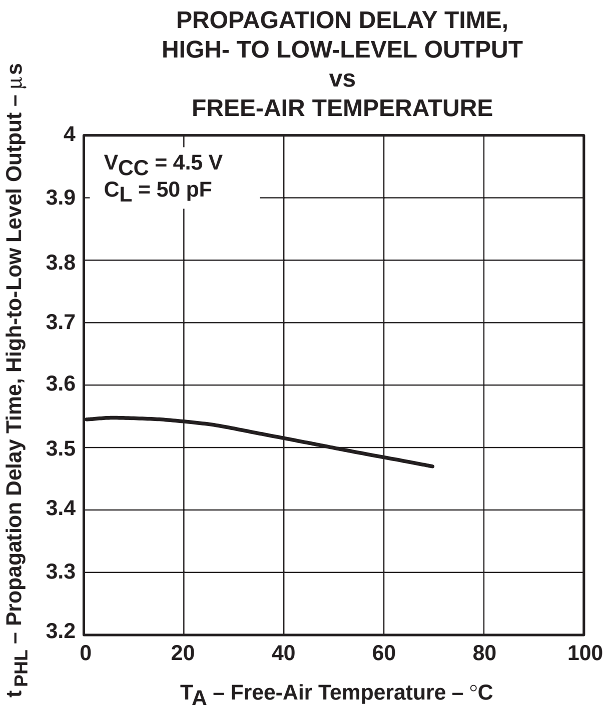


Figure 21

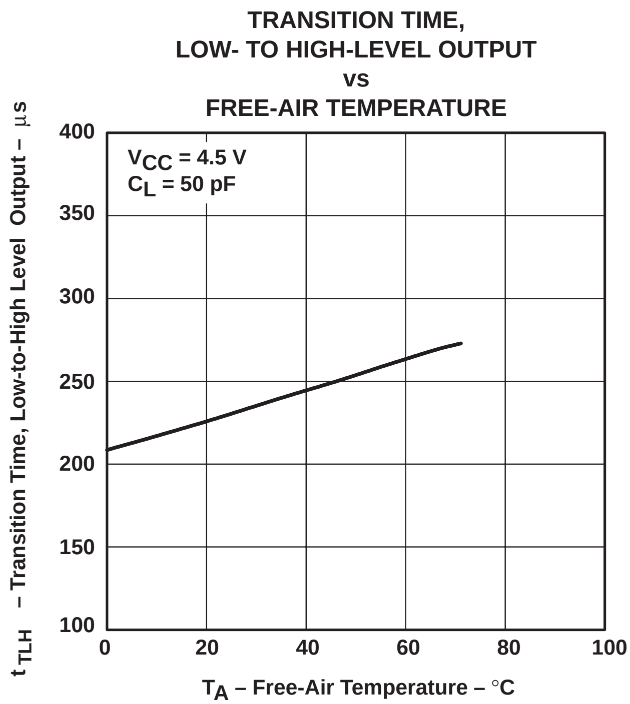


Figure 22

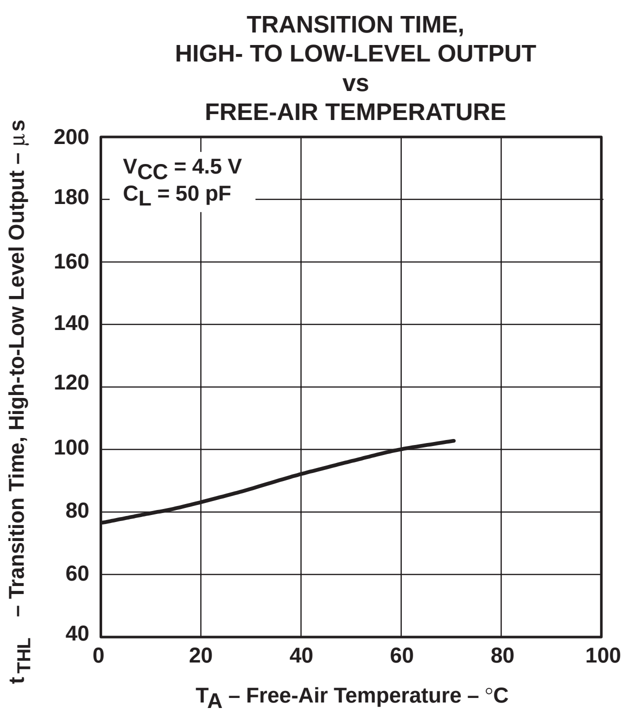


Figure 23

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