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SN65C3223E, SN75C3223E
3-V TO 5.5-V MULTICHANNEL RS-232 LINE DRIVERS/RECEIVERS
WITH ±15-kV ESD PROTECTION
SLLS727A−MAY 2006−REVISED JULY 2006

FEATURES

- **ESD Protection for RS-232 Bus Pins**
  - **±15-kV Human-Body Model (HBM)**
  - **±8-kV IEC 61000-4-2, Contact Discharge**
  - **±15-kV IEC 61000-4-2, Air-Gap Discharge**
- **Meet or Exceed the Requirements of TIA/EIA-232-F and ITU v.28 Standards**
- **Operate With 3-V to 5.5-V V_{CC} Supply**
- **Operate up to 1000 kbit/s**
- **Two Drivers and Two Receivers**
- **Low Standby Current . . . 1 μA Typ**
- **External Capacitors . . . 4 × 0.1 μF**
- **Accepts 5-V Logic Input With 3.3-V Supply**

APPLICATIONS

- **Battery-Powered Systems**
- **PDAs**
- **Notebooks**
- **Laptops**
- **Palmtop PCs**
- **Hand-Held Equipment**

DESCRIPTION/ORDERING INFORMATION

The SN65C3223E and SN75C3223E consist of two line drivers, two line receivers, and a dual charge-pump circuit with ±15-kV ESD protection pin to pin (serial-port connection pins, including GND). These devices meet the requirements of TIA/EIA-232-F and provide the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. The devices operate at typical data signaling rates up to 1000 kbit/s.

DB, DW, OR PW PACKAGE
(TOP VIEW)

EN	1	20	FORCEOFF
C1+	2	19	V_{CC}
V+	3	18	GND
C1−	4	17	DOUT1
C2+	5	16	RIN1
C2−	6	15	ROUT1
V−	7	14	FORCEON
DOUT2	8	13	DIN1
RIN2	9	12	DIN2
ROUT2	10	11	INVALID

RHL PACKAGE
(TOP VIEW)

C1+	2	23	V_{CC}
NC	3	22	NC
V+	4	21	GND
C1−	5	20	DOUT1
C2+	6	19	RIN1
C2−	7	18	ROUT1
V−	8	17	FORCEON
DOUT2	9	16	DIN1
NC	10	15	NC
RIN2	11	14	DIN2

EN 1, FORCEOFF 24, ROUT2 12, INVALID 13
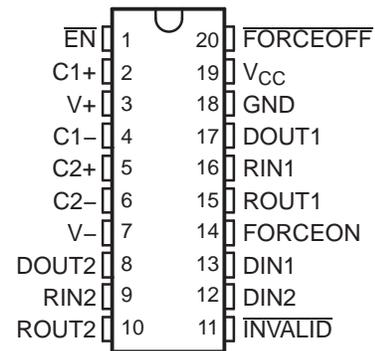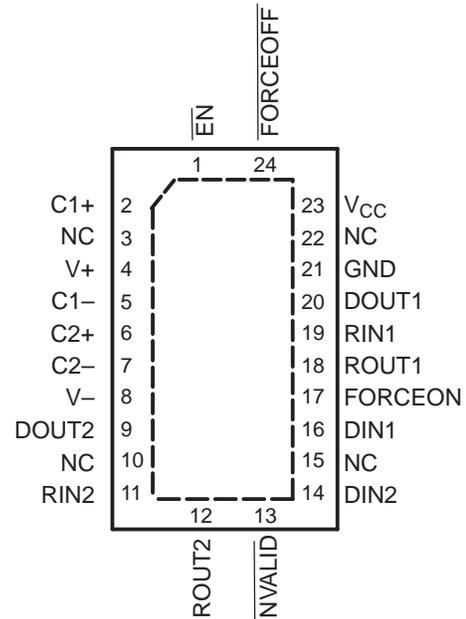
NC – No internal connection

Flexible control options for power management are available when the serial port is inactive. The auto-powerdown feature functions when FORCEON is low and FORCEOFF is high. During this mode of operation, if the devices do not sense a valid RS-232 signal, the driver outputs are disabled. If FORCEOFF is set low and EN is high, both drivers and receivers are shut off, and the supply current is reduced to 1 mA. Disconnecting the serial port or turning off the peripheral drivers causes auto-powerdown to occur. Auto-powerdown can be disabled when FORCEON and FORCEOFF are high. With auto-powerdown enabled, the devices are activated automatically when a valid signal is applied to any receiver input. The INVALID output is used to notify the user if an RS-232 signal is present at any receiver input. INVALID is high (valid data) if any receiver input voltage is greater than 2.7 V or less than –2.7 V, or has been between –0.3 V and 0.3 V for less than 30 μs. INVALID is low (invalid data) if the receiver input voltage is between –0.3 V and 0.3 V for more than 30 μs. Refer to Figure 4 for receiver input levels.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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ORDERING INFORMATION

T_A	PACKAGE[1]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	SOIC – DW	Tube of 25	SN75C3223EDW	75C3223E
		Reel of 2000	SN75C3223EDWR	
	SSOP – DB	Tube of 70	SN75C3223EDB	MY223E
		Reel of 2000	SN75C3223EDBR	
	TSSOP – PW	Tube of 70	SN75C3223EPW	MY223E
		Reel of 2000	SN75C3223EPWR	
−40°C to 85°C	SOIC – DW	Tube of 25	SN65C3223EDW	65C3223E
		Reel of 2000	SN65C3223EDWR	
	SSOP – DB	Tube of 70	SN65C3223EDB	MU223E
		Reel of 2000	SN65C3223EDBR	
	TSSOP – PW	Tube of 70	SN65C3223EPW	MU223E
		Reel of 2000	SN65C3223EPWR	

(1)   Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLES

Each Driver[1]

INPUTS				OUTPUT DOUT	DRIVER STATUS
DIN	FORCEON	FORCEOFF	VALID RIN RS-232 LEVEL		
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with auto-powerdown disabled
H	H	H	X	L	
L	L	H	Yes	H	Normal operation with auto-powerdown enabled
H	L	H	Yes	L	
L	L	H	No	Z	Powered off by auto-powerdown feature
H	L	H	No	Z	

(1)   H = high level, L = low level, X = irrelevant, Z = high impedance

Each Receiver[1]

INPUTS			OUTPUT DOUT
RIN	EN	VALID RIN RS-232 LEVEL	
L	L	X	H
H	L	X	L
X	H	X	Z
Open	L	No	H

(1)   H = high level, L = low level, X = irrelevant,
      Z = high impedance (off),
      Open = input disconnected or connected driver off

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LOGIC DIAGRAM (POSITIVE LOGIC)
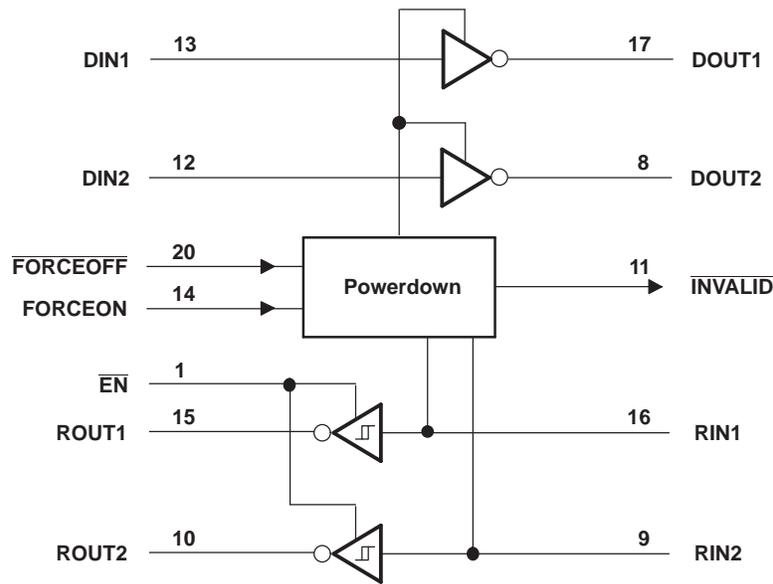
Pin numbers are for the DB, DW, and PW packages.

Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		−0.3	6	V
V+	Positive-output supply voltage range[2]		−0.3	7	V
V−	Negative-output supply voltage range[2]		0.3	−7	V
V+ − V−	Supply voltage difference[2]			13	V
V_I	Input voltage range	Driver (FORCEOFF, FORCEON, EN)	−0.3	6	V
		Receiver	−25	25	
V_O	Output voltage range	Driver	−13.2	13.2	V
		Receiver (INVALID)	−0.3	V_{CC} + 0.3	
θ_{JA}	Package thermal impedance[3][4]	DB package		70	°C/W
		DW package		58	
		PW package		83	
		RHL package		TBD	
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network GND.
(3) Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) − T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

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Recommended Operating Conditions[1]

See Figure 6

				MIN	NOM	MAX	UNIT
	Supply voltage		V_{CC} = 3.3 V	3	3.3	3.6	V
			V_{CC} = 5 V	4.5	5	5.5	
V_{IH}	Driver and control high-level input voltage	DIN, $\overline{EN}$, $\overline{FORCEOFF}$, FORCEON	V_{CC} = 3.3 V	2			V
			V_{CC} = 5 V	2.4			
V_{IL}	Driver and control low-level input voltage	DIN, $\overline{EN}$, $\overline{FORCEOFF}$, FORCEON				0.8	V
V_I	Driver and control input voltage	DIN, $\overline{EN}$, $\overline{FORCEOFF}$, FORCEON		0		5.5	V
	Receiver input voltage			−25		25	
T_A	Operating free-air temperature		SN75C3223E	0		70	°C
			SN65C3223E	−40		85	

(1)   Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

Electrical Characteristics[1]

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5)

	PARAMETER		TEST CONDITIONS	MIN	TYP[2]	MAX	UNIT
I_I	Input leakage current	$\overline{EN}$, $\overline{FORCEOFF}$, FORCEON			±0.01	±1	μA
I_{CC}	Supply current	Auto-powerdown disabled	V_{CC} = 3.3 V or 5 V, T_A = 25°C, No load, $\overline{FORCEOFF}$ and FORCEON at V_{CC}		0.3	1	mA
		Powered off	No load, $\overline{FORCEOFF}$ at GND		1	10	μA
		Auto-powerdown enabled	No load, $\overline{FORCEOFF}$ at V_{CC}, FORCEON at GND, All RIN are open or grounded		1	10	

(1)   Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.
(2)   All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

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DRIVER SECTION

Electrical Characteristics[1]

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5)

	PARAMETER	TEST CONDITIONS	MIN	TYP[2]	MAX	UNIT
V_{OH}	High-level output voltage	DOUT at R_L = 3 kΩ to GND	5	5.4		V
V_{OL}	Low-level output voltage	DOUT at R_L = 3 kΩ to GND	−5	−5.4		V
I_{IH}	High-level input current	V_I = V_{CC}		±0.01	±1	µA
I_{IL}	Low-level input current	V_I at GND		±0.01	±1	µA
I_{OS}	Short-circuit output current[3]	V_{CC} = 3.6 V, V_O = 0 V		±35	±60	mA
		V_{CC} = 5.5 V, V_O = 0 V				
r_o	Output resistance	V_{CC}, V+, and V− = 0 V, V_O = ±2 V	300	10M		Ω
I_{OZ}	Output leakage current	$\overline{FORCEOFF}$ = GND, V_{CC} = 3 V to 3.6 V, V_O = ±12 V			±25	µA
		$\overline{FORCEOFF}$ = GND, V_{CC} = 4.5 V to 5.5 V, V_O = ±12 V			±25	

(1)   Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(2)   All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(3)   Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

Switching Characteristics[1]

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5)

	PARAMETER	TEST CONDITIONS			MIN	TYP[2]	MAX	UNIT
	Maximum data rate (see Figure 1)	R_L = 3 kΩ, One DOUT switching	C_L = 1000 pF		250			kbit/s
			C_L = 250 pF,	V_{CC} = 3 V to 4.5 V	1000			
			C_L = 1000 pF,	V_{CC} = 4.5 V to 5.5 V	1000			
$t_{sk(p)}$	Pulse skew[3]	C_L = 150 pF to 2500 pF,	R_L = 3 kΩ to 7 kΩ,	See Figure 2		300		ns
SR(tr)	Slew rate, transition region (see Figure 1)	R_L = 7 kΩ,	C_L = 150 pF to 1000 pF		8		90	V/µs
		R_L = 3 kΩ	C_L = 1000 pF		12		60	
			C_L = 150 pF to 250 pF		24		150	

(1)   Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(2)   All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(3)   Pulse skew is defined as |t_{PLH} − t_{PHL}| of each channel of the same device.

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RECEIVER SECTION

Electrical Characteristics[1]

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 6)

PARAMETER		TEST CONDITIONS	MIN	TYP[2]	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -1$ mA	$V_{CC} - 0.6$	$V_{CC} - 0.1$		V
V_{OL}	Low-level output voltage	$I_{OL} = 1.6$ mA			0.4	V
V_{IT+}	Positive-going input threshold voltage	$V_{CC} = 3.3$ V		1.6	2.4	V
		$V_{CC} = 5$ V		1.9	2.4	
V_{IT-}	Negative-going input threshold voltage	$V_{CC} = 3.3$ V	0.6	1.1		V
		$V_{CC} = 5$ V	0.6	1.4		
V_{hys}	Input hysteresis ($V_{IT+} - V_{IT-}$)			0.5		V
I_{OZ}	Output leakage current	$\overline{EN} = V_{CC}$		±0.05		µA
r_i	Input resistance	$V_I = \pm3$ V to ±25 V	3	5		kΩ

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

Switching Characteristics[1]

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP[2]	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 150 pF, See Figure 3	150	ns
t_{PHL}	Propagation delay time, high- to low-level output	C_L = 150 pF, See Figure 3	150	ns
t_{en}	Output enable time	C_L = 150 pF, R_L = 3 kΩ, See Figure 4	200	ns
t_{dis}	Output disable time	C_L = 150 pF, R_L = 3 kΩ, See Figure 4	200	ns
$t_{sk(p)}$	Pulse skew[3]	See Figure 3	50	ns

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(3) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

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AUTO-POWERDOWN SECTION

Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5)

| PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
$V_{T+(valid)}$	Receiver input threshold for $\overline{INVALID}$ high-level output voltage	FORCEON = GND,	$\overline{FORCEOFF}$ = V_{CC}		2.7	V
$V_{T(valid)}$	Receiver input threshold for $\overline{INVALID}$ high-level output voltage	FORCEON = GND,	$\overline{FORCEOFF}$ = V_{CC}	−2.7		V
$V_{T(invalid)}$	Receiver input threshold for $\overline{INVALID}$ low-level output voltage	FORCEON = GND,	$\overline{FORCEOFF}$ = V_{CC}	−0.3	0.3	V
V_{OH}	$\overline{INVALID}$ high-level output voltage	I_{OH} = 1 mA, $\overline{FORCEOFF}$ = V_{CC}	FORCEON = GND,	V_{CC} – 0.6		V
V_{OL}	$\overline{INVALID}$ low-level output voltage	I_{OL} = 1.6 mA, $\overline{FORCEOFF}$ = V_{CC}	FORCEON = GND,		0.4	V

Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5)

PARAMETER		TYP[1]	UNIT
t_{valid}	Propagation delay time, low- to high-level output	1	μs
$t_{invalid}$	Propagation delay time, high- to low-level output	30	μs
t_{en}	Supply enable time	100	μs

(1)   All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
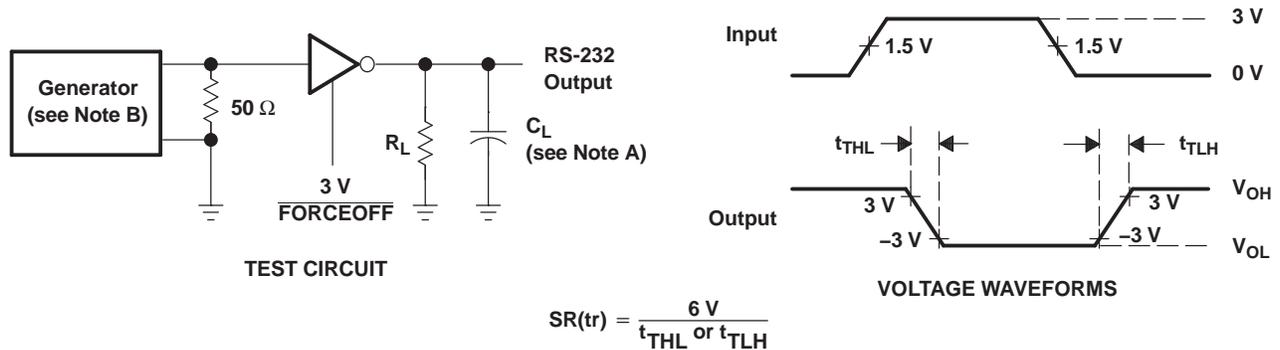
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PARAMETER MEASUREMENT INFORMATION

$$SR(tr) = \frac{6\ V}{t_{THL}\ \text{or}\ t_{TLH}}$$

A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω, 50% duty cycle, $t_r \leq$ 10 ns, $t_f \leq$ 10 ns.

Figure 1. Driver Slew Rate
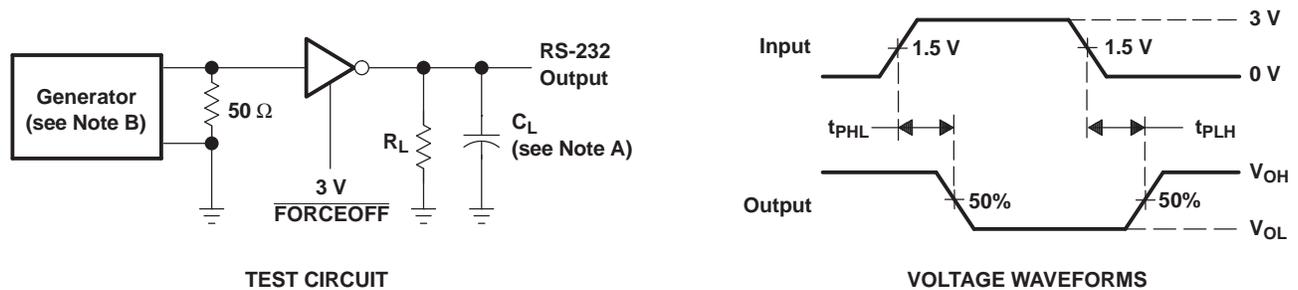
A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω, 50% duty cycle, $t_r \leq$ 10 ns, $t_f \leq$ 10 ns.

Figure 2. Driver Pulse Skew
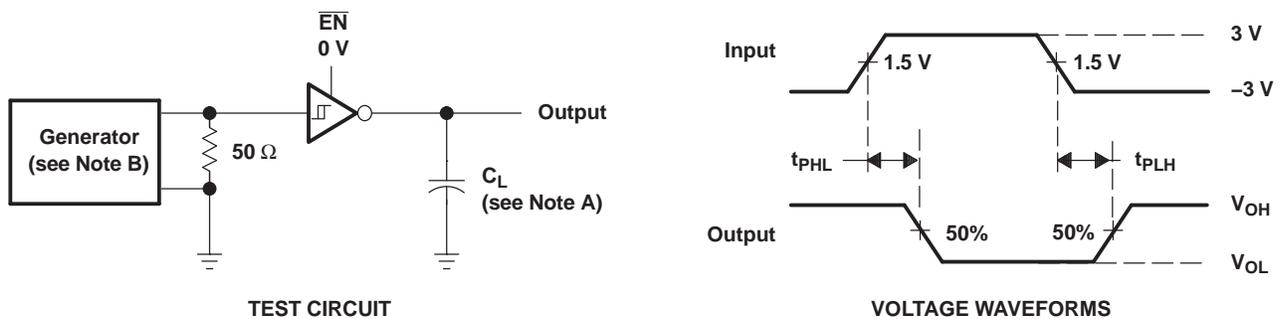
A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, $t_r \leq$ 10 ns, $t_f \leq$ 10 ns.

Figure 3. Receiver Propagation Delay Times
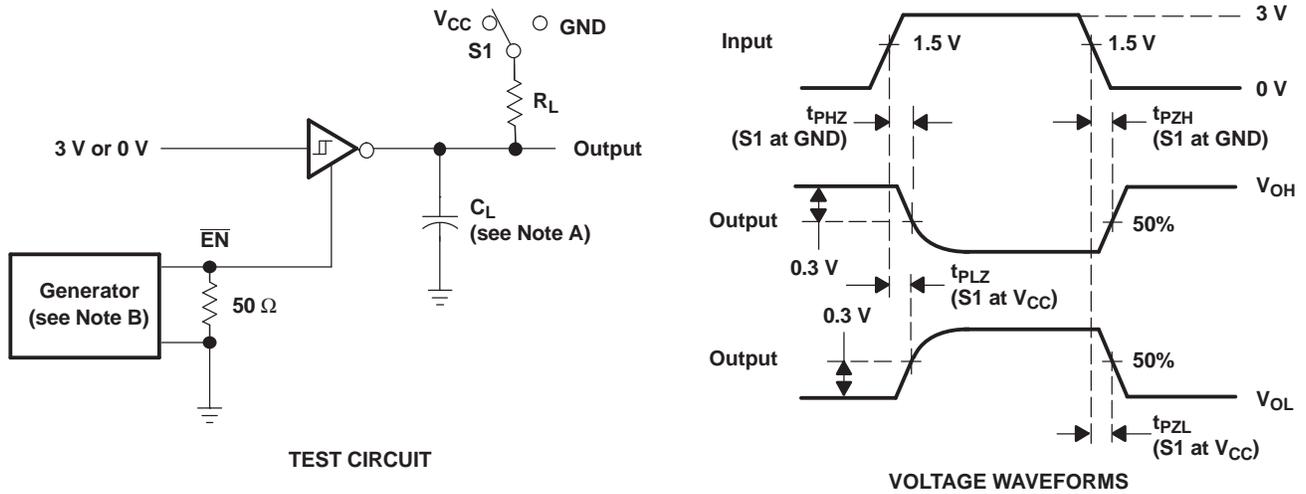
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PARAMETER MEASUREMENT INFORMATION (continued)


A. C_L includes probe and jig capacitance.

B.   The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

Figure 4. Receiver Enable and Disable Times

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PARAMETER MEASUREMENT INFORMATION (continued)

TEST CIRCUIT

VOLTAGE WAVEFORMS
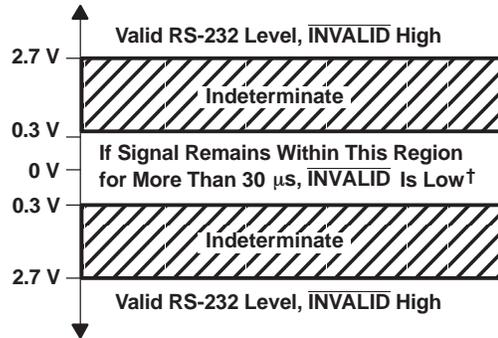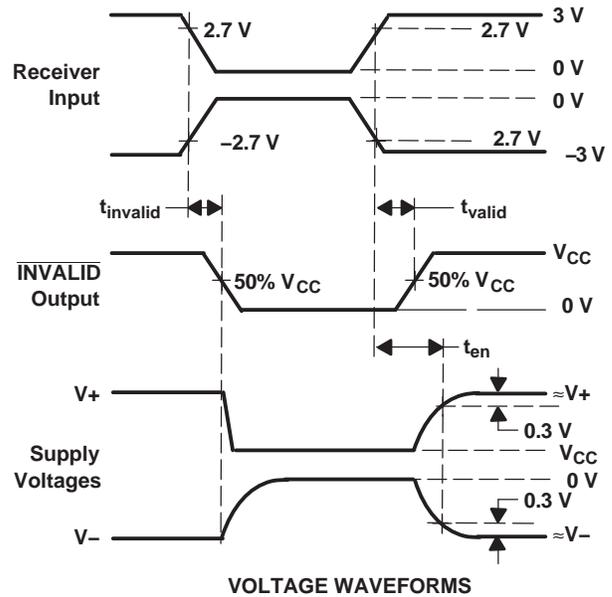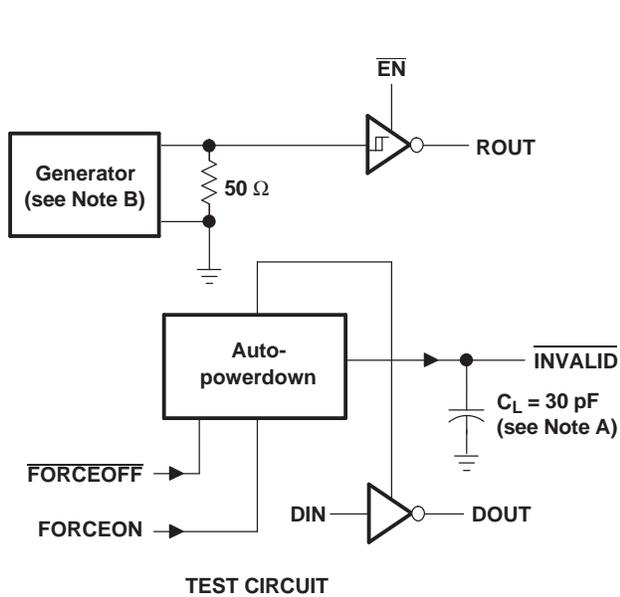
† Auto-powerdown disables drivers and reduces supply current to 1 μA

A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω, 50% duty cycle, $t_r \leq$ 10 ns, $t_f \leq$ 10 ns.

Figure 5. INVALID Propagation Delay Times and Supply Enabling Time

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APPLICATION INFORMATION
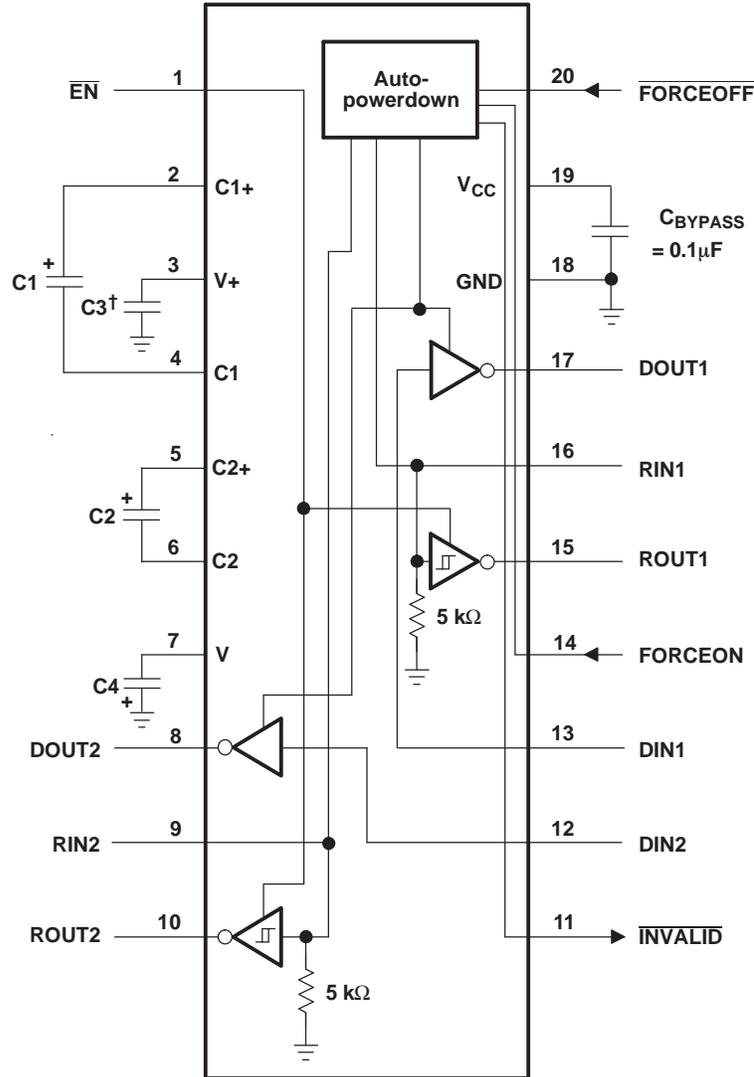
† C3 can be connected to V_{CC} or GND.

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

V_{CC} vs CAPACITOR VALUES

V_{CC}	C1	C2, C3, and C4
3.3 V ± 0.3 V	0.1 μF	0.1 μF
5 V ± 0.5 V	0.047 μF	0.33 μF
3 V to 5.5 V	0.1 μF	0.47 μF

Figure 6. Typical Operating Circuit and Capacitor Values

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SN65C3223EDB	ACTIVE	SSOP	DB	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65C3223EDBG4	ACTIVE	SSOP	DB	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65C3223EDBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65C3223EDBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65C3223EDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65C3223EDWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65C3223EDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65C3223EDWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65C3223EPW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65C3223EPWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65C3223EPWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65C3223EPWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C3223EDB	ACTIVE	SSOP	DB	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C3223EDBG4	ACTIVE	SSOP	DB	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C3223EDBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C3223EDBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C3223EDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C3223EDWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C3223EDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C3223EDWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C3223EPW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C3223EPWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C3223EPWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75C3223EPWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS
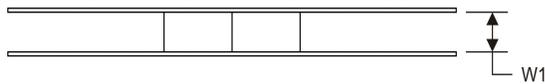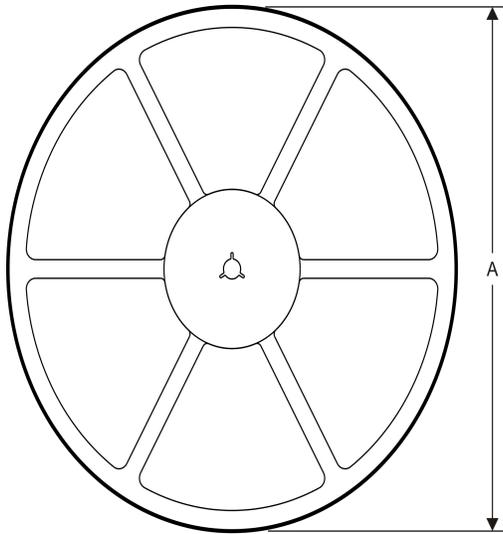
TAPE DIMENSIONS
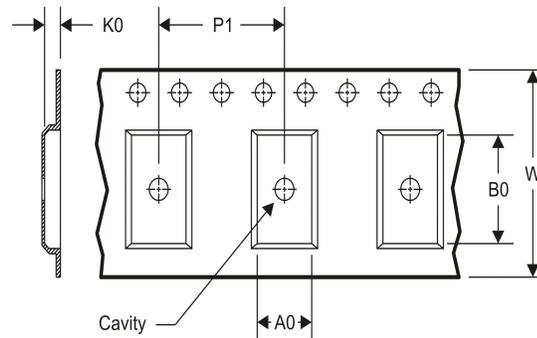
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65C3223EDBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN65C3223EDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN65C3223EPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN75C3223EDBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN75C3223EDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN75C3223EPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS
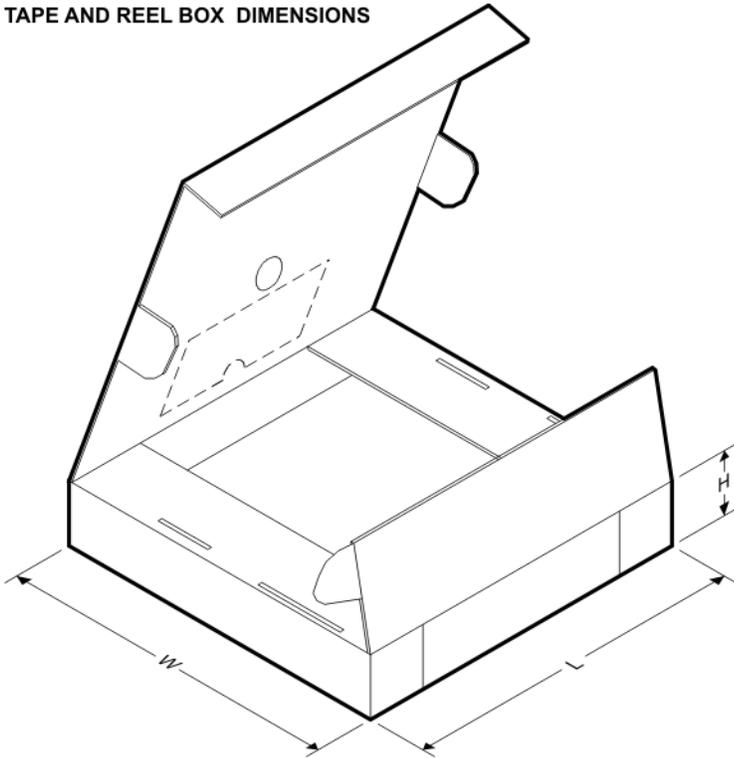
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65C3223EDBR	SSOP	DB	20	2000	367.0	367.0	38.0
SN65C3223EDWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN65C3223EPWR	TSSOP	PW	20	2000	367.0	367.0	38.0
SN75C3223EDBR	SSOP	DB	20	2000	367.0	367.0	38.0
SN75C3223EDWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN75C3223EPWR	TSSOP	PW	20	2000	367.0	367.0	38.0

DW (R−PDSO−G20)   PLASTIC SMALL OUTLINE

0.512 (13,00) / 0.496 (12,60)
0.419 (10,63) / 0.393 (9,97)
0.299 (7,60) / 0.291 (7,40)
0.050 (1,27)
0.020 (0,51) / 0.012 (0,31)
⊕ 0.010 (0,25) Ⓜ
Pin 1 Index Area
0.104 (2,65) Max
0.012 (0,30) / 0.004 (0,10)
0.013 (0,33) / 0.008 (0,20)
0.004 (0,10)
Gauge Plane
Seating Plane
0.010 (0,25)
0°−8°
0.050 (1,27) / 0.016 (0,40)

4040000−4/G 01/11
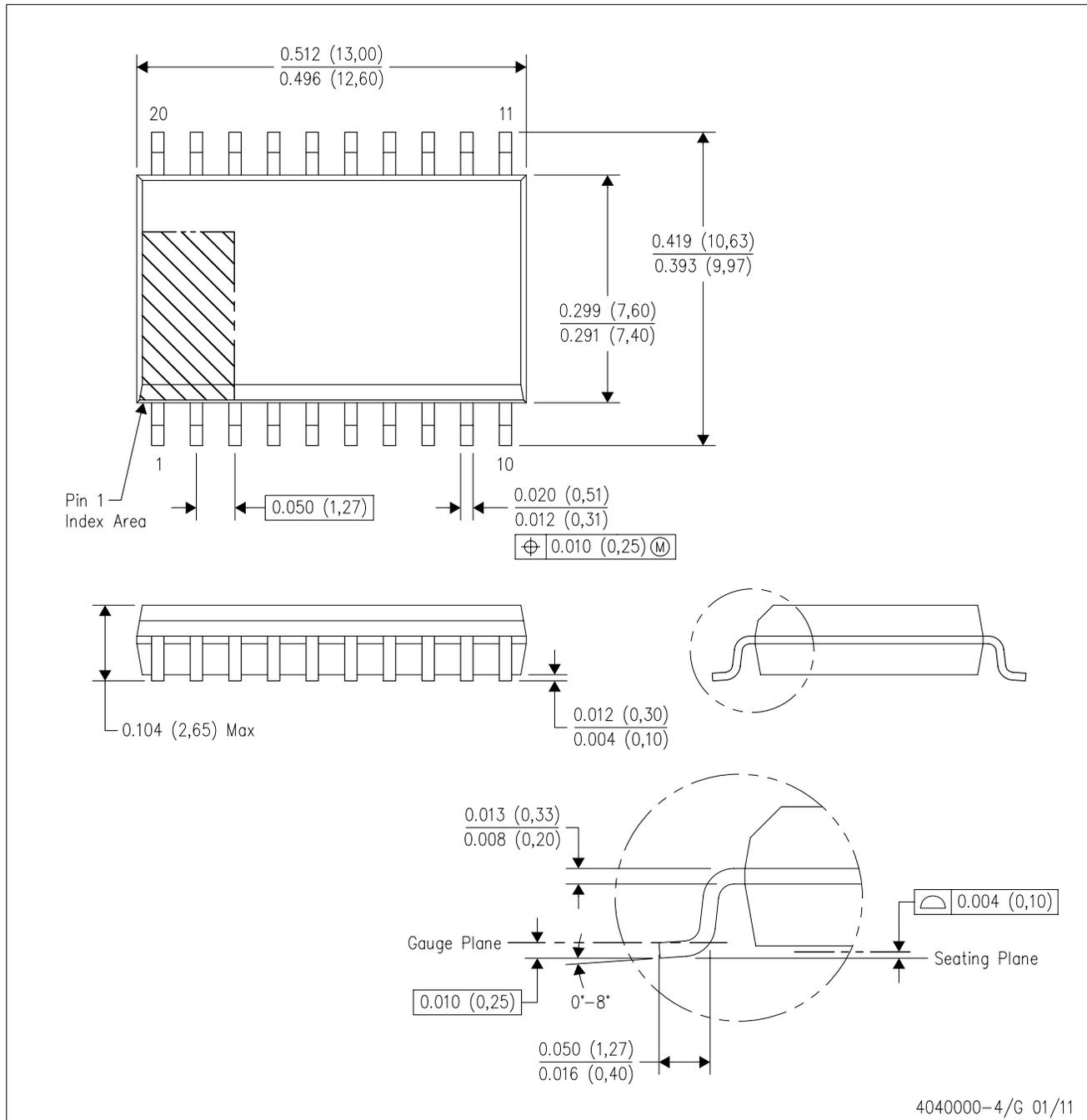
NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M−1994.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
        D. Falls within JEDEC MS−013 variation AC.
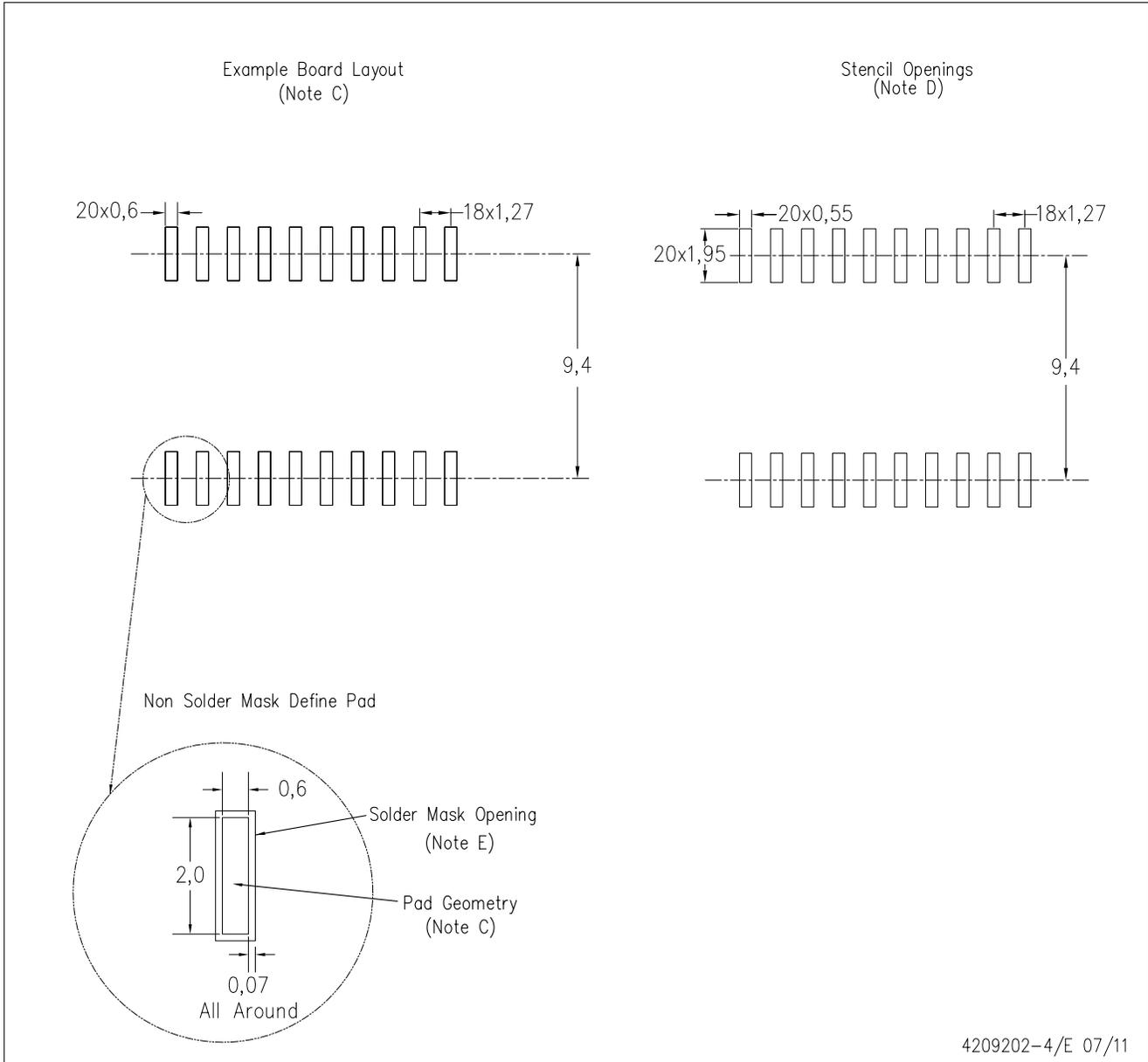
TEXAS INSTRUMENTS
www.ti.com

DW (R−PDSO−G20)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

Stencil Openings
(Note D)

20x0,6   18x1,27

20x0,55   18x1,27

20x1,95

9,4

9,4

Non Solder Mask Define Pad

0,6

Solder Mask Opening
(Note E)

2,0

Pad Geometry
(Note C)

0,07
All Around

4209202−4/E 07/11

NOTES: A. All linear dimensions are in millimeters.
          B. This drawing is subject to change without notice.
          C. Refer to IPC7351 for alternate board design.

          D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC−7525

          E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R−PDSO−G20)   PLASTIC SMALL OUTLINE

0,65   0,30 / 0,19   ⊕ 0,10 Ⓜ

20   11

⚠D 4,50 / 4,30   6,60 / 6,20

1   10

6,60 / 6,40

⚠C

0,15 NOM
Gage Plane
0°−8°   0,25   0,75 / 0,50

1,20 MAX   0,15 / 0,05

Seating Plane
⬭ 0,10
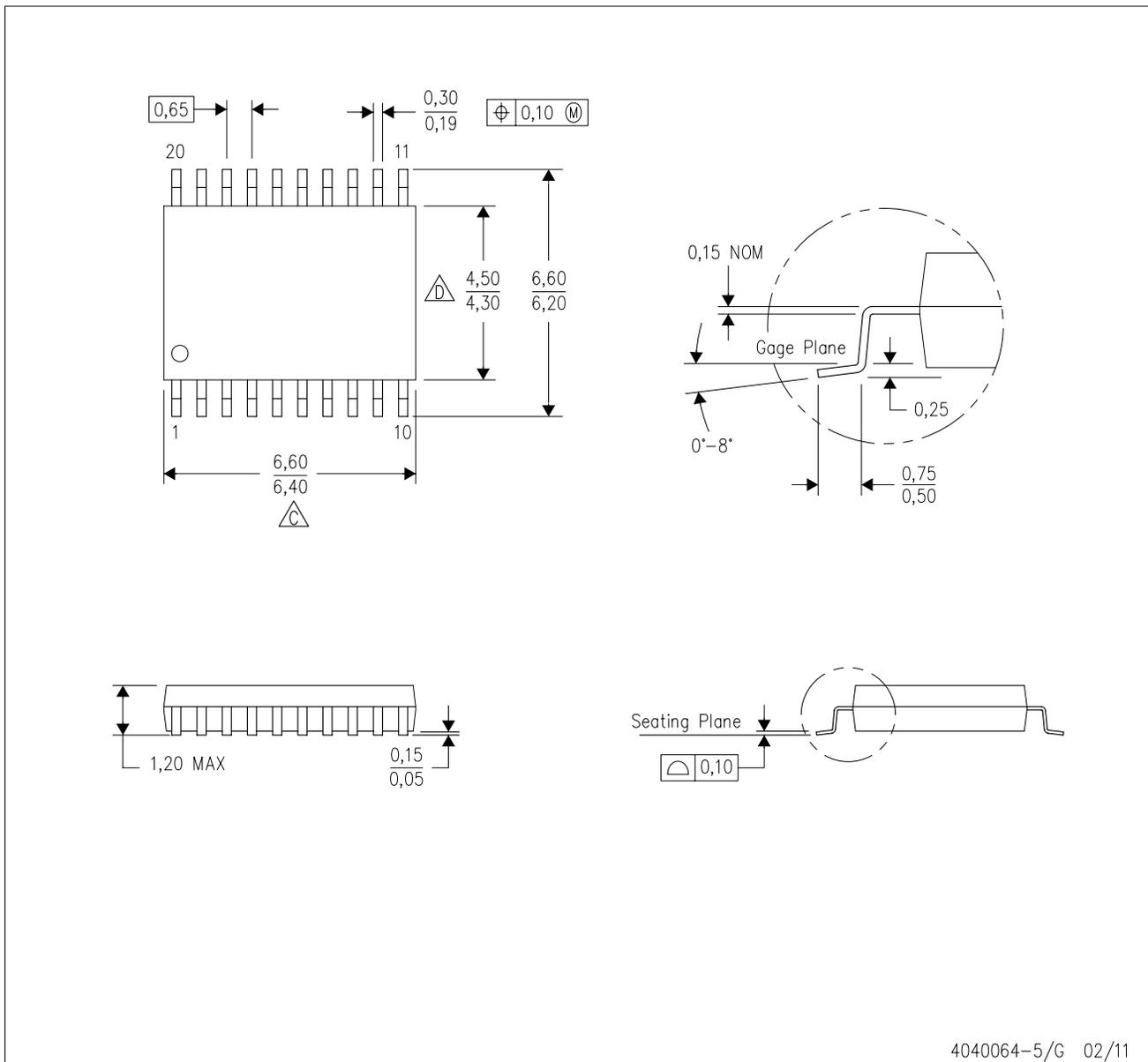
4040064−5/G 02/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
        B. This drawing is subject to change without notice.
        ⚠C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
        ⚠D Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
        E. Falls within JEDEC MO−153
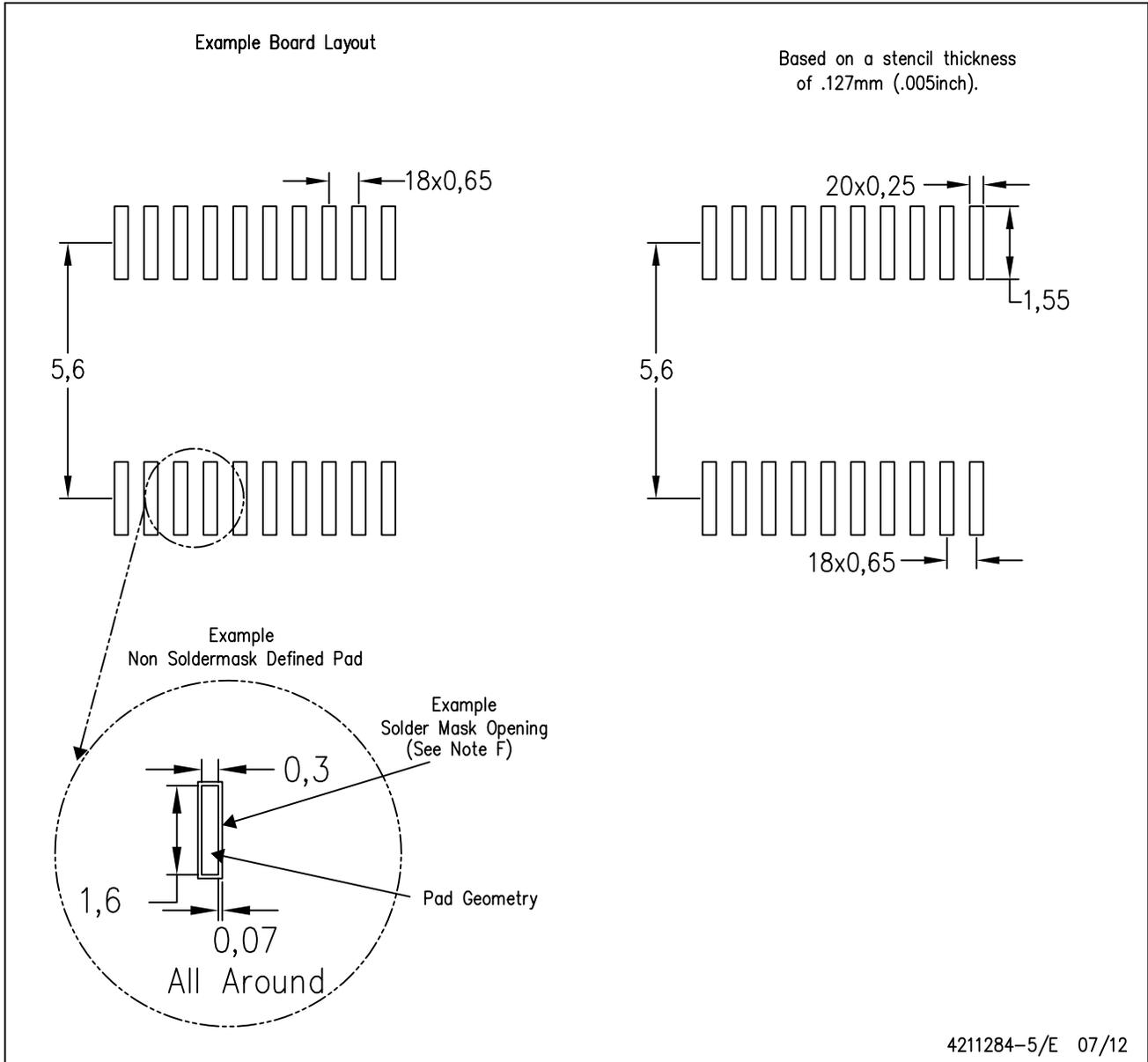
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PW (R−PDSO−G20)   PLASTIC SMALL OUTLINE

Example Board Layout

Based on a stencil thickness
of .127mm (.005inch).

18x0,65

20x0,25

1,55

5,6

5,6

18x0,65

Example
Non Soldermask Defined Pad

Example
Solder Mask Opening
(See Note F)

0,3

1,6

Pad Geometry

0,07
All Around

4211284−5/E 07/12

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Publication IPC−7351 is recommended for alternate design.
         D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
             contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
         E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

TEXAS
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DB (R-PDSO-G**) **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN
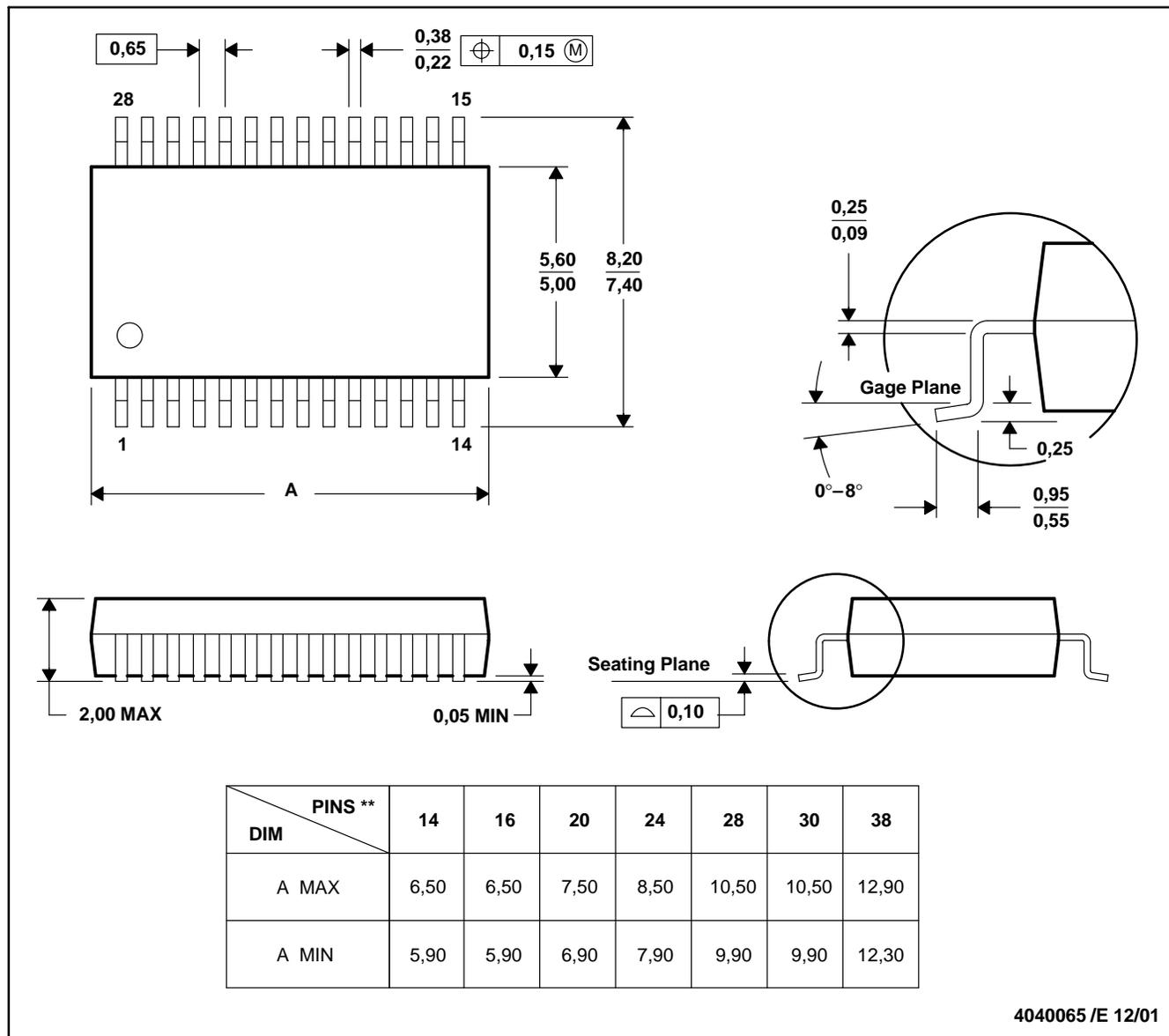
0,65

$\frac{0,38}{0,22}$ ⊕ 0,15 Ⓜ

28   15

$\frac{5,60}{5,00}$ $\frac{8,20}{7,40}$

$\frac{0,25}{0,09}$

Gage Plane

0°−8°

0,25

$\frac{0,95}{0,55}$

1   14

A

2,00 MAX   0,05 MIN

Seating Plane

⌒ 0,10

DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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