PLESSEY
SEMICONDUCTORS

SP1600 SERIES
ECL III

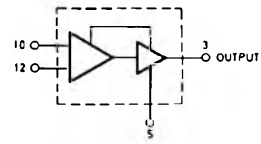
SP1648B
VOLTAGE-CONTROLLED OSCILLATOR

The SP1648 is an emitter-coupled oscillator, constructed on a single monolithic silicon chip. Output levels are compatible with PECL III logic levels. The oscillator requires an external parallel tank circuit consisting of the inductor (L) and capacitor (C).

A varactor diode may be incorporated into the tank circuit to provide a voltage variable input for the oscillator (VCO). The device may also be used in phase locked loops and many other applications requiring a fixed or variable frequency clock source of high spectral purity.

The SP1648 may be operated from a +5.0 Vdc supply or a −5.2 Vdc supply, depending upon system requirements.

SUPPLY VOLTAGE	GND PINS	SUPPLY PINS
+5.0 Vdc	7, 8	1, 14
−5.2 Vdc	1, 14	7, 8



Input Capacitance = 6pF typ
Maximum Series Resistance for L (External Inductance) = 50 Ω typ.
Power Dissipation = 150mW typ/pkg (+5.0 Vdc Supply)
Maximum Output Frequency = 225 Mhz typ

DG14

Fig. 1 Block diagram of SP1648

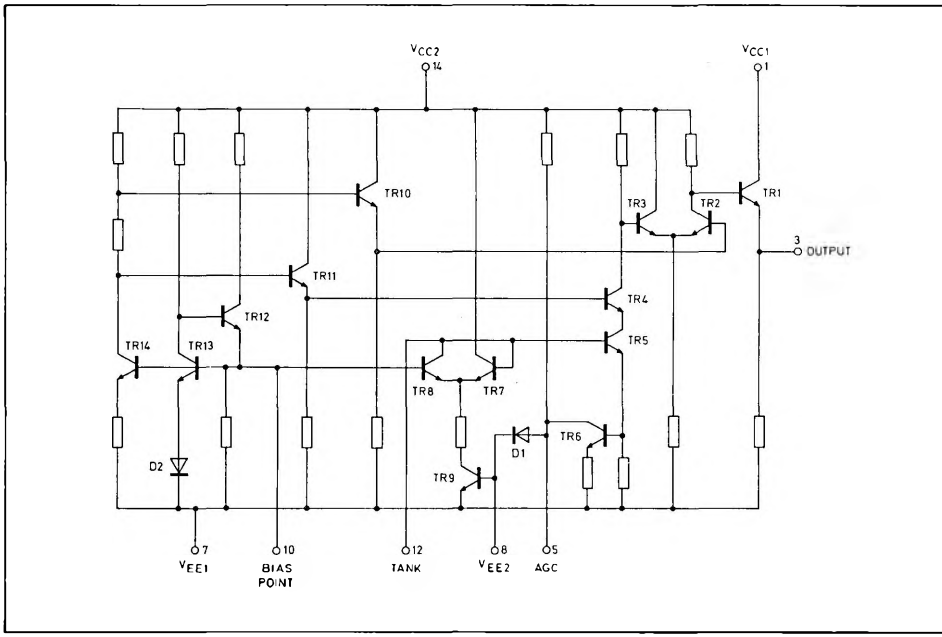


Fig. 2 Circuit diagram of SP1648

ELECTRICAL CHARACTERISTICS

Supply Voltage = +5.0 volts

@ Test Temperature	TEST VOLTAGE/CURRENT VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	V_{CC}	mAdc I_L
0°C	+1.900	+1.400	5.0	-5.0
+25°C	+1.800	+1.300	5.0	-5.0
+75°C	+1.700	+1.200	5.0	-5.0

Characteristic	Symbol	Pin Under Test	SP1648 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW $V_{IH\ max}$	$V_{IL\ min}$	V_{CC}	I_L	V_{EE} (Gnd)
Power Supply Drain Current	I_E	8	–	–	–	35	–	–	mAdc	–	–	1, 14		7, 8
Logic "1" Output Voltage	V_{OH}	3	4.00	4.16	4.04	4.19	4.10	4.28	Vdc	–	12	1, 14	3	7, 8
Logic "0" Output Voltage	V_{OL}	3	3.18	3.42	3.20	3.43	3.22	3.46	Vdc	12	–	1, 14	3	7, 8
Bias Voltage*	V_{Bias}*	10	1.45	1.8	1.4	1.7	1.3	1.6	Vdc	–	–	1, 14	–	7, 8
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max						
Peak-to-Peak Tank Voltage	V_{p-p}	12	–	–	–	–	500	–	–	–	–	mV	See Figure 4	–	1, 14	3	7, 8
Output Duty Cycle	V_{DC}	3	–	–	–	–	50	–	–	–	–	%	See Figure 4	–	1, 14	3	7, 8
Oscillation Frequency	f_{max}	–	–	–	–	195	225	–	–	–	–	MHz	See Figure 4	–	1, 14	3	7, 8

* This measurement guarantees the dc potential at the bias for purposes of incorporating a varactor diode at this point.

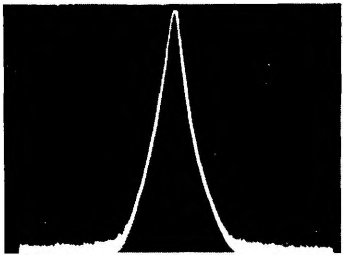
ELECTRICAL CHARACTERISTICS

Supply Voltage = –5.2 volts

@ Test Temperature	TEST VOLTAGE/CURRENT VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	V_{EE}	mAdc I_L
0°C	–3.300	–3.800	–5.2	–5.0
+25°C	–3.400	–3.900	–5.2	–5.0
+75°C	–3.500	–4.000	–5.2	–5.0

Characteristic	Symbol	Pin Under Test	SP1648 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW $V_{IH\ max}$	$V_{IL\ min}$	V_{EE}	I_L	V_{CC} (Gnd)
Power Supply Drain Current	I_E	8	–	–	–	36	–	–	mAdc	–	–	7, 8	–	1, 14
Logic "1" Output Voltage	V_{OH}	3	–1.000	–0.840	–0.960	–0.810	–0.900	–0.720	Vdc	–	12	7, 8	3	1, 14
Logic "0" Output Voltage	V_{OL}	3	–1.870	–1.635	–1.850	–1.620	–1.830	–1.595	Vdc	12	–	7, 8	3	1, 14
Bias Voltage*	V_{Bias}*	10	–3.750	–3.400	–3.800	–3.500	–3.900	–3.600	Vdc	–	–	7, 8	–	1, 14
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max						
Peak-to-Peak Voltage	V_{p-p}	12	–	–	–	–	500	–	–	–	–	mV	See Figure 4	–	7, 8	3	1, 14
Output Duty Cycle	V_{DC}	3	–	–	–	–	50	–	–	–	–	%	See Figure 4	–	7, 8	3	1, 14
Oscillation Frequency	f_{max}	–	–	–	–	195	225	–	–	–	–	MHz	See Figure 4	–	7, 8	3	1, 14

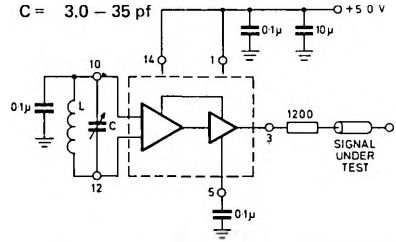
* This measurement guarantees the dc potential at the bias point for purposes of incorporating a varactor tuning diode at this point.



B.W. = 10kHz
Center Frequency = 100MHz
Scan Width = 50kHz/div
Vertical Scale = 10db/div

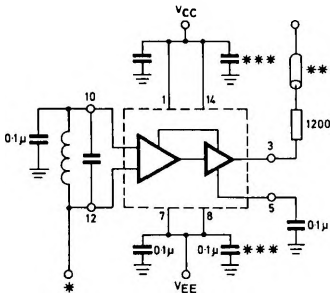
L: Micro Metal torroid #T20.13, 8 turns
#30 Enameled Copper wire.

C = 3.0 – 35 pf



* The 1200 ohm resistor and the scope termination impedance constitute a 25:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

Fig. 3 Spectral purity of signal at output



* Use high impedance probe (>1.0 Megohm must be used).

* * The 1200 -ohm resistor and the scope termination impedance constitute a 25:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

* * * Bypass only that supply opposite ground.

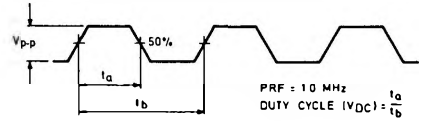


Fig. 4 Test circuit and waveforms

OPERATING CHARACTERISTICS

Figure 1 illustrates the circuit schematic for the SP1648. The oscillator incorporates positive feedback by coupling the base of transistor TR7 to the collector of TR8. An automatic gain control (AGC) is incorporated to limit the current through the emitter-coupled pair of transistors (TR7 and TR8) and allow optimum frequency response of the oscillator.

In order to maintain the high Q of the oscillator, and provide high spectral purity at the output, a cascode transistor (TR4) is used to translate from the emitter follower (TR5) to the output differential pair TR2 and TR3. TR2 and TR3, in conjunction with output transistor TR1, provide a highly buffered output which produces a square wave. Transistors TR10 thru TR14 provide this bias drive for the oscillator and output buffer. Figure 3 indicates the high spectral purity of the oscillator output (pin 3).

When operating the oscillator in the voltage controlled mode (Figure 5), it should be noted that the cathode of the varactor diode (D) should be biased at least 2 V_{BE} above V_{EE} ($\approx$ 1.4 V for positive supply operation).

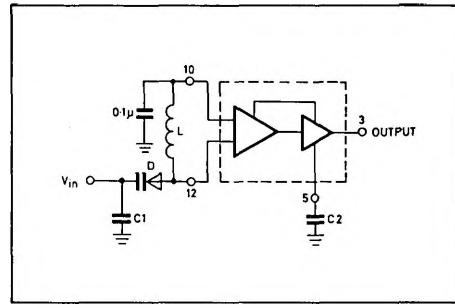


Fig. 5 The SP1648 operating in the voltage-controlled mode

When the SP1648 is used with a constant dc voltage to the varactor diode, the output frequency will vary slightly because of internal noise. This variation is plotted versus operating frequency in Figure 6.

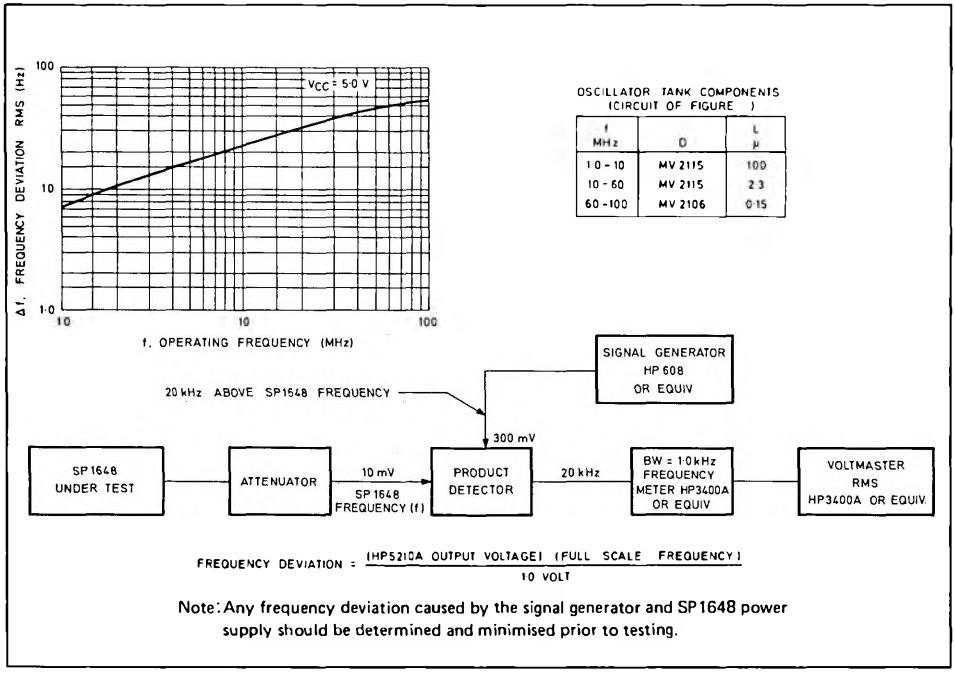


Fig. 6 Frequency deviation test circuit

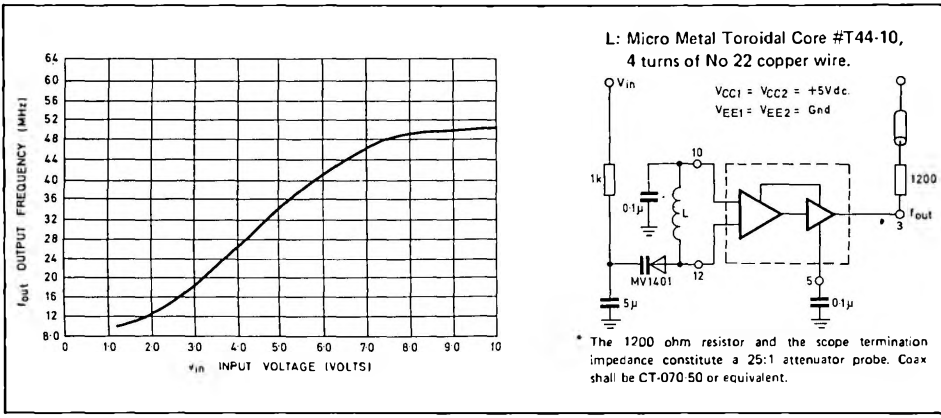


Fig. 7

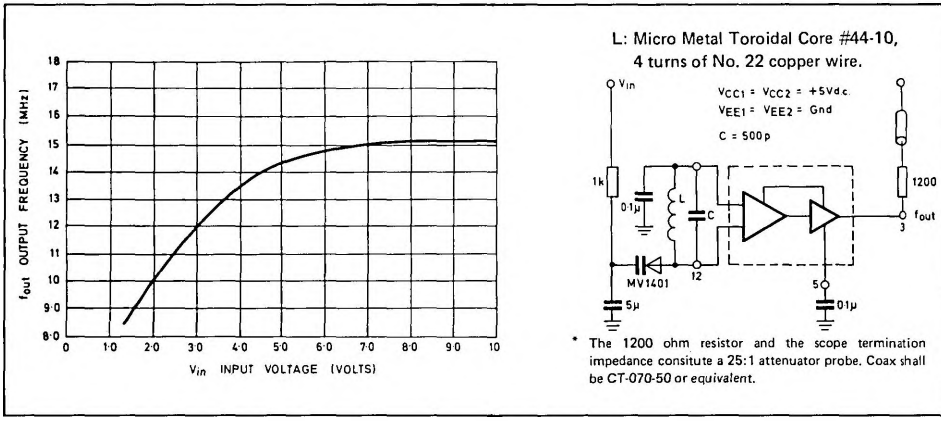


Fig. 8

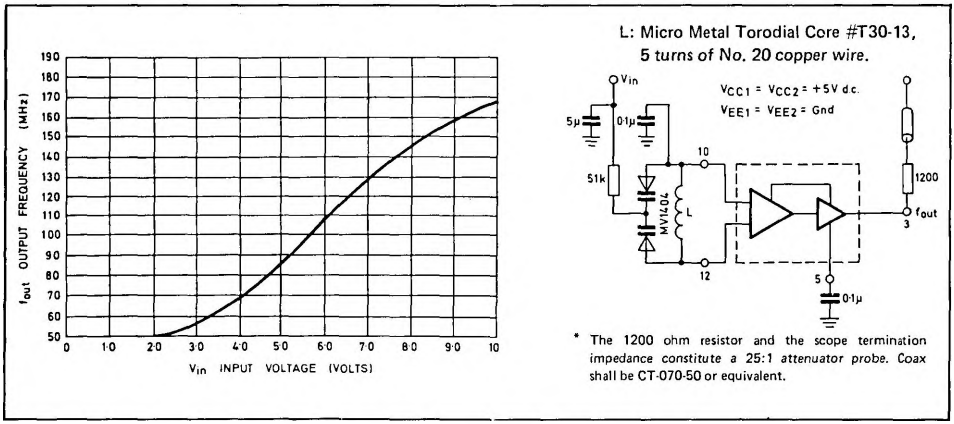


Fig. 9

Typical transfer characteristics for the oscillator in the voltage controlled mode are shown in Figures 7, 8, and 9. Figures 7 and 9 show transfer characteristics employing only the capacitance of the varactor diode (plus the input capacitance of of the oscillator, 6pF typical). Figure 8 illustrates the oscillator operating in a voltage controlled mode with the output frequency range limited. This is achieved by adding a capacitor in parallel with the tank circuit as shown. The 1 kΩ resistor in Figures 7 and 8 is used to protect the varactor diode during testing. It is not necessary as long as the dc input voltage does not cause the diode to become forward biased. The larger-valued resistor (51 kΩ) in Figure 9 is required to provide isolation for the high-impedance junctions of the two varactor diodes.

The tuning range of the oscillator in the voltage controlled mode may be calculated as:

$$\frac{f_{max}}{f_{min}} = \frac{\sqrt{C_D(max) + C_S}}{\sqrt{C_D(min) + C_S}}$$

where $f_{min} = \dfrac{1}{2\pi\sqrt{L\,(C_D(max) + C_S)}}$

C_S = shunt capacitance (input plus external capacitance).

C_D = varactor capacitance as a function of bias voltage.

Good RF and low-frequency by-passing is necessary on the power supply pins (see Figure 3).

Capacitors (C1 and C2 of Figure 5) should be used to bypass the AGC point and the VCO input (varactor diode), guaranteeing only dc levels at these points.

For output frequency operation between 1 MHz and 50 MHz a 0.1μF capacitor is sufficient for C1 and C2. At higher frequencies, smaller values of capacitance should be used; at lower frequencies, larger values of capacitance. At higher frequencies the value of bypass capacitors depends directly upon the physical layout of the system. All bypassing should be as close to the package pins as possible to minimize unwanted lead inductance.

The peak-to-peak swing of the tank circuit is set internally by the AGC circuitry. Since voltage swing of the tank circuit provides the drive for the output buffer, the AGC potential directly affects the output waveform. If it is desired to have a sine wave at the output of the SP1648, a series resistor is tied from the AGC point to the most negative power potential (ground if +5.0 volt supply is used, −5.2 volts if a negative supply is used).

At frequencies above 100 MHz typ, it may be necessary to increase the tank circuit peak-to-peak voltage in order to maintain a square wave at the output of the SP1648. This is accomplished by tying a series resistor (1 kΩ minimum) from the AGC to the most positive power potential (+5.0 volts if a +5.0 volt supply is used, ground if a −5.2 volt supply is used).