

SP 1674B (HIGH Z)

SP 1675 B (LOW Z)

TRIPLE 2-INPUT EXCLUSIVE-NOR GATE

This three gate array is designed to provide the positive logic Exclusive-NOR function in high speed applications. These devices contain a temperature compensated internal bias which insures that the threshold point remains in the centre of the transition region over the temperature range (0° to +75°). Input pulldown resistors eliminate the need to tie unused inputs to VEE.

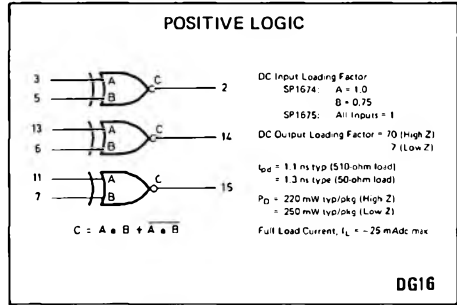
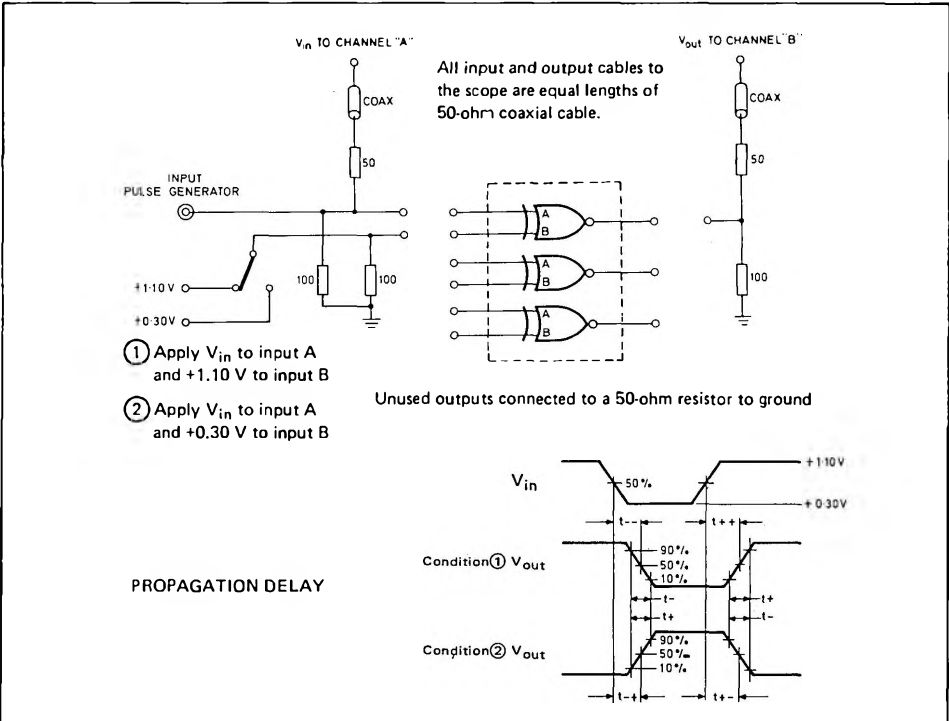


Fig. 1 Logic diagram of SP1674/1675



ELECTRICAL CHARACTERISTICS

This PECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC-14AZCB or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is in either a test socket or mounted on a printed circuit board. Outputs are tested with a 50-ohm resistor to -2.0 V.

Characteristic	Symbol	Pin Under Test	SP1674/SP1675 Test Limits										TEST VOLTAGE VALUES					
			0°C		+25°C		+75°C		Unit	V _{IH} max	V _{IH} min	V _{IHA} min	V _{IHA} max	V _{IILA} max	V _{EE}			
			Min	Max	Min	Max	Min	Max								V _{IL} max	V _{IL} min	V _{IHA} min
Power Supply Diem Current	I _E (Hi-Z) I _E (Lo-Z)	8 8	-	-	-	55 70	-	-	mAdc mAdc	-	-	-	-	-	8 8	1.16 1.16		
Input Current	I _{in} H 0.75 I _{in} H I _{in} L	3,11,13 5,6,7 *	-	-	-	350 270	-	-	μAdc μAdc	-	-	-	-	-	8 8	1.16 1.16		
Input Current	I _{in} L	*	-	-	0.5	-	-	-	μAdc	-	-	-	-	-	8	1.16		
Logic "1" Output Voltage	V _{OH}	2	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	Vdc	3.5	3.5	-	-	-	8	1.16		
Logic "0" Output Voltage	V _{OL}	2	-1.870	-1.635	-1.850	-1.620	-1.830	-1.595	Vdc	3.5	3.5	-	-	-	8	1.16		
Logic "1" Threshold Voltage	V _{OH(A)}	2	-1.020	-	-0.980	-	-0.920	-	Vdc	-	-	3.5	3.5	3.5	8	1.16		
Logic "0" Threshold Voltage	V _{OL(A)}	2	-	-1.615	-	-1.500	-	-1.575	Vdc	-	-	3	3	3	8	1.16		
Switching Times (50Ω Load)			Typ	Max	Typ	Max	Typ	Max										
Propagation Delay	t _p 2+ t _p 3-2+ t _p 3-3- t _p 5+2+ t _p 5-2+ t _p 5-2-	2 2 2 2 2	1.3 1.4 1.4 1.7	1.8 1.8 1.4 2.3	1.3 1.4 1.7 1.7	1.8 1.9 1.6 2.3	1.5 1.5 1.9 1.9	2.2 2.2 2.3 2.7	ns	-	-	-	-	-	-	-		
Rise Time	t _r +	2	1.9	2.5	1.9	2.5	2.1	2.8	ns	-	-	-	-	-	8	1.16		
Fall Time	t _f -	2	1.6	2.2	1.6	2.2	1.8	2.5	ns	-	-	-	-	-	8	1.16		

© Test Temperature
0°C
+25°C
+75°C

TEST VOLTAGE APPLIED TO PINS LISTED BELOW:

V _{IH} max	V _{IH} min	V _{IHA} min	V _{IHA} max	V _{IILA} max	V _{EE}
-0.840	-1.870	-1.135	-1.500	-	-5.2
-0.810	-1.850	-1.095	-1.485	-	-5.2
-0.720	-1.830	-1.035	-1.460	-	-5.2

* Individually test each input applying V_{IH} or V_{IL} to input under test.