PLESSEY
SEMICONDUCTORS

SP1600 SERIES
ECL III

SP1690B
UHF PRESCALER TYPE D FLIP-FLOP

The SP1690 is a high speed D master-slave flip-flop capable of toggle rates over 500 MHz. Designed primarily for high speed prescaling applications in communications and instrumentation, this device employs two data inputs, two clock inputs and complementary $\overline{Q}$ and Q outputs. It is a higher frequency replacement for the SP1670 (350 MHz) D flip-flop. No set or reset inputs are provided and an extra data input is provided on pin 11.

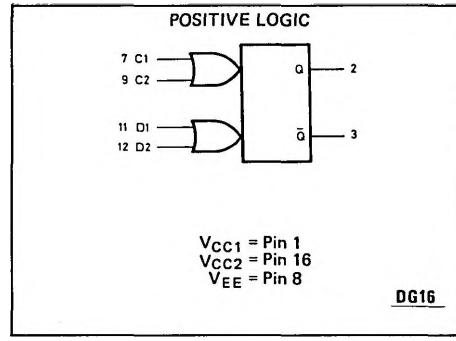
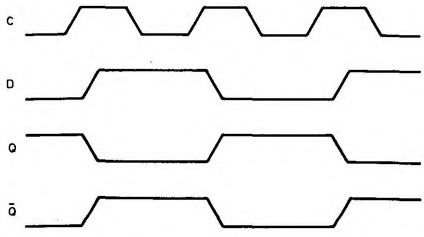


Fig. 1 Logic diagram of SP1690

FEATURES

- P_D = 200 mW typ/pkg (No Load)
- f_{tog} = 500 MHz min



TRUTH TABLE

C	D	Q_{n+1}
L	ø	Q_n
H	ø	Q_n
⌐	L	L
⌐	H	H

C = C1 + C2 ø = Don't Care
D = D1 + D2

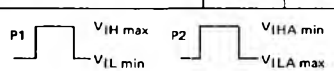
Fig. 2 Timing diagram

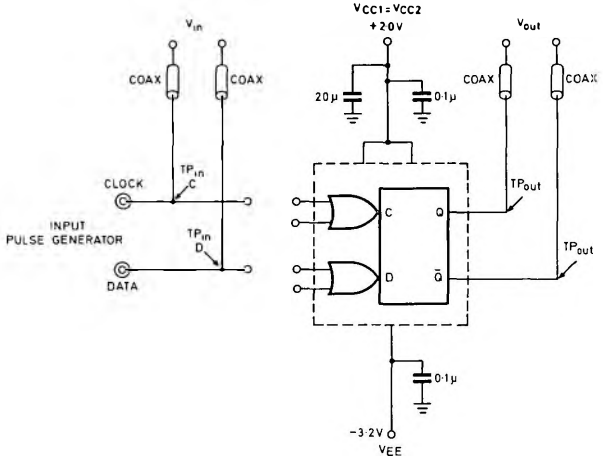
ELECTRICAL CHARACTERISTICS

Each PECL III series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
0°C	−0.840	−1.870	−1.135	−1.500	−5.2
+25°C	−0.810	−1.850	−1.095	−1.485	−5.2
+75°C	−0.720	−1.830	−1.035	−1.460	−5.2

Characteristic	Symbol	Pin Under Test	SP1690 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	P1	P2	Gnd
Power Supply Drain Current	I_E	8	–	–	–	59	–	–	mAdc	7,9,11,12	–	–	–	8	–	–	1,16
Input Current	$I_{in\ H}$	7	–	–	–	250	–	–	μAdc	7	–	–	–	8	–	–	1,16
		11	–	–	–	270	–	–	μAdc	11	–	–	–	8	–	–	1,16
	$I_{in\ L}$	7	–	–	0.5	–	–	–	μAdc	–	7	–	–	8	–	–	1,16
		11	–	–	0.5	–	–	–	μAdc	–	11	–	–	8	–	–	1,16
Logic "1" Output Voltage	V_{OH}	2	−1.000	−0.840	−0.960	−0.810	−0.900	−0.720	Vdc	11	–	–	–	8	7	–	1,16
Logic "0" Output Voltage	V_{OL}	2	−1.870	−1.635	−1.850	−1.620	−1.830	−1.595	Vdc	–	11	–	–	8	7	–	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	−1.020	–	−0.980	–	−0.920	–	Vdc	11	–	–	–	8	–	7	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	−1.615	–	−1.600	–	−1.575	Vdc	–	11	–	–	8	–	7	1,16
Switching Parameters					Min	Typ	Max							−3.2 Vdc			+2.0 Vdc
Clock to Output Delay	t_{7+2+}	2	–	–	–	1.5	–	–	–	ns	–	–	–	–	8	–	–	1,16
	t_{8+2+}		–	–	–	1.5	–	–	–		–	–	–	–		–	–	
Output Rise Time	t_+		–	–	–	1.3	–	–	–		–	–	–	–		–	–	
Output Fall Time	t_-		–	–	–	1.3	–	–	–		–	–	–	–		–	–	
Setup Time	$t_{setup\ H}$		–	–	–	0.3	–	–	–		–	–	–	–		–	–	
	$t_{setup\ L}$		–	–	–	0.3	–	–	–		–	–	–	–		–	–	
Hold Time	$t_{hold\ H}$		–	–	–	0.2	–	–	–		–	–	–	–		–	–	
	$t_{hold\ L}$		–	–	–	0.3	–	–	–		–	–	–	–		–	–	
Toggle Frequency	t_{tog}	2	–	–	500	540	–	–	–	MHz	–	–	–	–	8	–	–	1,16





All input and output cables to the scope are equal lengths of 50-ohm coaxial cable

50-ohm termination to ground located in each scope channel input

Fig. 3 Propagation delay test circuit

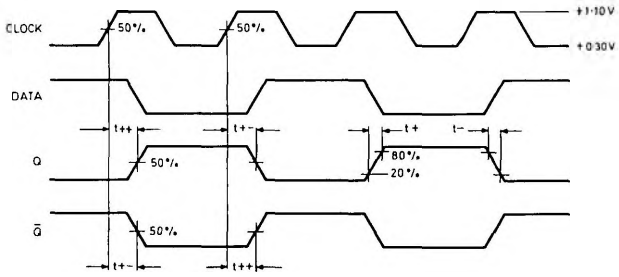


Fig. 4 Clock delay waveforms at +25°C

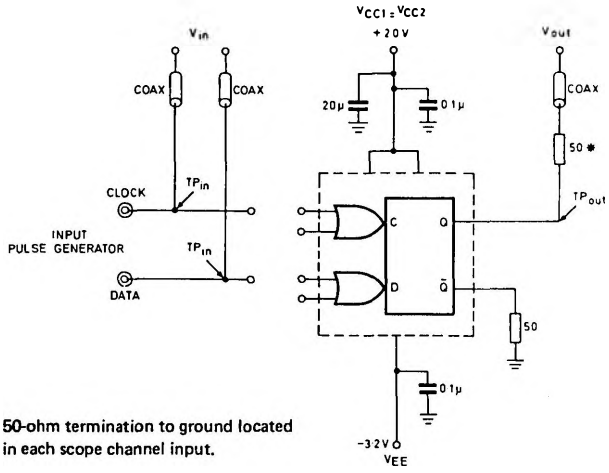
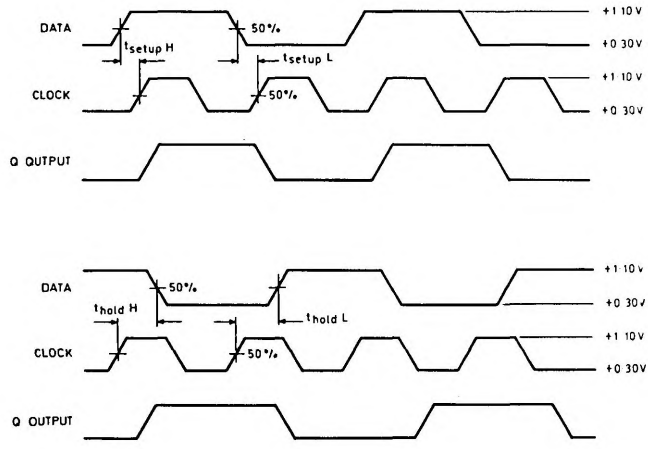


Fig. 5 Set up and hold time test circuit



Setup time is the minimum time before the positive transition of the clock pulse (C) that information must be present at the date (D) input.

Hold time is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the data (D) input.

Fig. 6 Set up and hold time waveforms

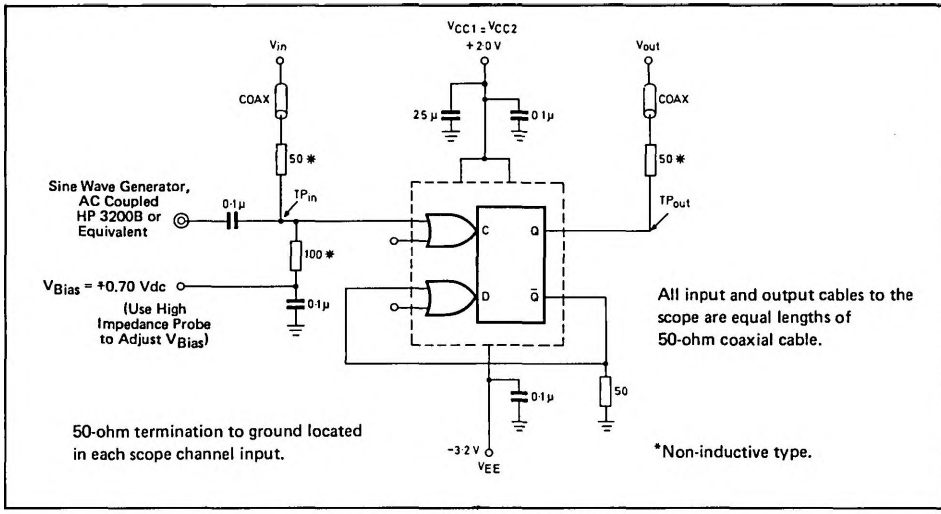
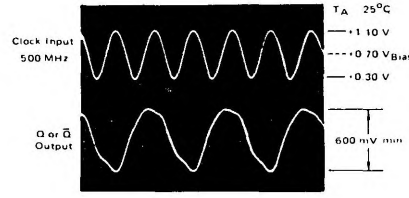


Fig. 7 Toggle frequency test circuit



The maximum toggle frequency of the SP1690 has been exceeded when either:

1. The output peak-to-peak voltage swing falls below 600 millivolts,

   OR

2. The device ceases to toggle (divide by two).

Fig. 8 Toggle frequency waveforms