

SP8000 SERIES HIGH SPEED DIVIDERS

SP8600A&B&M 250MHz ÷ 4 COUNTER

The SP8600 is a fixed ratio emitter coupled logic $\div 4$ counter with a specified input frequency range of 15—250 MHz. The operating temperature range is specified by the device code suffix letter: 'A' denotes -55° C to $+125^{\circ}$ C, 'B' denotes 0° C to $+70^{\circ}$ C operation, 'M' denotes -40° C to $+85^{\circ}$ C.

Intended for use with an external bias arrangement and capacitive coupling to the signal source, the SP8600 can be either single driven, or double driven with two complementary input signals.

The outputs are complementary free collectors that can have their load resistors taken to any bias voltage up to 12V more positive than V_{EE}.

FEATURES

- Low Power
- Free Collector Outputs to Interface to TTL
- 250 MHz ÷ 4 Over Full Military Temp.
 Range



Fig. 1 Pin connections (bottom view)

APPLICATIONS

- Synthesizers Mobile and Fixed
- Counters
- Timers



Fig. 2 Circuit diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T _{amb} :	'A' grade 'B' grade 'M' grade	55°C to +125°C 0°C to +70°C 40°C to +85°C					
Supply	voltage Vcc VEE	400 to 800 mV p-p 250 to 800 mV p-p					
Input voltage (single driven — other input decoupled to ground plane)							
Input voltage (double complementary input drive) Input bias voltage							

Bias chain as in test circuit (see Fig. 3 and operating notes).

		Value	_	Units	Conditions
Characteristic	Min.	Τγρ.	Max.		
Max. input frequency	250	390*		MHz	Typical figure quoted at +25°C.
Min. input frequency with sinusoidal input Min. slew rate of			25	MHz	
square wave input for correct operation Output current	1.6		20	V/µs mA	Single input drive Input f=250 MHz.
Power supply drain current		16*	25	mA	V _{EE} = = —5.2 V, V _{BIAS} as Fig. 3.

*~t +25°C



Fig. 3 Test circuit



Fig. 4 Maximum input frequency v. power supply voltage (typical)



Fig. 5 Maximum input frequency v. temperature

OPERATING NOTES

The circuit performance obtained from the SP8600 is optimized if normal high frequency rules for circuit layout are obeyed — leads should be kept short, capacitors and resistors should be of non-inductive types, etc.

The signal source is normally AC coupled to one of the inputs or, if complementary signals are available, to both inputs. The inputs require an external bias chain to set the DC potential on the inputs (see Fig. 3). No appreciable change in performance is observed over a range of DC bias from -2.5V to -3.5V.

Any tendency for the circuit to self-oscillate in the absence of input signal (or when the input signal is very small) can be overcome by offsetting the two inputs by approximately 40mV. using, for example, the bias arrangement shown in Fig. 6. The input wave form may be sinusoidal, but below 25 MHz incorrect operation may occur because of the limited slew rate of the input signal. A square wave input with a slew rate greater than $20V/\mu$ s ensures correct operation down to DC.

The output is in the form of complementary free collectors with at least 2mA available from them. For satisfactory high frequency interfacing to ECL or Schottky TTL the circuit techniques illustrated in Fig. 7 are recommended.

For maximum frequency operation, it is essential that the output load risistor values be such that the output transistors do not saturate. If the load resistors are connected to the OV rail, then saturation can occur with resistance values greater than 600Ω . Of course, if the load resistors are taken to a more positive potential, then higher values can be used. N.B. If only one output is used, the other output should be connected to OV.



Fig. 6 Bias arrangement to prevent self-oscillation under no-signal conditions



Fig. 7 ECL and Schottky TTL interfacing

SP8600

ABSOLUTE MAXIMUM RATINGS

Power supply voltage $V_{CC} - V_{EE}$ Input voltage V_{IN}	10V Not greater than supply voltage in use
Bias voltage on o/p's V_{00T} — V_{EE} Operating junction temperature Storage temperature	14V ÷175°C max. —55°C to +175°C