PLESSEY
SEMICONDUCTORS

SP8000 SERIES
HIGH SPEED DIVIDERS

SP8601A, B & M 150MHz÷4

The SP8601 is a fixed ratio emitter coupled logic ÷4 counter with a maximum specified input frequency of 150 MHz but with a typical maximum operating frequency well in excess of this (see Typical Operating Characteristics). The operating temperature range is specified by the final coding letter: 'A' denotes −55°C to +125°C, 'B' denotes 0°C to +70°C, and 'M' denotes −40°C to +85°C.

The SP8601 can be operated with single input drive or with double, complementary, I/P drive. It can be driven with direct coupling from ECL II levels (or from an SP8602 device), or it can be capacitively coupled to the signal source if an external bias is provided.

There are complementary free collector outputs that can have their external load resistor connected to any bias up to 12 volts more positive than V_{EE}.

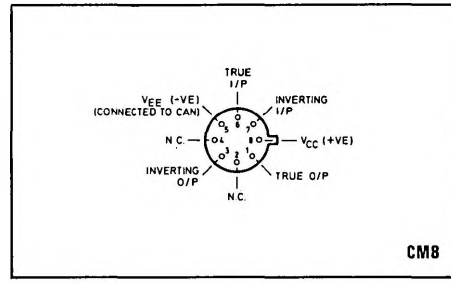


Fig. 1 Pin connections (bottom view)

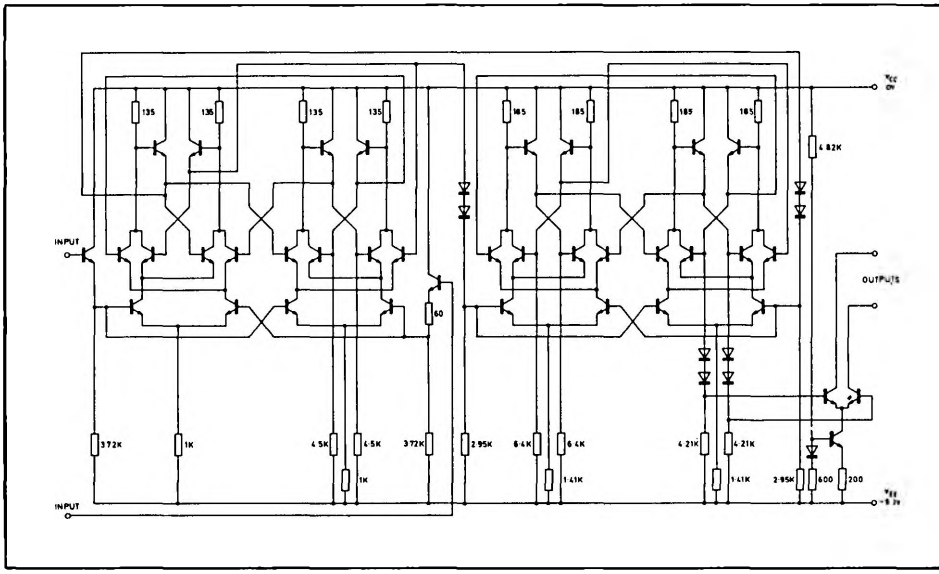


Fig. 2 Circuit diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb}: 'A' grade	−55°C to +125°C
'B' grade	0°C to +70°C
'M' grade	−40°C to +85°C
Operating supply voltage V_{CC}	0V.
V_{EE}	−5.2V ±0.25V
Input voltage (single drive — other input decoupled to ground plane)	400 to 800 mV (p-p)
Input voltage (double drive)	250 to 800 mV (p-p)
Bias voltage	Bias chain as in test circuit (see Fig. 2).

Characteristic	Value			Units	Conditions
	Min	Typ.	Max.		
Max. input frequency	150			MHz.	
Min. input freq. with sinusoidal input.			15	MHz.	
Min. slew rate of square wave input for correct operation			20	V/μs	Single input drive
Output current	1.6			mA	Input freq.= 150 MHz. R_{load} = 50Ω
Power supply drain current		18	25	mA	V_{EE} = −5.2V

OPERATING NOTES

Circuit performance obtained from the SP8601 is optimised if normal high frequency rules for circuit layout are obeyed — leads should be kept short, capacitors and resistors should be of non-inductive types, etc.

The signal source is normally directly coupled into the device, which will tolerate a wide range of input bias voltages, but was designed for inputs from ECL II levels and can therefore be satisfactorily driven from SP8602 range of counters. The bias voltage on the input marginally affects the overall power consumption of the device (For typical operating characteristics with varying bias voltages see Fig. 4).

If it is not practicable to directly couple the input signal, then a bias chain similar to the one shown in Fig. 3 can be used.

The input waveform may be sinusoidal, but below about 10 MHz incorrect operation may occur because of the limited slew rate of the input signal. A square wave input with a slew rate of greater than 20 V/μs ensures correct operation down to DC.

The output is in the form of complementary free collectors with 2 mA min. available from them. The output voltage swing obviously depends on the value of load resistor used and also the frequency of operation. The following table gives some typical examples of output voltage for different load resistors. With careful board layout to minimise capacitance these figures can easily be exceeded.

Min. Output Voltage	Load Resistor	Input Frequency
1.1V	1kΩ	120 MHz
320mV	200Ω	150 MHz
80mV	50Ω	180 MHz

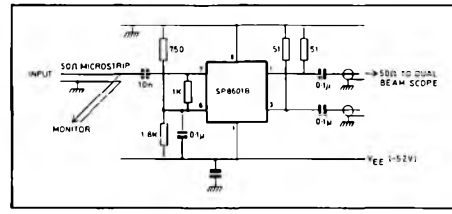
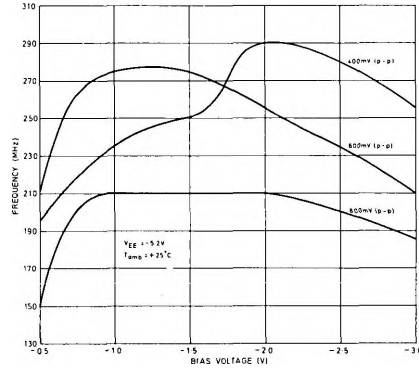


Fig. 3 Test circuit

TYPICAL OPERATING CHARACTERISTICS



NOTE: The value of the coupling and decoupling capacitors used are uncritical but they should be of a type and value suitable for the frequencies involved.

Fig. 4 Maximum input frequency v. bias voltage at single input drive levels of 400, 600 and 800 mV (typical device)

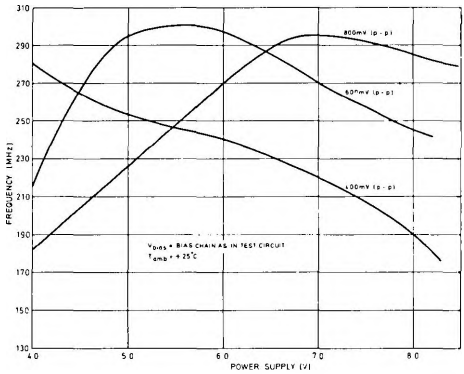


Fig. 5 Maximum frequency v. power supply voltage at single input drive levels of 400, 600 and 800 mV (typical device)

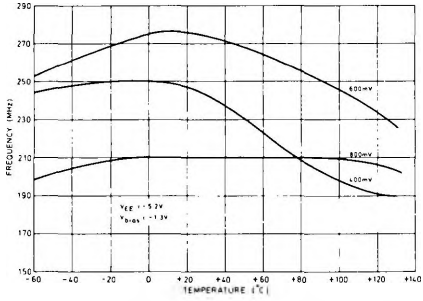


Fig. 6 Maximum input frequency v. temperature at single input drive levels of 400, 600 and 800 mV (typical device)

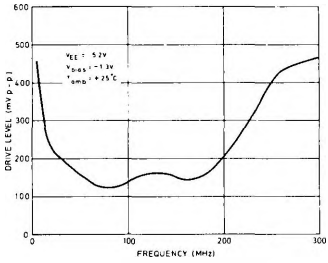


Fig. 7 Minimum single input drive level for correct operation v. input frequency (typical device)

APPLICATION NOTES

The SP8601 used with two SP8602 series ÷2 counters to give a 500 MHz divide-by-sixteen prescaler is shown in Fig. 8. Capacitors marked thus * may need to be increased in value for low frequency operation.

For correct operation when interfacing with TTL and ECL II the circuits shown in Figs. 9, 10 and 11 are recommended.

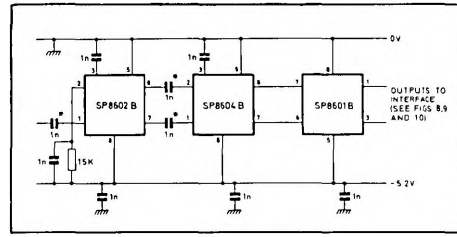


Fig. 8 Divide-by-sixteen prescaler

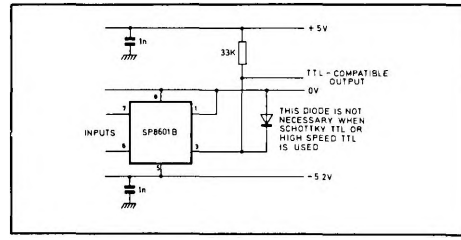


Fig. 9 TTL interface (fanout = 1 TTL gate)

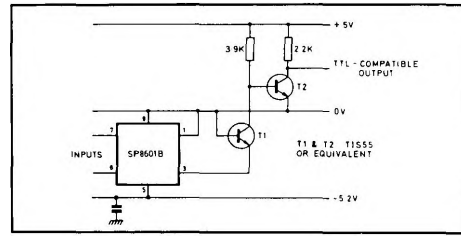


Fig. 10 High fanout TTL interface

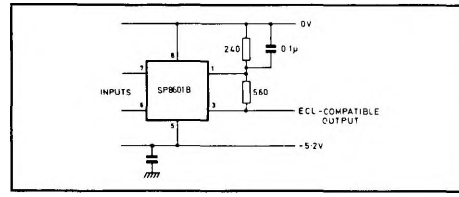


Fig. 11 ECL II interface

ABSOLUTE MAXIMUM RATINGS

Power supply voltage	
V_{CC}—V_{EE}	10 V
Input voltage V_{in}	Not greater than the supply voltage in use
Bias voltage on outputs	
V_{out}—V_{EE}	14 V
(see Operating Notes)	
Operating junction temperature	+175 C
Storage temperature	−55 C to +175 C