PLESSEY
SEMICONDUCTORS

SP 8000 SERIES

HIGH SPEED DIVIDERS

SP 8640A, B & M 200 MHz
SP 8641A, B & M 250 MHz
SP 8642A, B & M 300 MHz
SP 8643A, B & M 350 MHz
SP 8646A, B & M 200 MHz TTL OUTPUTS
SP 8647 A, B & M 250 MHz TTL OUTPUTS

UHF PROGRAMMABLE DIVIDERS ÷10/11

In frequency synthesis it is desirable to start programmable division at as high a frequency as possible, because this raises the comparison frequency and so improves the overall synthesiser performance.

The SP8640 series are UHF integrated circuits that can be logically programmed to divide by either 10 or 11, with input frequencies up to 350 MHz. The design of very fast fully programmable dividers is therefore greatly simplified by the use of these devices and makes them particularly useful in frequency synthesisers operating in the UHF band.

Inputs and outputs are ECL compatible throughout the temperature range: the clock inputs and programming inputs are ECL III compatible while the two complementary outputs are ECL II compatible to reduce power consumption in the output stage. ECL 10K output compatability can be achieved very simply however (see Operating Notes). The SP8646/7 feature an additional TTL compatible output.

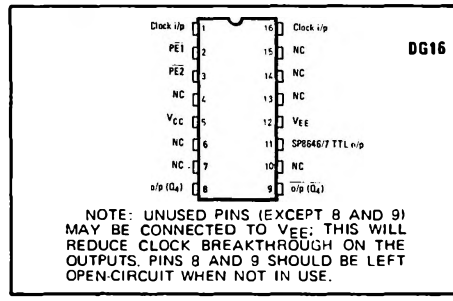
The division ratio is controlled by two $\overline{PE}$ inputs. The counter will divide by 10 when either $\overline{PE}$ input is in the high state and by 11 when both inputs are in the low state. Both the $\overline{PE}$ inputs and the clock inputs have nominal 4.3k Ω pulldown resistors to V_{EE} (negative rail).

FEATURES

- Military and Industrial Variants.
- 350 MHz Toggle Frequency
- Low Power Consumption
- ECL Compatibility on All I/Ps & O/Ps
- Low Propagation Delay
- True and Inverse Outputs
- Optional TTL Output

QUICK REFERENCE DATA

- Full Temperature Range Operation:
  'A' Grade —55°C to +125°C
  'B' Grade 0°C to +70°C
  'M' Grade —40°C to +85°C
- Supply Voltage
  $|V_{CC} - V_{EE}|$ 5.2V
- Power Consumption 250mW Typ.
- Propagation Delay 3ns Typ.



NOTE: UNUSED PINS (EXCEPT 8 AND 9) MAY BE CONNECTED TO V_{EE}; THIS WILL REDUCE CLOCK BREAKTHROUGH ON THE OUTPUTS. PINS 8 AND 9 SHOULD BE LEFT OPEN-CIRCUIT WHEN NOT IN USE.

Fig. 1 Pin connections (top)

ABSOLUTE MAXIMUM RATINGS

Supply voltage $\|V_{CC} - V_{EE}\|$	8V
Input voltage $V_{in\ (d.c.)}$	Not greater than the supply voltage in use.
Output current I_{out}	20mA
Max. junction temperature	+150°C
Storage temperature range	−55°C to +175°C

Clock Pulse	Q_1	Q_2	Q_3	Q_4	TTL O/P
1	L	H	H	H	H
2	L	L	H	H	H
3	L	L	L	H	H
4	H	L	L	H	H
5	H	H	L	H	H
6	L	H	H	L	L
7	L	L	H	L	L
8	L	L	L	L	L
9	H	L	L	L	L
10	H	H	L	L	L
11	H	H	H	H	H

Extra state

Table 1 Count sequence

$\overline{PE_1}$	$\overline{PE_2}$	Div Ratio
L	L	11
H	L	10
L	H	10
H	H	10

Table 2 Truth table for control inputs

The maximum possible loop delay for control is obtained if the L→H transition from Q_4 or the H→L transition from $\overline{Q_4}$ is used to clock the stage controlling the ÷10/11. The loop delay is 10 clock periods minus the internal delays of the ÷10/11 circuit.

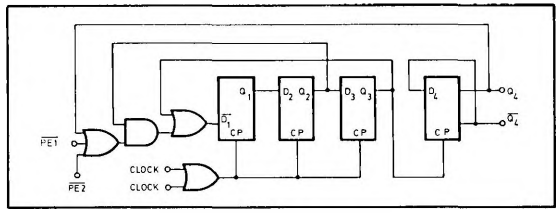


Fig. 2 Logic diagram (positive logic)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb}: −55 C to −125 C (A grade)
−40 C to −85 C (M grade)
0 C to −70 C (B grade)

Supply voltage (see note 1): V_{CC} 0V
V_{EE} −5.2V

Static Characteristics (all SP8640 series devices)

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Clock and $\overline{PE}$ input voltage levels					
V_{INH}	−1.10		−0.81	V	T_{amb} = +25°C,
V_{INL}	−1.85		−1.50	V	see Note 2
Input pulldown resistance, between pins 1, 2, 3, and 16 and V_{EE} (pin 12)		4.3		KΩ	
Output voltage levels					
V_{OH}	−0.85			V	T_{amb} = +25°C,
V_{OL}			−1.50	V	see Note 3. I_{out} (external) = 0mA (There is an internal circuit equivalent to a 2kΩ pulldown resistor on each output)
Power supply drain current		50	65	mA	

NOTES

1. The devices are specified for operation with the power supplies of V_{CC} = 0V and V_{EE} = −5.2V ± 0.25V, which are the normal ECL supply rails. They will also operate satisfactorily with TTL rails of V_{CC} = +5V ± 0.25V and V_{EE} = 0V.
2. The input reference voltage has the same temperature coefficient as ECL III and ECL 10K.
3. The output voltage levels have the same temperature coefficients as ECL II output levels.

Dynamic Characteristics

Characteristic	Type	Value			Units	Conditions
		Min.	Typ.	Max.		
Clock input voltage levels						
V_{INH}	All	−1.10		−0.90	V	T_{amb} = +25°C,
V_{INL}	All	−1.70		−1.50	V	see Note 4
Max. toggle frequency	SP8643	350			MHz	
	SP8642	300			MHz	
	SP8641/7	250			MHz	
	SP8640/6	200			MHz	
Min. frequency with sinewave clock input	All			50	MHz	
Min. slew rate of square wave input for correct operation down to DC	All			100	V/μs	
Propagation delay (clock input to device output)	All		3		ns	ECL Output
Set-up time	All		1.5		ns	See note 5
Release time	All		1.5		ns	See note 6

NOTES

4 The devices are dynamically tested using the circuit shown in Fig. 5. The bias chain has the same temperature coefficient as ECL III and ECL 10K, and therefore tracks the input reference throughout the temperature range. The devices are tested with input amplitudes of 400 and 800 mV p-p about that reference, over the full temperature range.

5. Set-up time is defined as the minimum time that can elapse between a L→H transition of a control input and the next L→H clock pulse transition to ensure that the ÷10 mode is forced by that clock pulse (see Fig. 3).

6. Release time is defined as the minimum time that can elapse between a H→L transition of a control input and the next L→H clock pulse transition to ensure that the ÷11 mode is forced by that clock pulse (see Fig. 4).

7. SP8646, SP8647 TTL output current = 8mA at V_{OL} = +0.5V, measured at +25°C, temperature coefficient = +0.5mV/°C

8. SP8646, SP8647 Q_4 to TTL output delay = 3ns, typical

9. The TTL O/P is a free collector and requires a 2k Ω (typ) pull-up resistor. The current taken by this resistor must be included in the 8mA current in Note 7 above.

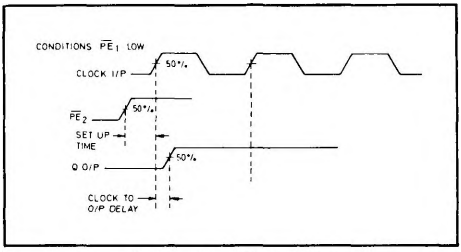


Fig. 3 Set-up timing diagram

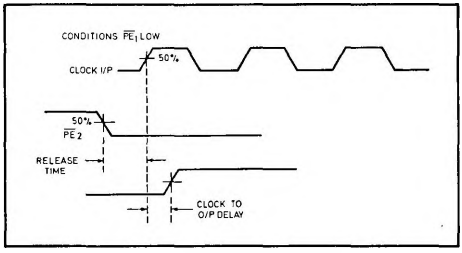


Fig. 4 Release timing diagram

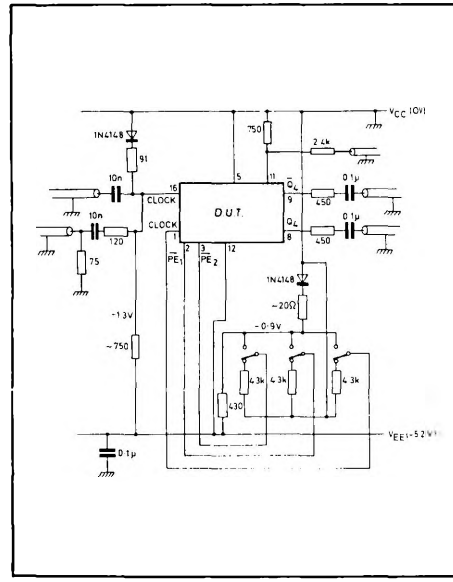


Fig. 5 Test circuit for dynamic measurements

OPERATING NOTES

The SP8640 range of devices are designed to operate in the UHF band and therefore PCB layouts should comply with normal UHF rules, e.g. non-inductive resistors and capacitors should be used, power supply rails decoupled, etc.

All clock and control inputs are compatible with ECL III and ECL 10K throughout the temperature range. However, it is often desirable to capacitively-couple the signal source to the clock, in which case an external bias network is required as shown in Fig. 6.

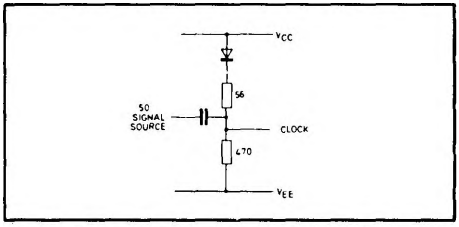


Fig. 6 Recommended input bias configuration for capacitive coupling to a contir uous 50Ω signal source.

The ÷10/11 can be controlled by a TTL fully programmable counter, provided that delays within the loop are kept to a minimum. The outputs and control inputs must therefore interface to TTL. The input TTL to ECL interface is accomplished with two resistors as shown in Fig. 7. The output ECL to TTL interface has been provided on chip in the SP8646/7. A discrete interface may be constructed as shown in Fig. 7. Both output interfaces will operate satisfactorily over the full military temperature range (−55°C to +125°C). The propagation delay through the divider plus the interface and one Schottky TTL gate is approximately 10 ns. At an input frequency of 350 MHz this would only leave about 16 ns for the fully-programmable counter to control the ÷10/11. The loop delay can be increased by extending the ÷10/11 function to, say, ÷20/21 or ÷40/41 (see Application Notes).

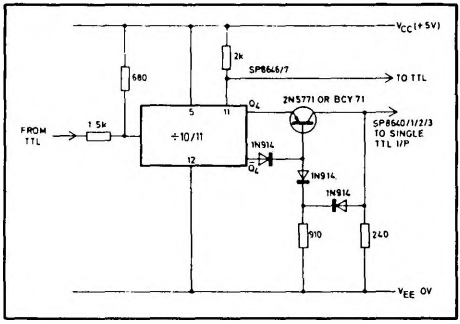


Fig. 7 TTL to ECL and ECL/TTL interfaces (for SP8640 devices and TTL operating from the same supply rails)

The SP8640 device ECL o/ps are compatible with ECL II levels when there is no external load. They can be made compatible with ECL III and ECL 10K with a simple potential dividing network as shown in Fig. 8.

The control and clock inputs are already compatible with ECL III and ECL 10K. The interface circuit of Fig. 8 can be used to increase noise immunity when interfacing from ECL III and ECL 10K outputs at low current levels to ECL III and ECL 10K inputs.

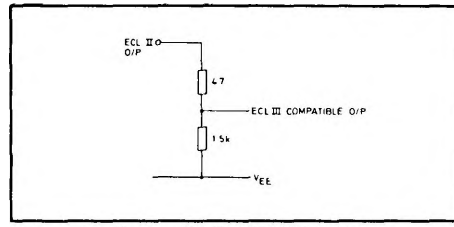


Fig. 8 ECL II to ECL III interface