

UHF DECADE COUNTERS
SP8665B 1.0GHz \div 10 **SP8666B** 1.1GHz \div 10

SP8667B 1.2GHz \div 10

The SP8665/6/7 high speed decade counters operating at an input frequency of up to 1GHz over the temperature range 0°C to +70°C.

The device has a typical power dissipation of 550mW at the nominal supply voltage of 6.8V.

The clock input is biased internally and is coupled to the signal source by a capacitor. The input signal path is completed by an input reference decoupling capacitor which is connected to earth. If no signal is present at the clock input the device will self-oscillate. If this is undesirable it may be prevented by connecting a 15k Ω resistor from the input to V_{EE} (pin 10 to pin 7). This will reduce the input sensitivity of the device by approximately 100mV.

The clock inhibit input is compatible with standard ECL III circuits using a common V_{CC} to the SP8665/6/7. A 6k Ω pulldown resistor is included on the chip. The input should be left open circuit when not in use. The SP8665/6/7 outputs are compatible with standard ECL II circuits. They may be used to drive ECL 10K by the inclusion of two resistors as shown in Fig. 4.

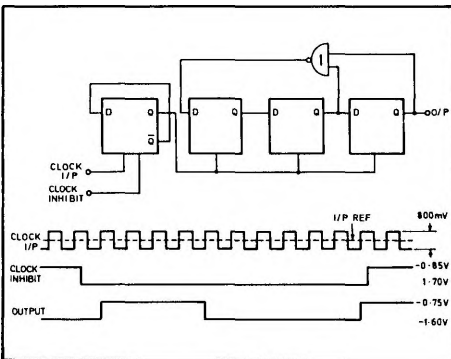


Fig. 2 Logic diagram

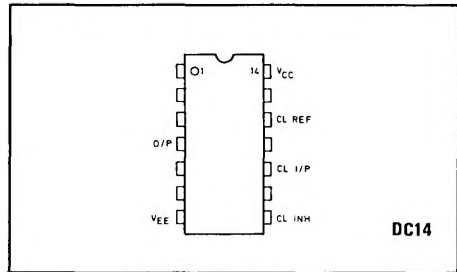


Fig. 1 Pin connections

FEATURES

- Guaranteed operation over large temperature range 0°C to 70°C
- Wide input dynamic range
- Self biasing clock input
- Clock inhibit input for direct gating capability

ABSOLUTE MAXIMUM RATINGS

Power supply voltage V _{CC} - V _{EE}	0V to +10V
Input voltage inhibit input	V _{EE} to V _{CC}
Input voltage CP input	2.5V p-p
Output current	20mA
Operating junction temperature	+150°C
Storage temperature	-55°C to 150°C

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):

Supply voltage	6.8V ± 0.3V
Clock input	AC coupled, self-biasing
Clock inhibit input	ECL III compatible
Output	ECL II compatible
T _{amb}	0°C to +70°C
Supply voltage	V _{CC} = 0V V _{EE} = -6.8V
Clock input voltage	400mV to 1.2V (peak to peak)

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Max. i/p frequency	SP8665	1.0			GHz
	SP8666	1.1			GHz
	SP8667	1.2			GHz
Min. i/p frequency				200	MHz
Min. i/p frequency				100	MHz
Min. slew rate for square wave input				200	V/μsec
Clock i/p impedance		400			Ω
Inhibit input reference level		-1.3			V
Inhibit input pulldown resistor (internal)		6			kΩ
Output pulldown resistor (internal)		3			kΩ
Power supply drain current		80	105		mA

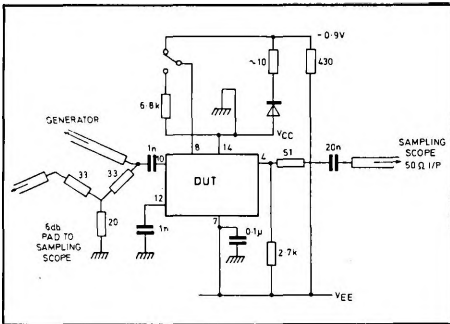


Fig. 3 Test circuit

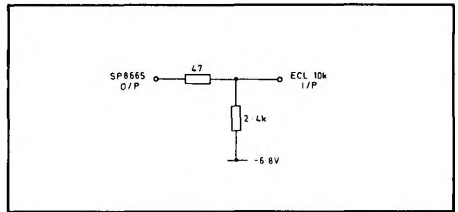


Fig. 4 SP8665 to ECL 10K