PLESSEY
SEMICONDUCTORS

SP 8000 SERIES
HIGH SPEED DIVIDERS

SP 8743 B & M
AC COUPLED UHF PROGRAMMABLE DIVIDER 500 MHz ÷8/9

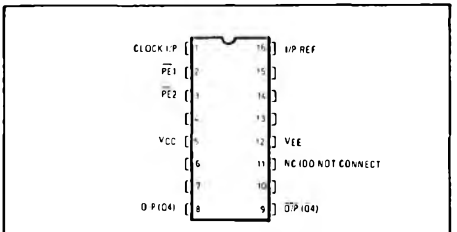
The SP8743M and B are high speed, programmable ÷ 8/9 counters operating at an input frequency of up to 500MHz over the temperature ranges −40°C to +85°C and 0°C to 70°C respectively.

The clock input is biased internally and is coupled to the signal source by a capacitor. The input signal path is completed by an input reference decoupling capacitor which is connected to ground.

The division ratio is controlled by two $\overline{PE}$ inputs. The counter will divide by 8 when either input is in the high state and by 9 when both inputs are in the low state. These inputs are compatible with standard ECL 10K inputs and have the same temperature characteristics. Both inputs have nominal 4.3kΩ internal pulldown resistors.

The true and inverse outputs are compatible with standard ECL II outputs. They may be used to drive ECL 10K circuits by the inclusion of two resistors as shown in Fig. 4.

When using the device as a divide-by-eight prescaler the inverse output (o/p) should be connected to a $\overline{PE}$ input.



NOTE: UNUSED PINS (EXCEPT 8, 9 and 11) MAY BE CONNECTED TO V_{EE}, THIS WILL REDUCE CLOCK BREAKTHROUGH ON THE OUTPUTS.

DG 16
DC 16

Fig. 1 Pin connections

ABSOLUTE MAXIMUM RATINGS

Power supply voltage, $\lvert V_{CC} - V_{EE} \rvert$	0V to +8V
Input voltage PE inputs	0V to V_{CC}
Input voltage CP input	2V p-p
Output current	20mA
Operating junction temperature	+150°C
Storage temperature	−55°C to +150°C

FEATURES

- Operating Temperature Range:
  0°C to 70°C ('B' grade)
  −40°C to +85°C ('M' grade)
- Self Biasing Clock Input
- Wide Input Dynamic Range
- Control Inputs ECL 10K Compatible
- Low Propagation Delay
- True and Inverse Outputs Available

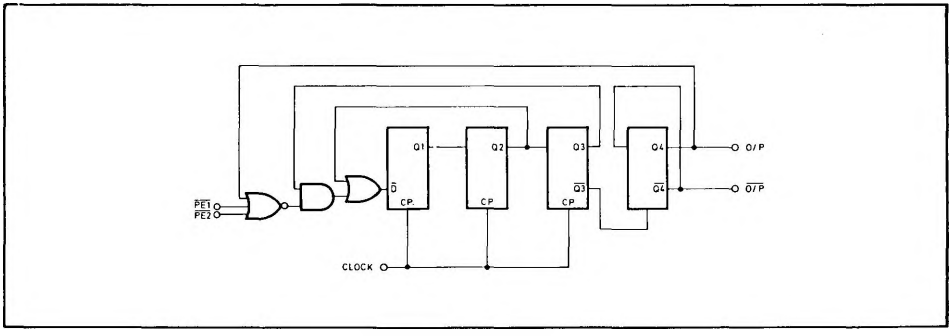


Fig. 2 SP8743 logic diagram

Count Sequence			
Q_1	Q_2	Q_3	Q_4
L	H	H	H
L	L	H	H
H	L	L	L
H	H	L	L
L	H	H	L
L	L	H	L
L	L	L	H ← Extra state
H	L	L	H
H	H	L	H

Division Ratio				
	9	8	8	8
$\overline{PE1}$	L	L	H	H
$\overline{PE2}$	L	H	L	H

ELECTRICAL CHARACTERISTICS

$\overline{PE}$ inputs — ECL 10K compatible
Outputs — ECL II compatible

Test Conditions (unless otherwise stated):
T_{AMB} 0°C to +70°C ('B' grade) −40°C to +85°C ('M' grade)
Supply Voltage V_{CC} = +5.2V ± 0.25V V_{EE} = 0V
Clock Input Voltage 400mV to 800mV p-p

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Max. i/p frequency	500			MHz	V_{CC} = +5.2V
Min. i/p frequency			40		Sinewave Input
Min. Slew rate for square wave input			100	V/μs	
Propagation delay (clock i/p to device o/p)		4		ns	
$\overline{PE}$ input reference level		+3.9		V	V_{CC} = +5.2V, 25°C
Power Supply drain current		45	60	mA	V_{CC} = +5.2V, 25°C
$\overline{PE}$ input pulldown resistors		4.3		kΩ	
Clock i/p impedance (i/p to i/p ref. low freq.)		400		Ω	

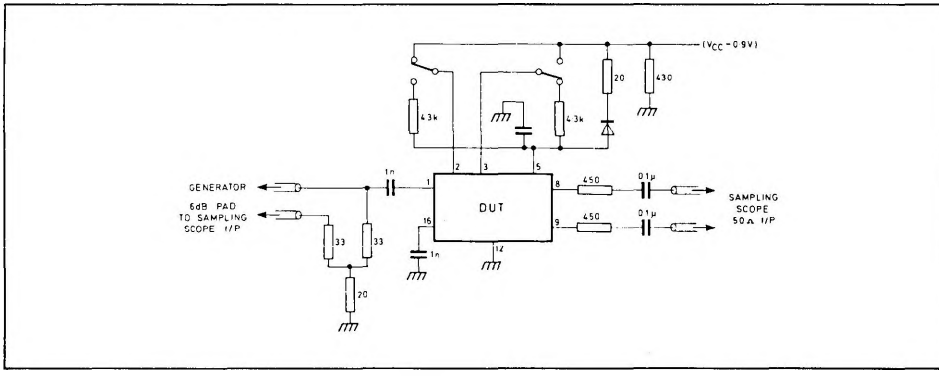


Fig. 3 Test circuit

APPLICATIONS INFORMATION

Interfaces

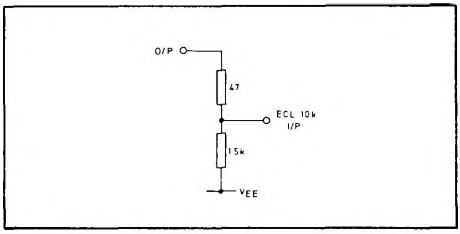


Fig. 4

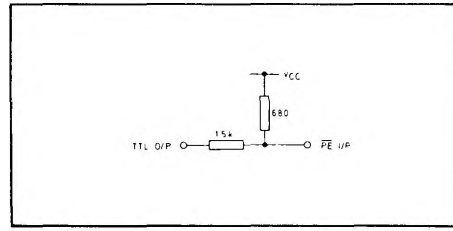


Fig. 5

When operating the SP8743 in a synthesiser loop at 500MHz, the delay time through the programmable divider controlling the SP8743 is approximately 12ns As we believe that this delay would be a severe problem with TTL, we strongly recommend the use of ECL.

The simple passive interface from the output of the SP8743 into ECL 10K logic is defined in Fig. 4.

If TTL is required, the input interface to the $\overline{PE}$ pins, and the output of the SP8743 into TTL, is shown in Fig. 5.

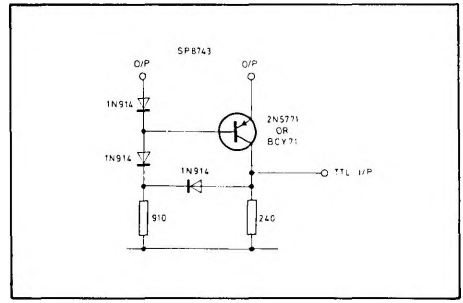


Fig. 6 SP8743 O/P to TTL I/P. Total delay from SP8743 clock I/P to Schottky gate O/P = 15ns typical.

Sub-Systems

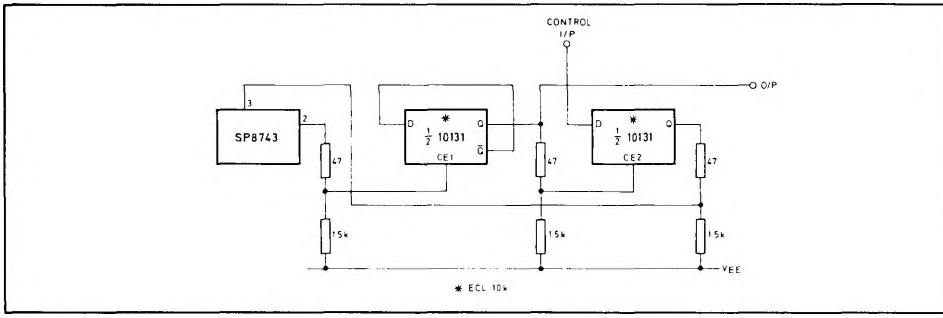


Fig.7 A ÷ 32/33 application. Control loop delay time approx. 56ns.

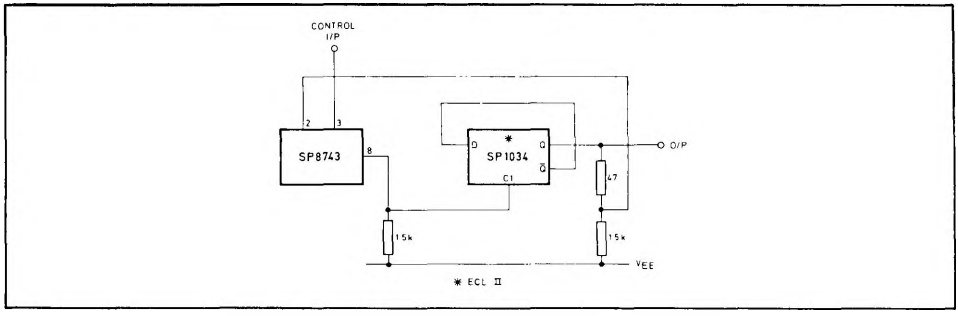


Fig.8 A÷16/17 application. Control loop delay time approx. 24ns using SP1034