PLESSEY
SEMICONDUCTORS

SP8000 SERIES
HIGH SPEED DIVIDERS

SP 8794 A,B & M
÷ 8 CONTROL CIRCUIT FOR 2 - MODULUS DIVIDERS

The SP8794 is a divide by eight counter designed for use with 2-modulus counters. It increases the minimum division ratio of the 2-modulus counter while retaining the same difference in division ratios. Thus a divide by 10 or 11 with the SP8794 becomes a divide by 80 or 81, a divide by 5 or 6 becomes a divide by 40 or 41.

The function is especially useful in low power frequency synthesisers because it can bring the output frequency of the combined 2-modulus counter and SP8794 into the region where CMOS or low power TTL can control the divider.

The device interfaces easily to the SP8000 range of 2-modulus dividers. The control I/Ps are TTL and CMOS compatible and the output is a free collector which, with the addition of a pull-up resistor, interfaces to CMOS and TTL.

The SP8794 is available over three temperature ranges: 0°C to +70°C (SP8794B), −40°C to +85°C (SP8794M) and −55°C to +125°C (SP8794A).

The SP8794 requires supplies of 0V and +5V ± 0.25V

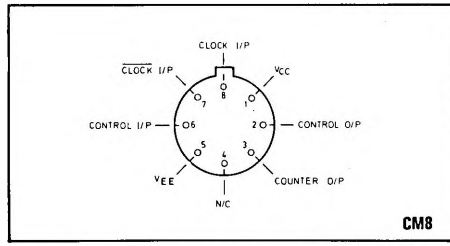

Fig. 1 Pin connections.

FEATURES

- Ultra-Low Power: 40mW
- Full Military Temperature Range
- Direct I/P & O/P Interfacing to CMOS & TTL
- Operates with 500MHz ÷ 10/11

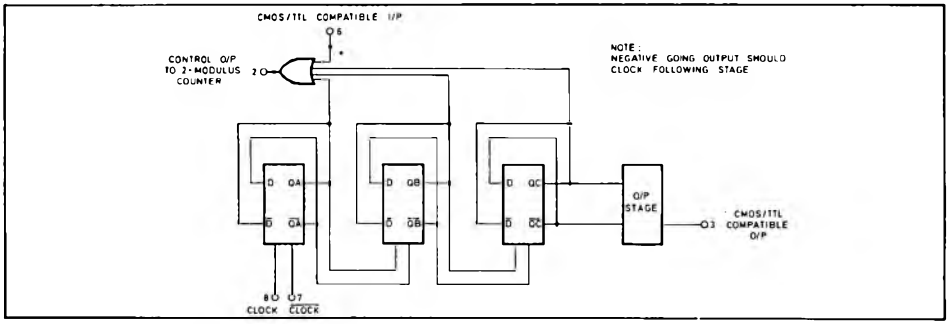

Fig. 2 Logic diagram.

ABSOLUTE MAXIMUM RATINGS

Power supply voltage $\lvert V_{CC} - V_{EE} \rvert$	8V
DC input voltage	Not greater than supply
AC input voltage	2.5Vp-p
Output bias voltage	12V
Control input bias voltage	12V
Operating juntion temperature	+150°C
Storage temp. range	−55°C to 150°C

APPLICATION

- Frequency Synthesisers

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb}: 'A' grade −55°C to +125°C
'B' grade 0°C to +70°C
'M' grade −40°C to +85°C

V_{CC} = +5V ±5%

V_{EE} = 0V

Clock input voltage with double complementary drive to CLOCK and $\overline{CLOCK}$ = 300mV to 1V p-p.

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Dynamic					
Toggle frequency	120			MHz	SP8794 as a prescaler (see note 1)
	40			MHz	SP8794 controlling a 2-modulus divider (see note 1)
Min. toggle frequency with sinewave input			20	MHz	See note 2
Min. toggle frequency with square wave input	0			Hz	Slew rate > 50V/μs
Clock to O/P delay (O/P −ve going)		18		ns	
Clock to O/P delay (O/P +ve going)		32		ns	
Control I/P to control O/P delay (O/P −ve going)		20		ns	10kΩ pulldown on O/P, see note 5
Control I/P to control O/P delay (O/P +ve going)		10		ns	10kΩ pulldown on O/P, see note 5
Control I/P to control O/P delay (O/P −ve going)		12		ns	4.3kΩ pulldown on O/P, see note 6
Control I/P to control O/P delay (O/P +ve going)		9		ns	4.3kΩ pulldown on O/P, see note 6
Clock to control O/P delay (O/P −ve going)		30		ns	10kΩ pulldown on O/P, see note 5
Clock to control O/P delay (O/P +ve going)		16		ns	10kΩ pulldown on O/P, see note 5
Clock to control O/P delay (O/P −ve going)		21		ns	4.3kΩ pulldown on O/P, see note 6
Clock to control O/P delay (O/P +ve going)		16		ns	4.3kΩ pulldown on O/P, see note 6
Static					
Control I/P voltage level					
High state	3.5		10	V	See note 3
Low state	0		1.5	V	
Output voltage level					
V_{OL}			0.4	V	Sink current = 6.0mA
V_{OH} (see note 4)			12	V	See note 4
Input impedance		1.6		kΩ	f_{in} = 0Hz
I/P bias voltage (CLOCK & $\overline{CLOCK}$)					
Power supply drain current					

NOTES

1. The maximum frequency of operation is in excess of 120MHz when the SP8794 is used as a prescaler. The limitation on its maximum operating frequency is the saturating output stage. When the SP8794 is used as a controller for a 2-modulus device its internal delays do not permit operation at frequencies above 40MHz.
2. The device will normally be driven from a 2-modulus divider which will have fast output edges. Hence, there is normally no input slew rate problem.
3. TTL devices require a pull-up resistor to ensure the required minimum of 3.5V. Note that the device can interface from 10V CMOS with no additional components.
4. V_{OH} will be the supply voltage that the output pull-out resistor is connected to. This voltage should not exceed 12V.
5. The 10kΩ pulldown is the value of the input pulldown of the SP8695, with which the SP8794 can be used.
6. The 4.3kΩ pulldown is the value of the input pulldown of all the SP8640 series ÷ 10/11 devices, the SP8740 & SP8745 ÷ 5/6, the SP8741 & SP8746 ÷ 6/7 and the SP8743 ÷ 8/9, with which the SP8794 can be used.

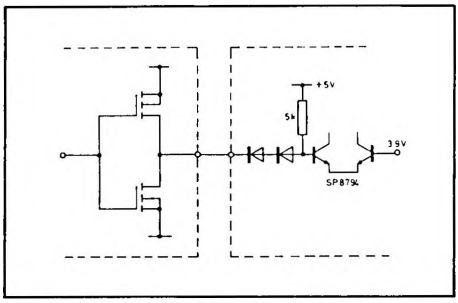

Fig. 3 CMOS and TTL compatible control I/P.

TRUTH TABLE	
Control I/P	Div. Ratio with ÷ 10/11
0	81
1	80

Max input frequency to combination = 200MHz (min.).
Power consumption of combination = 120mWtyp.
Time available to control the ÷ 80/81
= 80 clock periods minus delays through dividers
≅ 740ns (f_{in} = 100MHz)

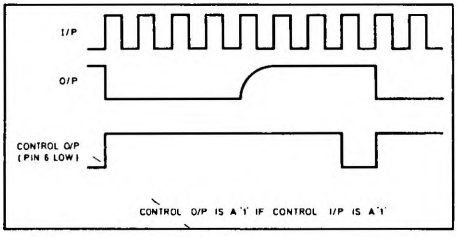

Fig. 4 SP8794 waveforms

APPLICATION NOTES

The SP8794 extends the division ratio of 2-modulus counters while retaining the same 2-modulus resolution. A typical application to give a ÷ 80/81 function is shown in Fig. 5. In this basic form, however, the devices will self-oscillate if no input signal source is present, This may be prevented by using one of the arrangements shown in Fig. 6.

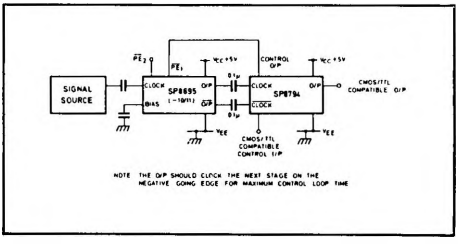

Fig. 5 SP8794 with SP8695 connected to give a low power ÷ 80/81

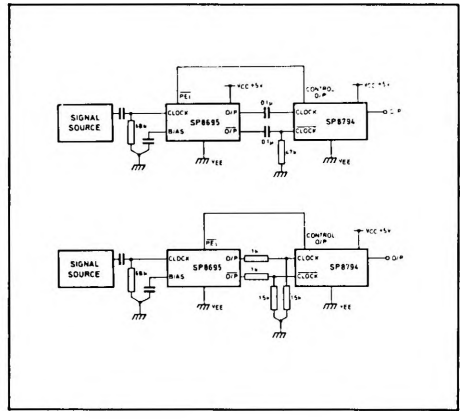

Fig. 6 Methods of preventing self-oscillation.