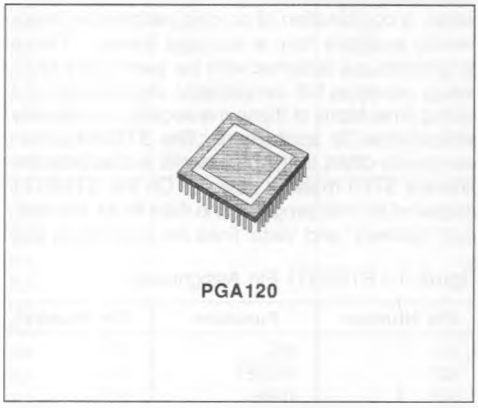
SGS-THOMSON MICROELECTRONICS

# ST63RT1

## 8-BIT HCMOS UNIVERSAL ROMLESS MCU FOR TV APPLICATIONS

**ADVANCE DATA**

- UNIVERSAL ST63XX FAMILY EMULATION CHIP
- 8-BIT ARCHITECTURE
- STATIC HCMOS OPERATION
- 4.5 TO 5.5 V SUPPLY OPERATING RANGE
- 4MHZ OR 8MHZ CLOCK OPTIONS
- PROGRAM ROM : 16K BYTES EXTERNAL
- DATA ROM : USER SELECTABLE SIZE
- DATA RAM : 256 BYTES
- DATA EEPROM : 128 BYTES
- 120 CERAMIC PGA PACKAGE
- 14/15 BIT PHASE LOCKED LOOP PERIPHERAL (PLL)
- 14 BIT VOLTAGE SYNTHESIS TUNING PERIPHERAL (VS)
- ON-CHIP 5 LINES BY 15 COLUMNS ON-SCREEN-DISPLAY GENERATOR (OSD)
- THE ON-CHIP OSD CAN BE DISABLED ALLOWING DIRECT DRIVING OF AN EXTERNAL OSD GENERATOR (ST63RS1).
- 24 SOFTWARE PROGRAMMABLE GENERAL PURPOSE INPUTS/OUTPUTS, INCLUDING 8 DIRECT LED DRIVING OUTPUTS
- TWO TIMERS EACH INCLUDING AN 8-BIT COUNTER WITH A 7-BIT PROGRAMMABLE PRESCALER
- DIGITAL WATCHDOG FUNCTION
- SERIAL PERIPHERAL INTERFACE (SPI) SUPPORTING S-BUS/$I^2C$BUS AND STANDARD SERIAL PROTOCOLS
- FOUR 6-BIT PWM D/A CONVERTERS
- AFC A/D CONVERTER WITH 0.5V RESOLUTION
- INFRARED SIGNAL PRE-PROCESSOR



PGA120

- FOUR INTERRUPT VECTORS (IR, Timer 1 & 2, OSD VSYNC)
- ON-CHIP CLOCK OSCILLATOR
- ON-BOARD POWER-ON RESET CIRCUITRY
- ALL ROM TYPES ARE SUPPORTED BY PIN-TO-PIN PIGGYBACK VERSIONS.
- BYTE EFFICIENT INSTRUCTION SET
- BIT TEST AND JUMP INSTRUCTIONS
- WAIT, STOP AND BIT MANIPULATION INSTRUCTIONS
- 1.625µs TCYCLE (8.0 MHz clock)
- TRUE LIFO 6-LEVEL STACK
- THE DEVELOPMENT TOOL OF THE ST63XX MICROCONTROLLERS CONSISTS OF THE EMST63-HW/TVS EMULATION AND DEVELOPMENT SYSTEM CONNECTED VIA A STANDARD RS232 SERIAL LINE TO AN MS-DOS™ PC.

## GENERAL DESCRIPTION

The ST63RT1 universal romless device is the emulation device of the 8-bit HCMOS ST63XX MCU family, a series of devices specially oriented to TV applications. Different packages and configurations are available to offer different performance/cost tradeoffs. All ST63XX members are based on a building block approach: to a common Core is associated a combination of on-chip peripherals (macrocells) available from a standard library. These peripherals are designed with the same Core technology providing full compatibility, short design and testing time. Many of these macrocells are specially dedicated to TV applications. The ST63RT1 romless device offers all the macrocells available on the different ST63 masked devices. On the ST63RT1 instead of on-chip program and data ROM, the relevant "address" and "data" lines are lead out so that an external memory can be addressed. The addressing capability of this device is 16K; in addition the on-chip OSD of the ST63RT1 can be disabled and an external OSD generator (ST63RS1) can be addressed to allow the generation of customized on-screen character sets.

The macrocells of the ST63RS1 are: two 8-bit counter with a 7-bit programmable prescaler (Timer), a Digital Watchdog Timer, a Serial Peripheral Interface (SPI), a 6-Bit PWM D/A Converter, an AFC A/D converter with 0.5V resolution, a 14/15 bit Phase Locked Loop peripheral (PLL), a 5 lines by 15 columns On-screen display generator (OSD) and a 14 bit Voltage synthesis tuning peripheral (VS). In addition 128 bytes of on-chip EEPROM are available.

**Figure 1 :** ST63RT1 Pin Assignment.

| Pin Number | Function | Pin Number | Function | Pin Number | Function |
|---|---|---|---|---|---|
| A1 | NC | F1 | PC4 | L1 | NC |
| A2 | RESET | F2 | IDB4 | L2 | NC |
| A3 | IDB6 | F3 | PC3/BLK | L3 | NC |
| A4 | PA2 | F4 | NA | L4 | OUT1 |
| A5 | IDB7 | F5 | NA | L5 | DA4 |
| A6 | AD0 | F6 | NA | L6 | AD13 |
| A7 | AD1 | F7 | NA | L7 | AD8 |
| A8 | D3 | F8 | NA | L8 | AD5 |
| A9 | D2 | F9 | NA | L9 | CDEDLD |
| A10 | D0 | F10 | NA | L10 | BSW3 |
| A11 | PA5 | F11 | PB0 | L11 | NC |
| A12 | VDD | F12 | PB1 | L12 | IAB3 |
| A13 | NC | F13 | PB2/VSYN | L13 | KBY0 |
| B1 | NC | G1 | PC7/B | M1 | NC |
| B2 | NC | G2 | PC5/R | M2 | NC |
| B3 | NC | G3 | PC6/G | M3 | DA1 |
| B4 | PA0 | G4 | NA | M4 | DA3 |
| B5 | PA3 | G5 | NA | M5 | VDD |
| B6 | CE | G6 | NA | M6 | AD10 |
| B7 | D6 | G7 | NA | M7 | AD9 |
| B8 | D4 | G8 | NA | M8 | AD6 |
| B9 | D1 | G9 | NA | M9 | AD2 |
| B10 | PA4 | G10 | NA | M10 | BSW0 |
| B11 | PA6 | G11 | PB4 | M11 | NC |
| B12 | NC | G12 | PB5/SCL | M12 | NC |
| B13 | NC | G13 | PB3/HSYN | M13 | NC |

**Figure 1 :** ST63RT1 Pin Assignment - Cont'ed

| Pin Number | Function | Pin Number | Function | Pin Number | Function |
|---|---|---|---|---|---|
| C1 | NC | H1 | PLLIN | N1 | NC |
| C2 | NC | H2 | IDB3 | N2 | IDB0 |
| C3 | NC | H3 | PLLOUT | N3 | DA2 |
| C4 | OSCOUT | H4 | NA | N4 | IAB5 |
| C5 | PA1 | H5 | NA | N5 | AD12 |
| C6 | VSS | H6 | NA | N6 | AD11 |
| C7 | D7 | H7 | NA | N7 | IAB4 |
| C8 | D5 | H8 | NA | N8 | AD7 |
| C9 | IAB2 | H9 | NA | N9 | AD4 |
| C10 | PA7 | H10 | NA | N10 | AD3 |
| C11 | NC | H11 | VSS | N11 | BSW1 |
| C12 | NC | H12 | PB7/SEN | N12 | BSW2 |
| C13 | NC | H13 | PB6/SDA | N13 | NC |
| D1 | PC0 | J1 | VS | | |
| D2 | IDB5 | J2 | IDB2 | | |
| D3 | NC | J3 | VSS | | |
| D4 | NA | J4 | NA | | |
| D5 | NA | J5 | NA | | |
| D6 | NA | J6 | NA | | |
| D7 | NA | J7 | NA | | |
| D8 | NA | J8 | NA | | |
| D9 | NA | J9 | NA | | |
| D10 | NA | J10 | NA | | |
| D11 | NC | J11 | KBY2 | | |
| D12 | NC | J12 | OSDOSCIN | | |
| D13 | TEST | J13 | OSDOSCO | | |
| E1 | PC2-ON/$\overline{OFF}$ | K1 | IRIN | | |
| E2 | PC1 | K2 | IDB1 | | |
| E3 | OSCIN | K3 | NC | | |
| E4 | NA | K4 | NA | | |
| E5 | NA | K5 | NA | | |
| E6 | NA | K6 | NA | | |
| E7 | NA | K7 | NA | | |
| E8 | NA | K8 | NA | | |
| E9 | NA | K9 | NA | | |
| E10 | NA | K10 | NA | | |
| E11 | PDEDLD | K11 | NA | | |
| E12 | IAB1 | K12 | KBY1 | | |
| E13 | AFC | K13 | IAB0 | | |

**NC: Not Connected**

**NA: Not Available**

**Figure 2 :** Frequency Synthesis TV System with External PLL.

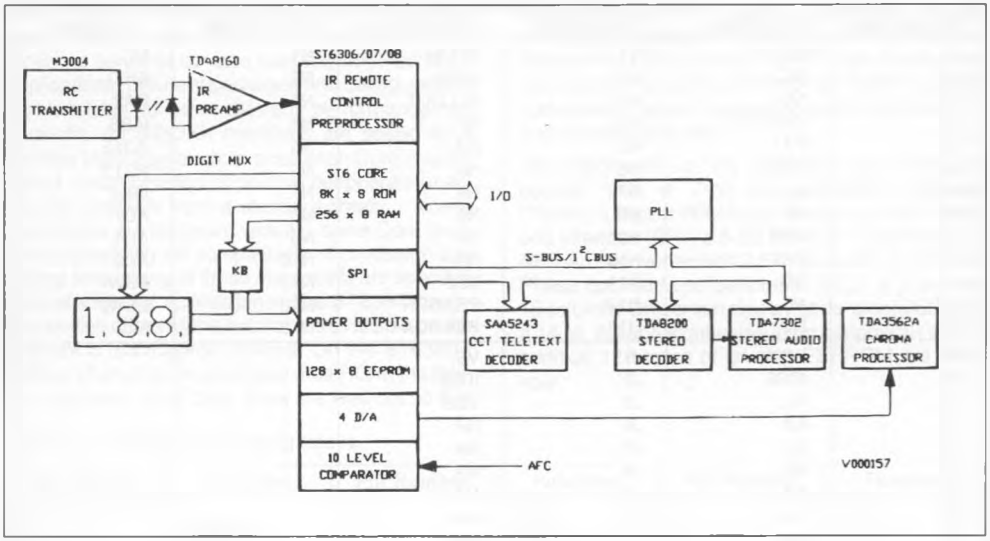



**Figure 3 :** Frequency Synthesis TV System with On-chip PLL and OSD.

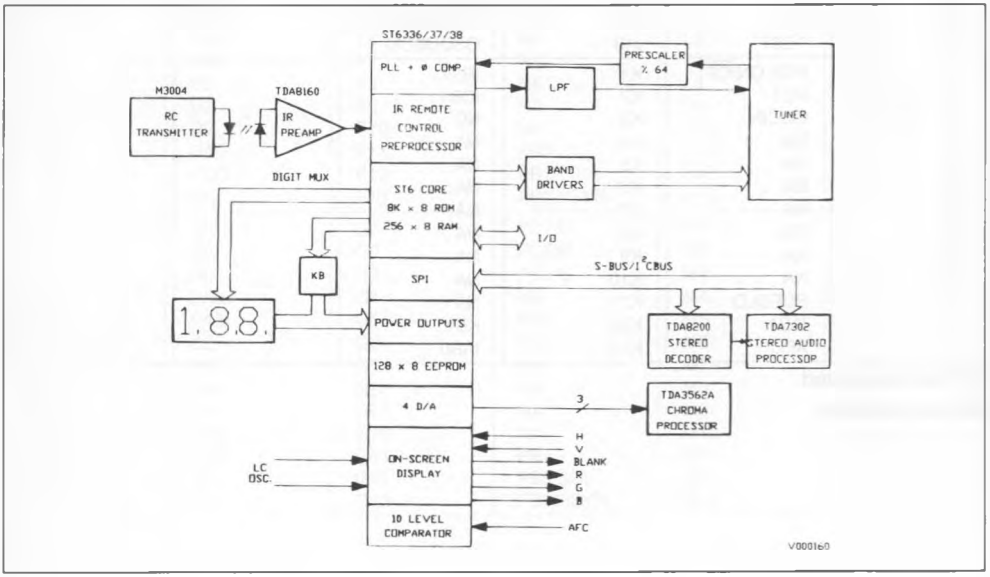


**Figure 4** : Voltage Synthesis TV System with On-chip OSD.

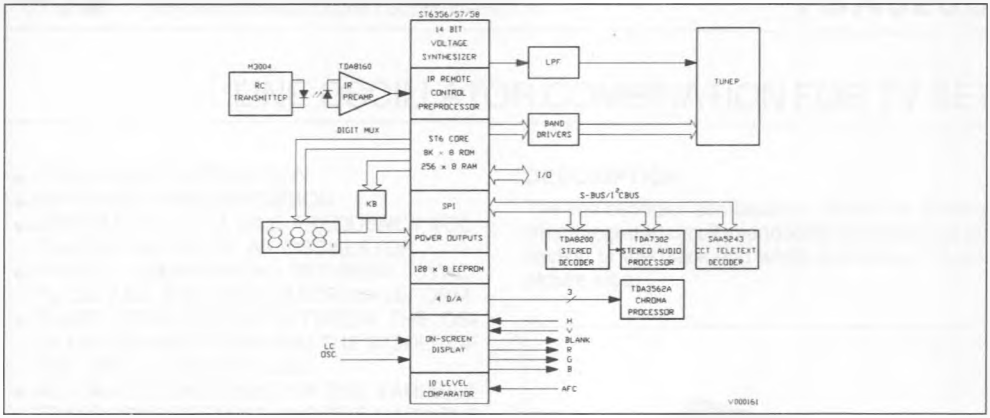



**Figure 5** : ST63RT1 - ST63RS1 (OSD Generator) System Description.