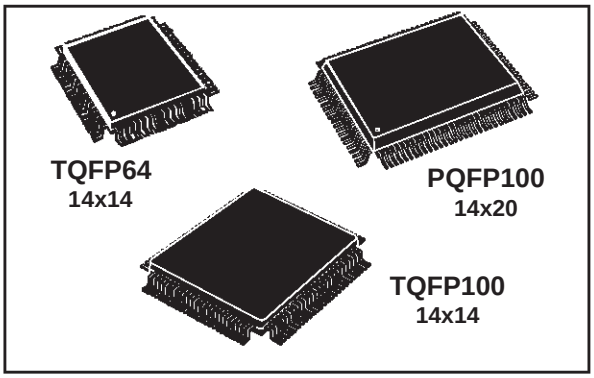
ST92F124/ST92F150/ST92F250

8/16-BIT SINGLE VOLTAGE FLASH MCU FAMILY WITH RAM, E^3 TM(EMULATED EEPROM), CAN 2.0B AND J1850 BLPD

DATA BRIEFING

- **Memories**
  - Internal Memory: Single Voltage FLASH up to 256 Kbytes, RAM up to 8Kbytes, 1K byte E^3 TM (Emulated EEPROM)
  - In-Application Programming (IAP)
  - 224 general purpose registers (register file) available as RAM, accumulators or index pointers
- **Clock, Reset and Supply Management**
  - Register-oriented 8/16 bit CORE with RUN, WFI, SLOW, HALT and STOP modes
  - 0-24 MHz Operation (Int. Clock), 4.5-5.5 V range
  - PLL Clock Generator (3-5 MHz crystal)
  - Minimum instruction time: 80 ns (25 MHz int. clock)
- **Interrupt Management**
  - 80, 77 or 48 I/O pins (depending on device)
  - 4 external fast interrupts + 1 NMI
  - Up to 16 pins programmable as wake-up or additional external interrupt with multi-level interrupt handler
- **Timers**
  - 16-bit Timer with 8-bit Prescaler, and Watchdog Timer (activated by software or by hardware)
  - 16-bit Standard Timer that can be used to generate a time base independent of PLL Clock Generator
  - Two 16-bit independent Extended Function Timers (EFTs) with Prescaler, 2 Input Captures and two Output Compares (100-pin devices only)
  - Two 16-bit Multifunction Timers, with Prescaler, 2 Input Captures and two Output Compares
- **Communication Interfaces**
  - Serial Peripheral Interface (SPI) with Selectable Master/Slave mode
  - One Multiprotocol Serial Communications Interface with asynchronous and synchronous capabilities
  - One asynchronous Serial Communications Interface (on 100-pin versions only)
  - J1850 Byte Level Protocol Decoder (JBLPD) (on F150J versions only)



  - One or two full I C multiple Master/Slave Interfaces supporting Access Bus
  - One or two CAN 2.0B (150 version only) Active interfaces with:
    - Up to 1 MBit/s communication speed
    - 3 Transmit Mailboxes with priority configuration by software
    - Enhanced Filtering mechanism
    - 2 prioritized FIFO receive schemes
    - Time-Triggered Communication support
- DMA controller for reduced processor overhead
- 10-bit Analog to Digital Converter allowing up to 16 input channels on 100-pin devices or 8 input channels on 64-pin devices
- **Instruction Set**
  - Rich Instruction Set with 14 Addressing Modes
  - Division-by-zero trap generation
- **Development Tools**
  - Versatile Development Tools, including Assembler, Linker, C-Compiler, Source Level Debugger, Real Time Operating System (OSEK OS, CMX) and CAN drivers
  - Hardware Emulator, Flash Programming Boards

DEVICE SUMMARY

Features	ST92F124R9	ST92F150C(R/V)1	ST92F150JV1	ST92F150JDV1	ST92F250CV2
FLASH - bytes	60K	128K			256K
RAM - bytes	2K	4K		6K	8K
E^3 TM - bytes	1K				
Timers	2 MFT, STIM, WD	2 MFT, 0/2 EFT, STIM, WD	2 MFT, 2 EFT, STIM, WD		
Serial Interface	SCI, SPI, I C	1/2 SCI, SPI, I C	2 SCI, SPI, 2 I C		
ADC	8 x 10 bits	8/16 x 10 bits	16 x 10 bits		
Network Interface	-	CAN	J1850	2 CAN, J1850	CAN
Temp. Range	-40^0C to 85^0 C or -40^0 C to 125^0 C				
Packages	TQFP64	P/TQFP100 and TQFP64	PQFP100	P/TQFP100	

Rev. 1.1

1 GENERAL DESCRIPTION

1.1 INTRODUCTION

The ST92F124/F150/F250 microcontroller is developed and manufactured by STMicroelectronics using a proprietary n-well HCMOS process. Its performance derives from the use of a flexible 256-register programming model for ultra-fast context switching and real-time event response. The intelligent on-chip peripherals offload the ST9 core from I/O and data management processing tasks allowing critical application tasks to get the maximum use of core resources. The new-generation ST9 MCU devices now also support low power consumption and low voltage operation for power-efficient and low-cost embedded systems.

1.1.1 ST9+ Core

The advanced Core consists of the Central Processing Unit (CPU), the Register File, the Interrupt and DMA controller, and the Memory Management Unit. The MMU allows a single linear address space of up to 4 Mbytes.

Four independent buses are controlled by the Core: a 22-bit memory bus, an 8-bit register data bus, an 8-bit register address bus and a 6-bit interrupt/DMA bus which connects the interrupt and DMA controllers in the on-chip peripherals with the core.

This multiple bus architecture makes the ST9 family devices highly efficient for accessing on and off-chip memory and fast exchange of data with the on-chip peripherals.

The general-purpose registers can be used as accumulators, index registers, or address pointers. Adjacent register pairs make up 16-bit registers for addressing or 16-bit processing. Although the ST9 has an 8-bit ALU, the chip handles 16-bit operations, including arithmetic, loads/stores, and memory/register and memory/memory exchanges.

The powerful I/O capabilities demanded by microcontroller applications are fulfilled by the ST92F150/F124 with 48 (64-pin devices) or 77 (100-pin devices) I/O lines dedicated to digital Input/Output and with 80 I/O lines by the ST92F250. These lines are grouped into up to ten 8-bit I/O Ports and can be configured on a bit basis under software control to provide timing, status signals, an address/data bus for interfacing to the external memory, timer inputs and outputs, analog inputs, external interrupts and serial or parallel I/O. Two memory spaces are available to support this wide range of configurations: a combined Program/ Data Memory Space and the internal Register File, which includes the control and status registers of the on-chip peripherals.

1.1.2 External Memory Interface

100-pin devices have a 22-bit external address bus allowing them to address up to 4M bytes of external memory. 64-pin devices have an 11-bit external address bus for addressing up to 2K bytes.

1.1.3 On-chip Peripherals

Two 16-bit Multifunction Timers, each with an 8 bit Prescaler and 12 operating modes allow simple use for complex waveform generation and measurement, PWM functions and many other system timing functions by the usage of the two associated DMA channels for each timer.

On 100-pin devices, two Extended Function Timers provide further timing and signal generation capabilities.

A Standard Timer can be used to generate a stable time base independent from the PLL.

An I^2C interface (two in the ST92F250) provides fast I^2C and Access Bus support.

The SPI is a synchronous serial interface for Master and Slave device communication. It supports single master and multimaster systems.

A J1850 Byte Level Protocol Decoder is available (on some devices only) for communicating with a J1850 network.

The bxCAN (basic extended) interface supports 2.0B Active protocol. It has 3 transmit mailboxes, 2 independent receive FIFOs and 8 filters.

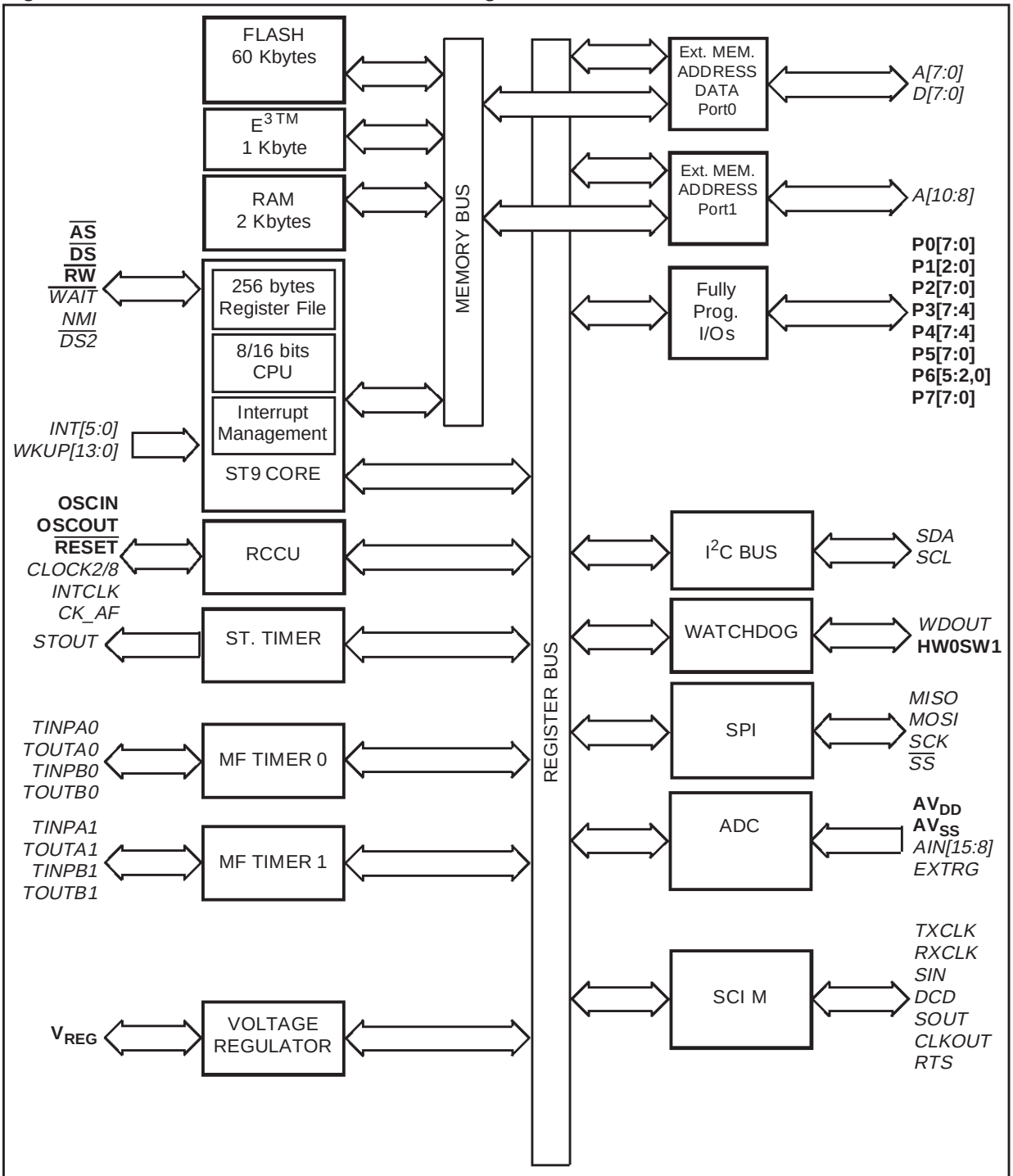
In addition, there is an 16 channel Analog to Digital Converter with integral sample and hold, fast conversion time and 10-bit resolution. In the 64-pin version only 8 input channels are available.

There is one Multiprotocol Serial Communications Interface with an integral generator, asynchronous and synchronous capability (fully programmable format) and associated address/wake-up option, plus two DMA channels.

On some devices, there is an additional asynchronous Serial Communications interface.

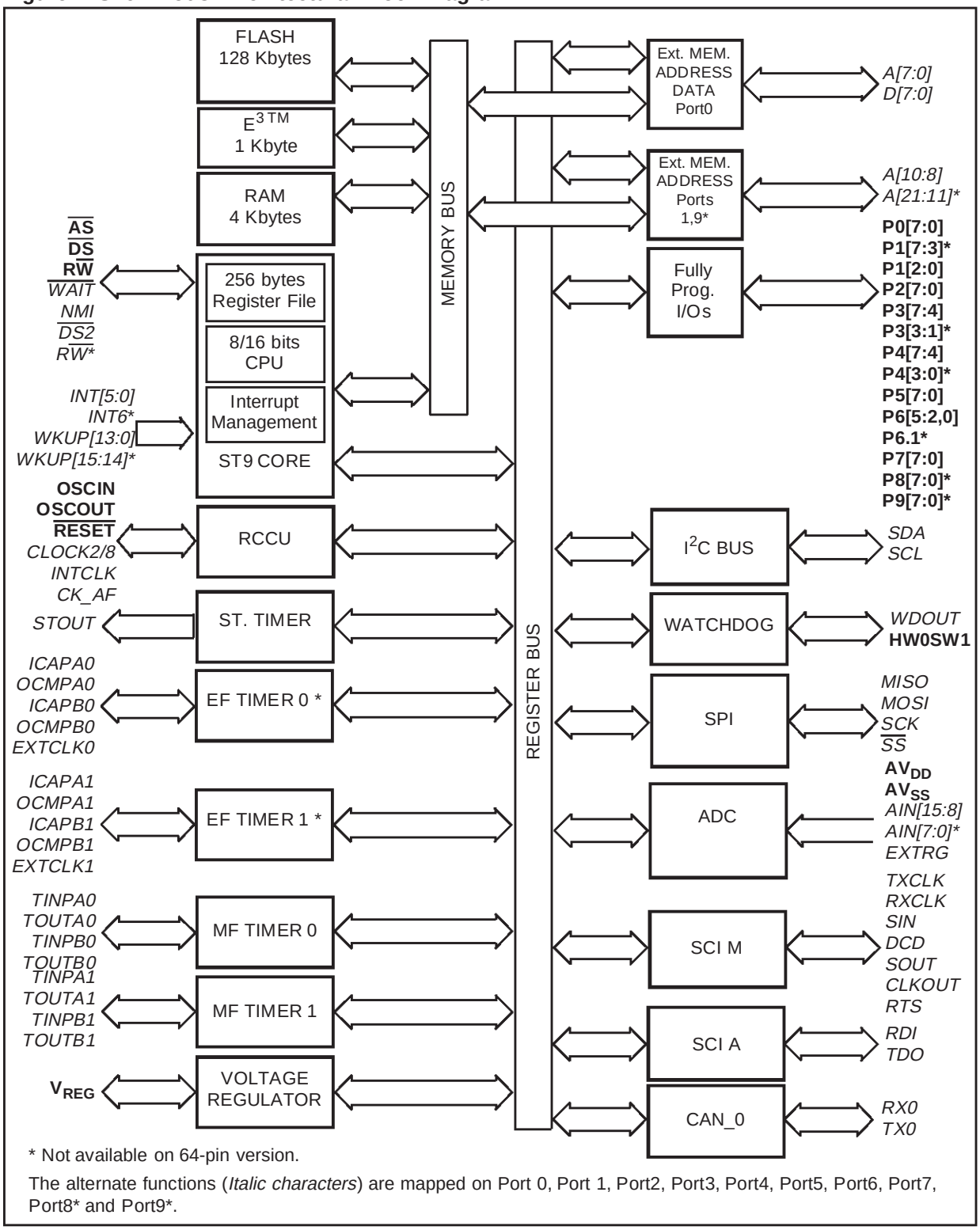
Finally, a programmable PLL Clock Generator allows the usage of standard 3 to 5 MHz crystals to obtain a large range of internal frequencies up to 25MHz. Low power Run (SLOW), Wait For Interrupt, low power Wait For Interrupt, STOP and HALT modes are also available.

Figure 1. ST92F124R9: Architectural Block Diagram



The alternate functions (*Italic characters*) are mapped on Port 0, Port 1, Port2, Port3, Port4, Port5, Port6 and Port7.

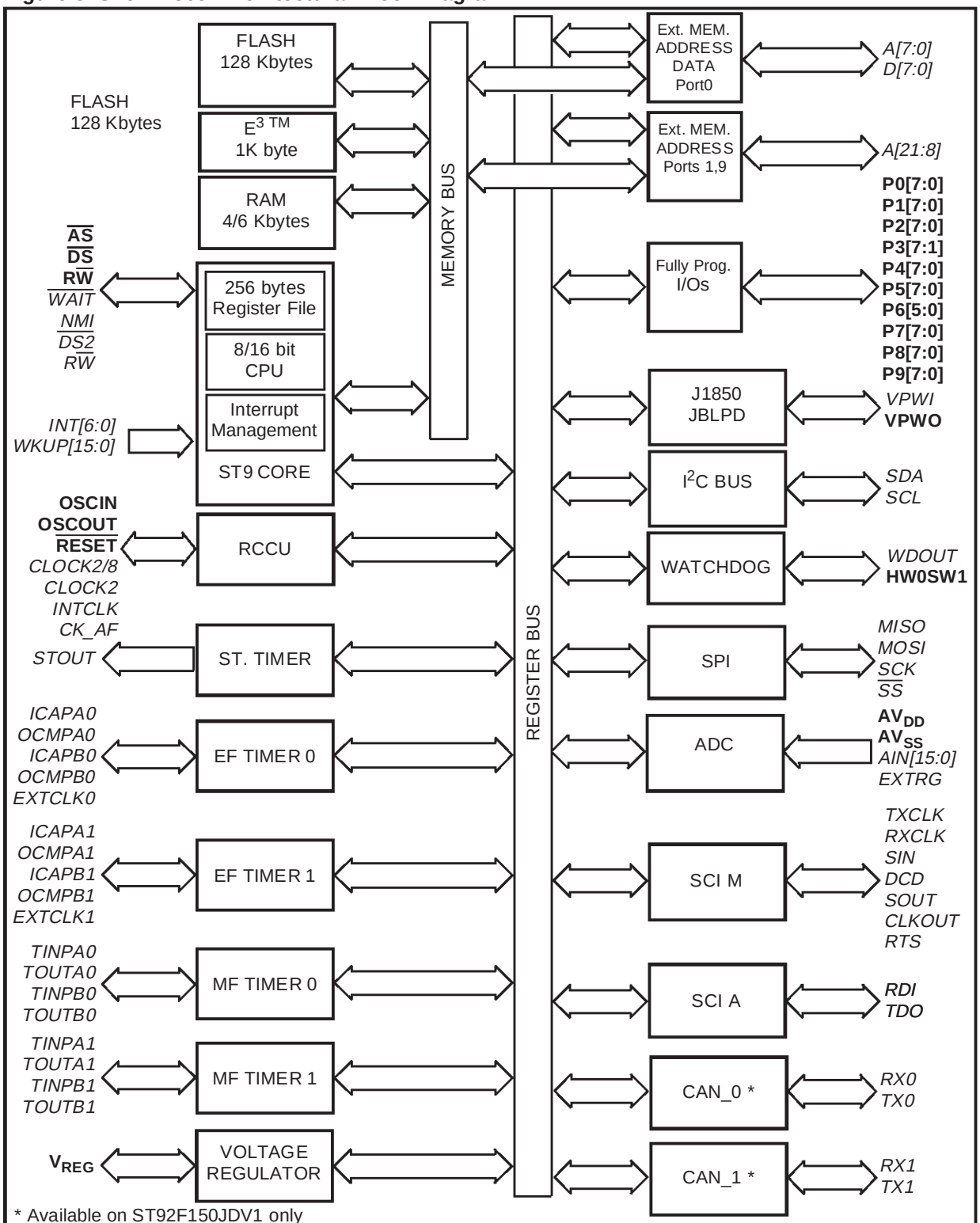
Figure 2. ST92F150C: Architectural Block Diagram



* Not available on 64-pin version.

The alternate functions (*Italic characters*) are mapped on Port 0, Port 1, Port2, Port3, Port4, Port5, Port6, Port7, Port8* and Port9*.

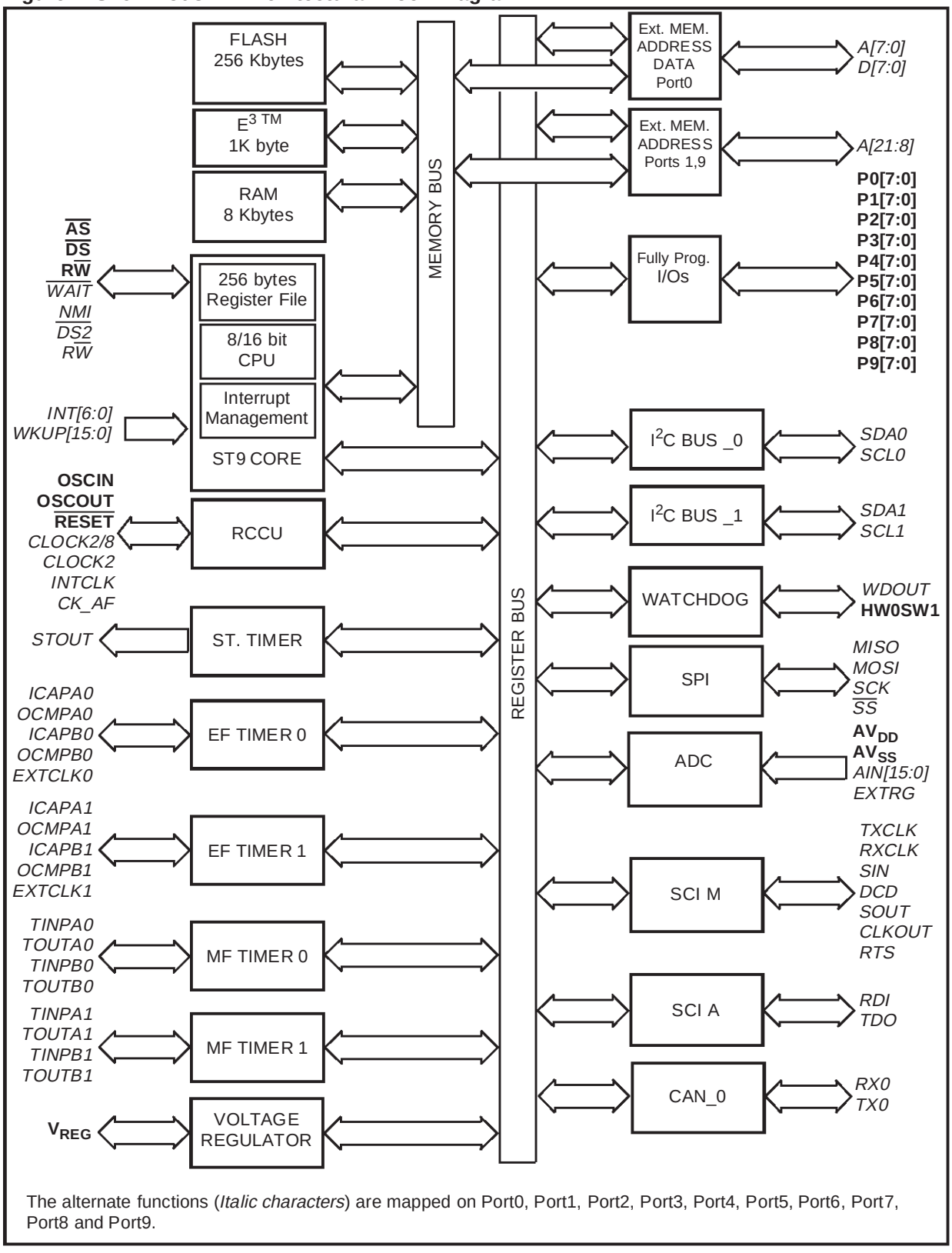
Figure 3. ST92F150J: Architectural Block Diagram



* Available on ST92F150JDV1 only

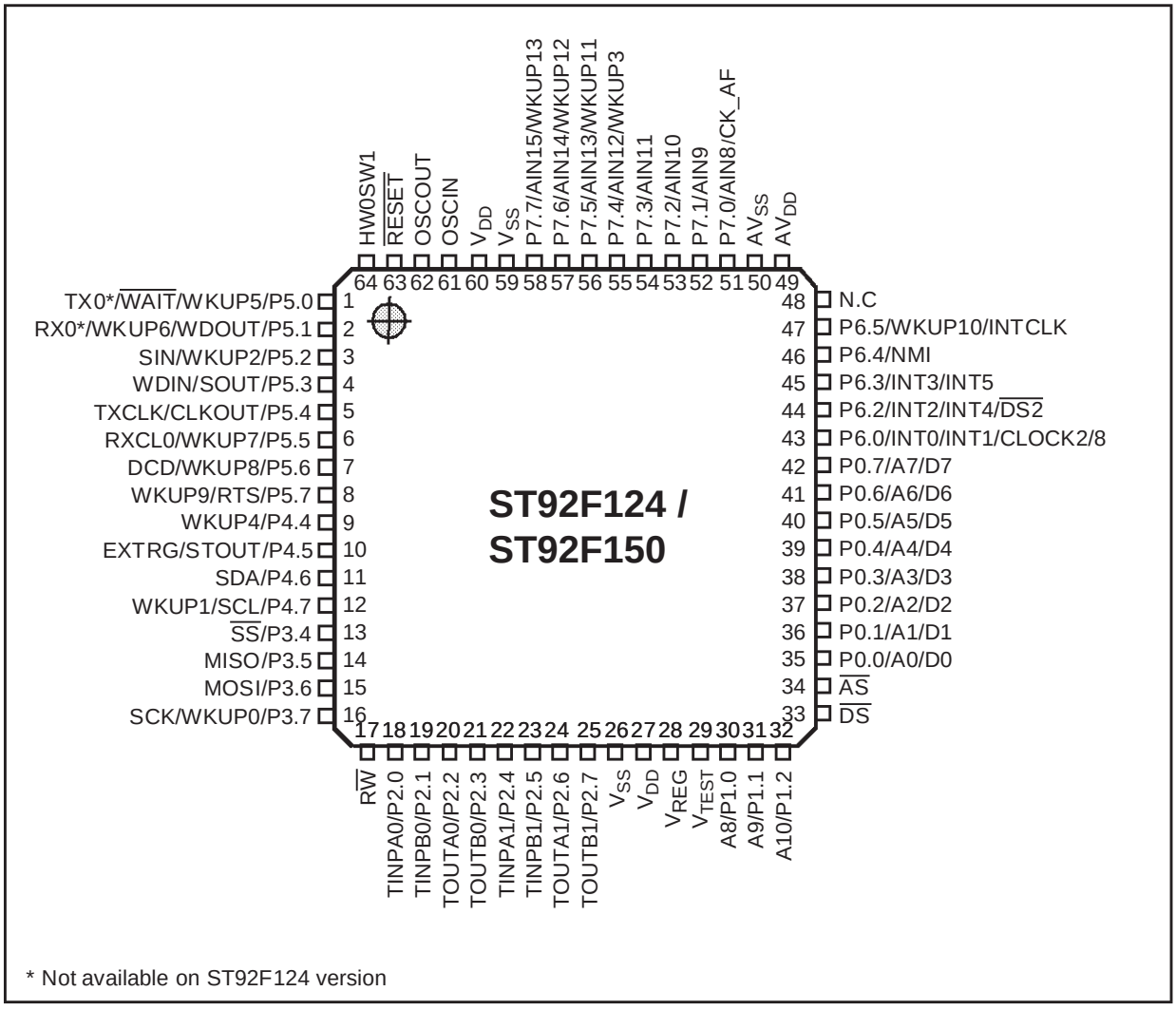
The alternate functions (*Italic characters*) are mapped on Port0, Port1, Port2, Port3, Port4, Port5, Port6, Port7, Port8 and Port9.

Figure 4. ST92F250CV2: Architectural Block Diagram



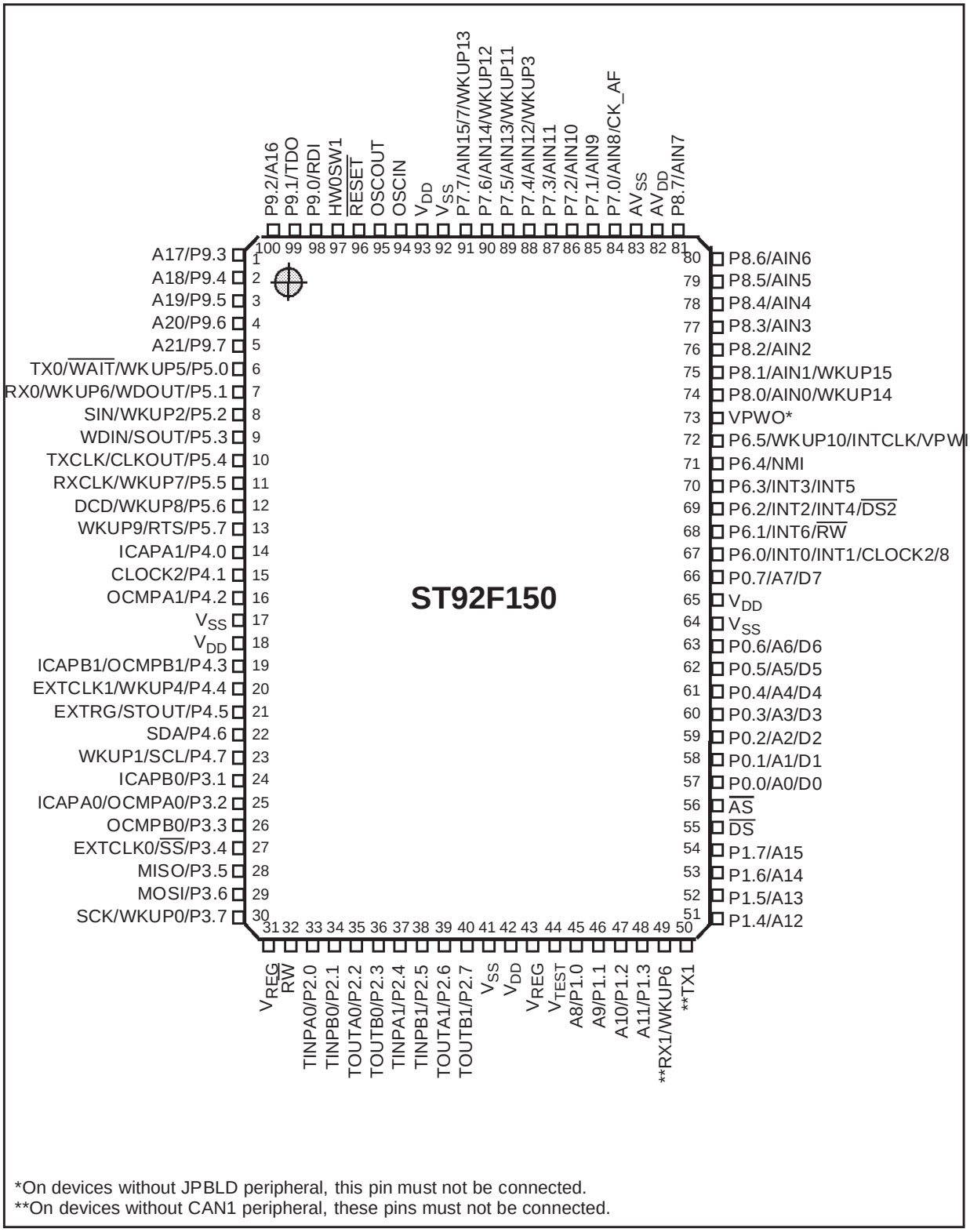
The alternate functions (*Italic characters*) are mapped on Port0, Port1, Port2, Port3, Port4, Port5, Port6, Port7, Port8 and Port9.

Figure 5. ST92F124/ST92F150: Pin Configuration (Top-view TQFP64)



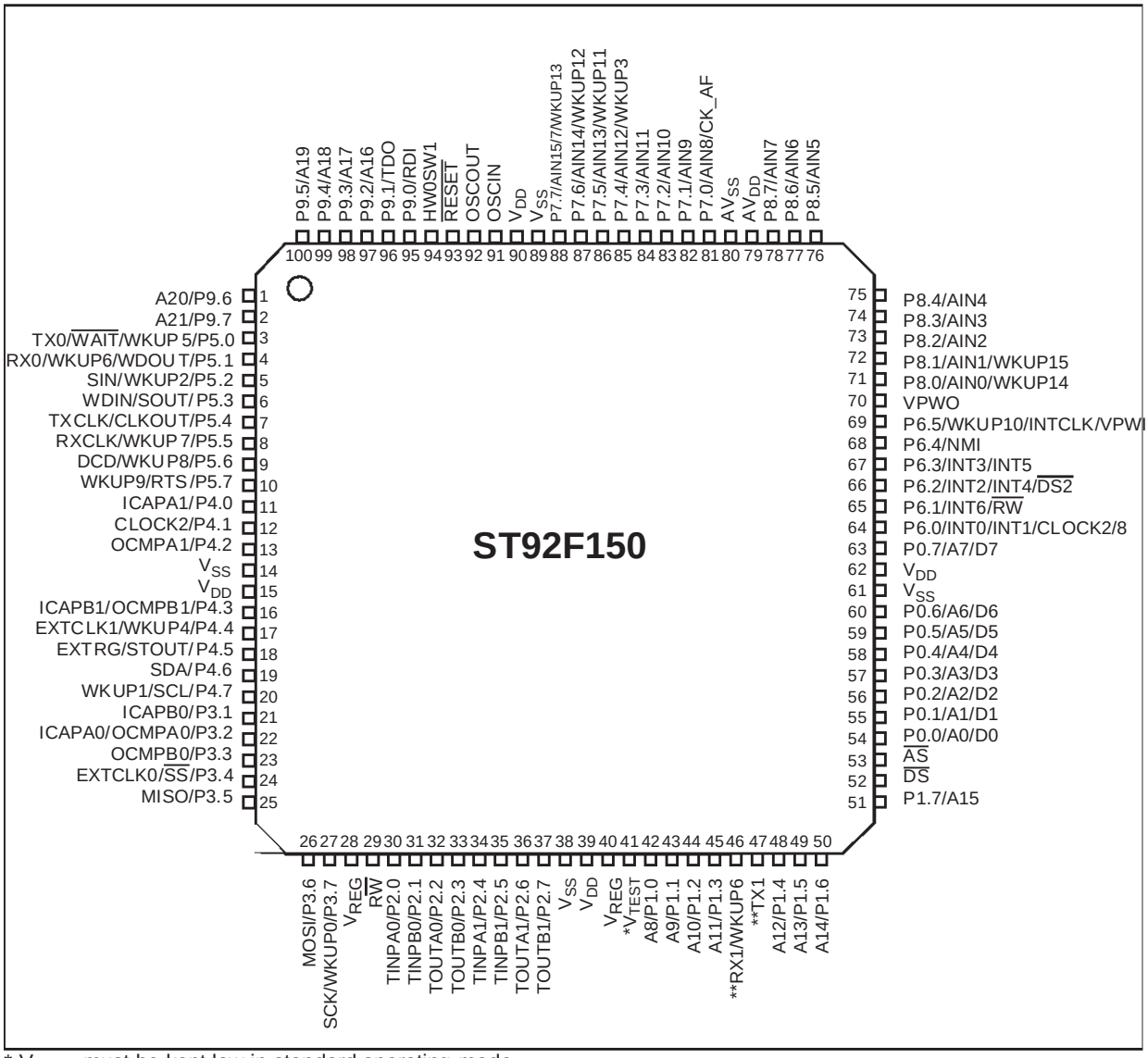
* Not available on ST92F124 version

Figure 6. ST92F150: Pin Configuration (Top-view PQFP100)



*On devices without JPBLD peripheral, this pin must not be connected.
**On devices without CAN1 peripheral, these pins must not be connected.

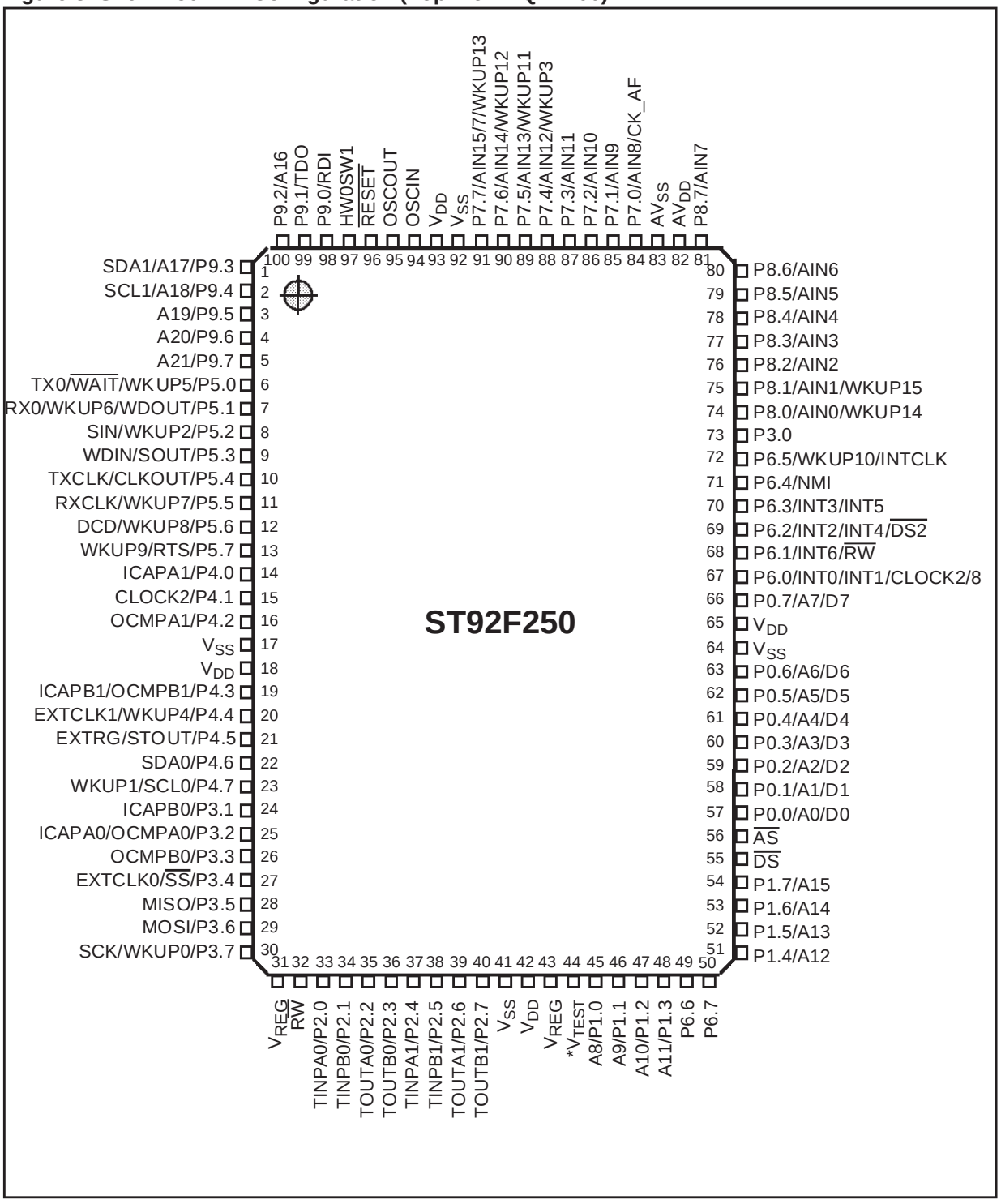
Figure 7. ST92F150: Pin Configuration (Top-view TQFP100)



* V_{TEST} must be kept low in standard operating mode.

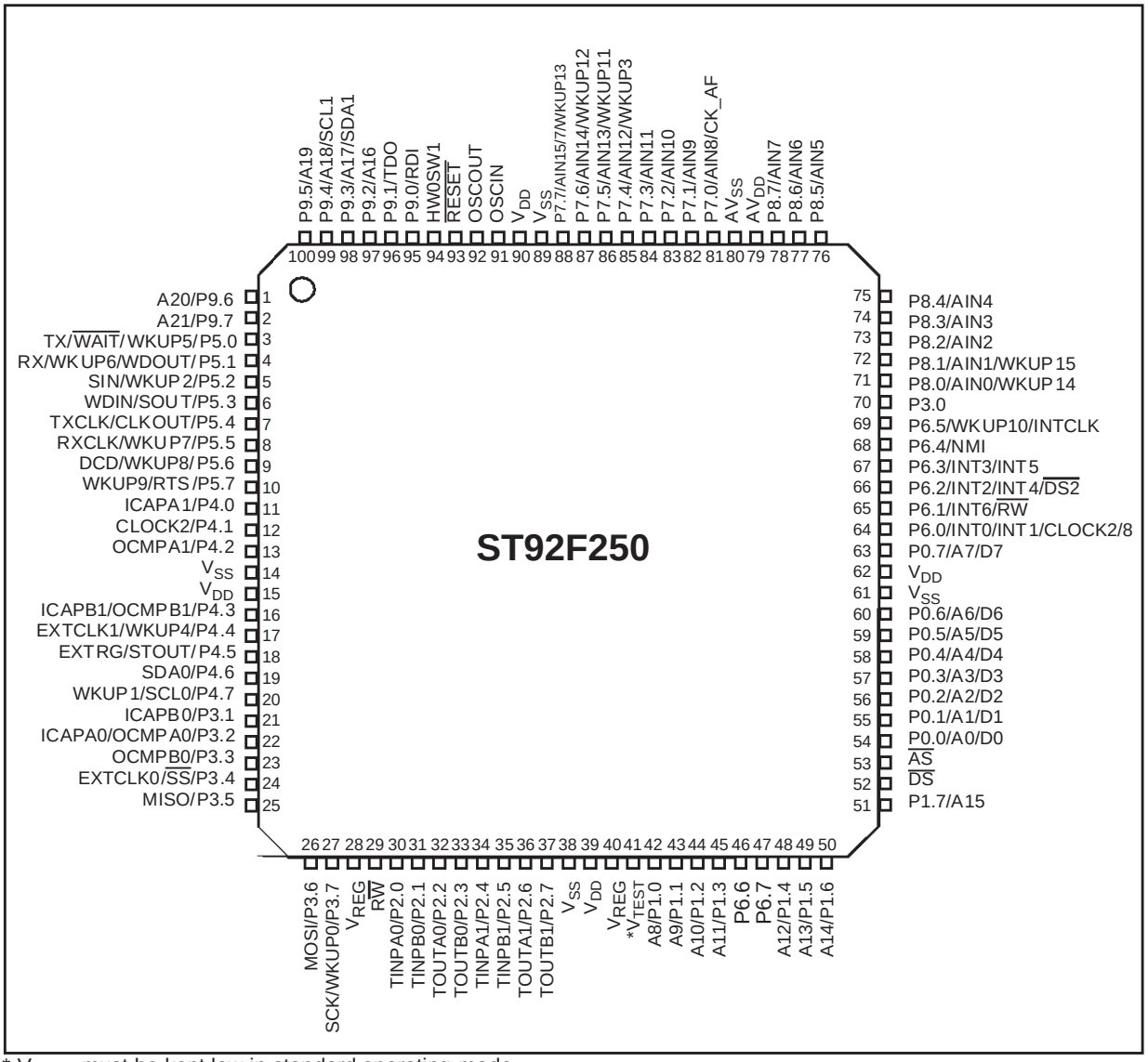
**On devices without CAN1 peripheral, these pins must not be connected.

Figure 8. ST92F250: Pin Configuration (Top-view PQFP100)



* V_{TEST} must be kept low in standard operating mode.

Figure 9. ST92F250: Pin Configuration (Top-view TQFP100)



* V_{TEST} must be kept low in standard operating mode.

Notes: