

**STK672-050**

Microstep Operation-Supported 4-Phase Stepping Motor Driver ($I_O = 3.0A$)

Overview

The STK672-050 is a unipolar constant-current chopper-type externally-excited 4-phase stepping motor driver hybrid IC which uses MOSFET power devices. It has a microstep operation-supported 4-phase distributed controller built-in to realize a high torque, low vibration, low noise stepping motor driver using a simple control circuit.

Applications

- Printer, copier, and X-Y plotter stepping motor drivers

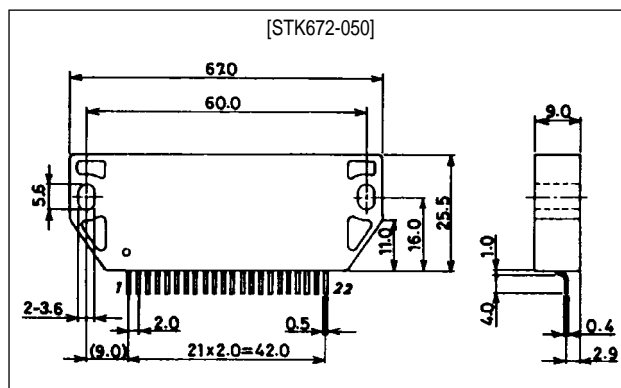
Features

- Microstep sine-wave driver operation using only an external clock input (0.2Ω current detection resistor built-in)
- Microstep drive using only an external reference voltage setting resistor
- 2, 1-2, W1-2, 2W1-2, 4W1-2 phase excitation selectable using external pins
- Selectable vector locus (perfect circle mode, inside 1 mode, outside 2 modes) to match motor characteristics in microstep drive state
- Phase hold function during excitation switching
- Schmitt trigger inputs with built-in pull-up resistor (20kΩ)
- Monitor output pin enabling real-time confirmation of IC excitation
- The CLK and RETURN inputs provide an internal noise elimination circuit as well as CMOS Schmitt circuit to prevent malfunction due to impulse noise.
- 4-phase distribution switch timing selected externally to either CLK rising-edge only detection mode or both rising-edge and falling-edge detection mode
- ENABLE pin for excitation current cutoff, thereby reducing system current drain when driver is stopped

Package Dimensions

unit: mm

4164



Series Organization

The following devices form a series with differing output capacity.

| Type No. | Output current (A) |
|------------|--------------------|
| STK672-040 | 1.5 |
| STK672-050 | 3.0 |

Specifications

Maximum Ratings at $T_a = 25^\circ\text{C}$

| Parameter | Symbol | Conditions | Ratings | Unit |
|--|-----------------------|--|--------------|------------------|
| Maximum supply voltage 1 | $V_{CC1 \text{ max}}$ | No signal | 52 | V |
| Maximum supply voltage 2 | $V_{CC2 \text{ max}}$ | No signal | -0.3 to +7.0 | V |
| Input voltage | $V_{IN \text{ max}}$ | Logic input block | -0.3 to +7.0 | V |
| Phase output current | $I_{OH \text{ max}}$ | One 0.5s pulse, V_{CC1} applied, Load/phase: $R = 5\Omega$, $L = 10\text{mH}$ | 4.0 | A |
| Repetitive avalanche handling capability | $E_{ar \text{ max}}$ | | 38 | mJ |
| Maximum output dissipation | $P_{d \text{ max}}$ | $\theta_{c-a} = 0$ | 25 | W |
| Operating substrate temperature | $T_c \text{ max}$ | | 105 | $^\circ\text{C}$ |
| Junction temperature | $T_j \text{ max}$ | | 150 | $^\circ\text{C}$ |
| Storage temperature | T_{stg} | | -40 to +125 | $^\circ\text{C}$ |

Allowable Operating Ranges at $T_a = 25^\circ\text{C}$

| Parameter | Symbol | Conditions | Ratings | Unit |
|--------------------------------|----------------------|--|----------------|------|
| Supply voltage 1 | V_{CC1} | With signal | 10 to 45 | V |
| Supply voltage 2 | V_{CC2} | With signal | $5.0 \pm 5\%$ | V |
| Input voltage | V_{IH} | | 0 to V_{CC2} | V |
| Phase driver withstand voltage | V_{DSS} | Tr1, 2, 3, 4 (A, \bar{A} , B, \bar{B} outputs) | 100 (min) | V |
| Phase current | $I_{OH \text{ max}}$ | 50% duty | 3.0 (max) | A |

Electrical Characteristics at $T_c = 25^\circ\text{C}$, $V_{CC1} = 24\text{V}$, $V_{CC2} = 5\text{V}$

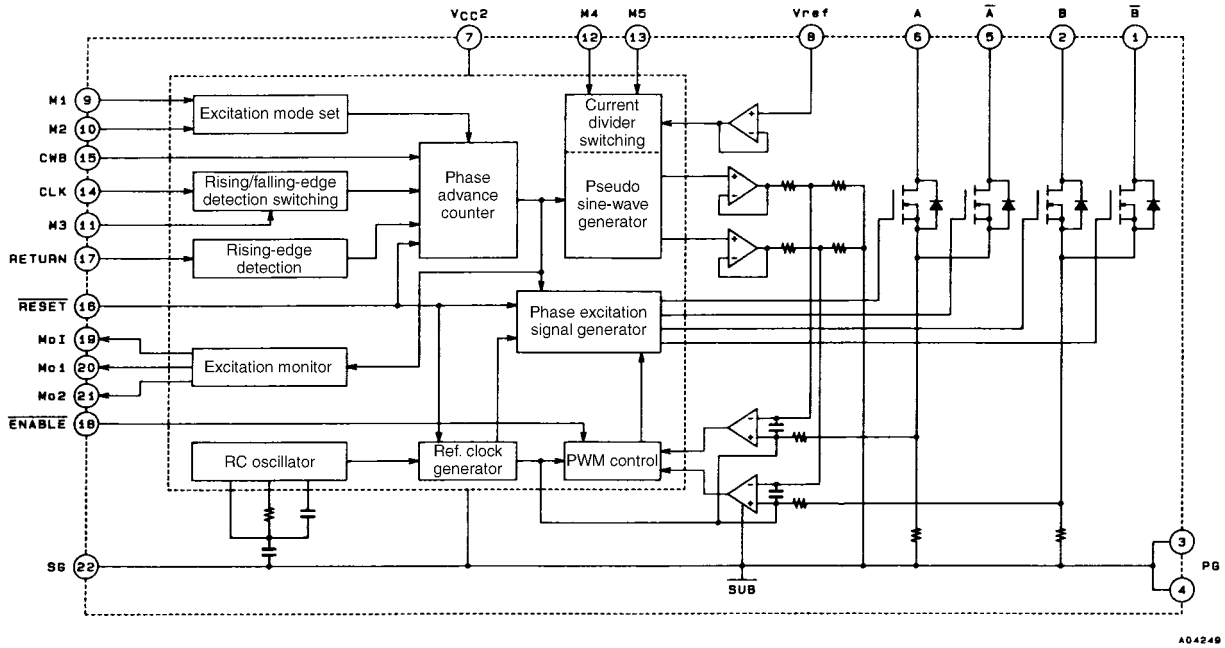
| Parameter | Symbol | Conditions | min | typ | max | Unit |
|---------------------------------------|---------------------|--|------|------|------|---------------|
| Control supply current | I_{CC} | Pin 7 input, ENABLE = low | - | 4.5 | 15 | mA |
| Output saturation voltage | V_{sat} | $R_L = 7.5\Omega$ ($I = 3\text{A}$) | - | 1.4 | 2.6 | V |
| Average output current | $I_{o \text{ ave}}$ | $V_{ref} = 0.6\text{V}$, Load/phase: $R = 3.5\Omega$, $L = 3.8\text{mH}$ | 0.45 | 0.50 | 0.55 | A |
| FET diode forward voltage | V_{df} | $I_f = 1.0\text{A}$ | - | 1.2 | 1.8 | V |
| [Control inputs] | | | | | | |
| Input voltage | V_{IH} | Excluding V_{ref} pin | 4.0 | - | - | V |
| | V_{IL} | Excluding V_{ref} pin | - | - | 1.0 | V |
| Input current | I_{IH} | Excluding V_{ref} pin | 0 | 1 | 10 | μA |
| | I_{IL} | Excluding V_{ref} pin | 125 | 250 | 510 | μA |
| [Vref input] | | | | | | |
| Input voltage | V_I | Pin 8 | 0 | - | 2.5 | V |
| Input current | I_I | Pin 8 | - | 1 | - | μA |
| [Control outputs] | | | | | | |
| Output voltage | V_{OH} | $I = -3\text{mA}$ (Mo1, Mo1, Mo2 pins) | 2.4 | - | - | V |
| | V_{OL} | $I = +3\text{mA}$ (Mo1, Mo1, Mo2 pins) | - | - | 0.4 | V |
| PWM frequency | f_c | | 37 | 47 | 57 | kHz |
| [Current division ratio (A/B)] | | | | | | |
| 2W1-2, W1-2, 1-2 | V_{ref} | $\theta = 1/8$ | | | 100 | % |
| 2W1-2, W1-2 | V_{ref} | $\theta = 2/8$ | | | 92 | % |
| 2W1-2 | V_{ref} | $\theta = 3/8$ | | | 83 | % |
| 2W1-2, W1-2, 1-2 | V_{ref} | $\theta = 4/8$ | | | 71 | % |

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| | | | | |
|-------------|------|----------------|-----|---|
| 2W1-2 | Vref | $\theta = 5/8$ | 55 | % |
| 2W1-2, W1-2 | Vref | $\theta = 6/8$ | 40 | % |
| 2W1-2 | Vref | $\theta = 7/8$ | 20 | % |
| 2 | Vref | | 100 | % |

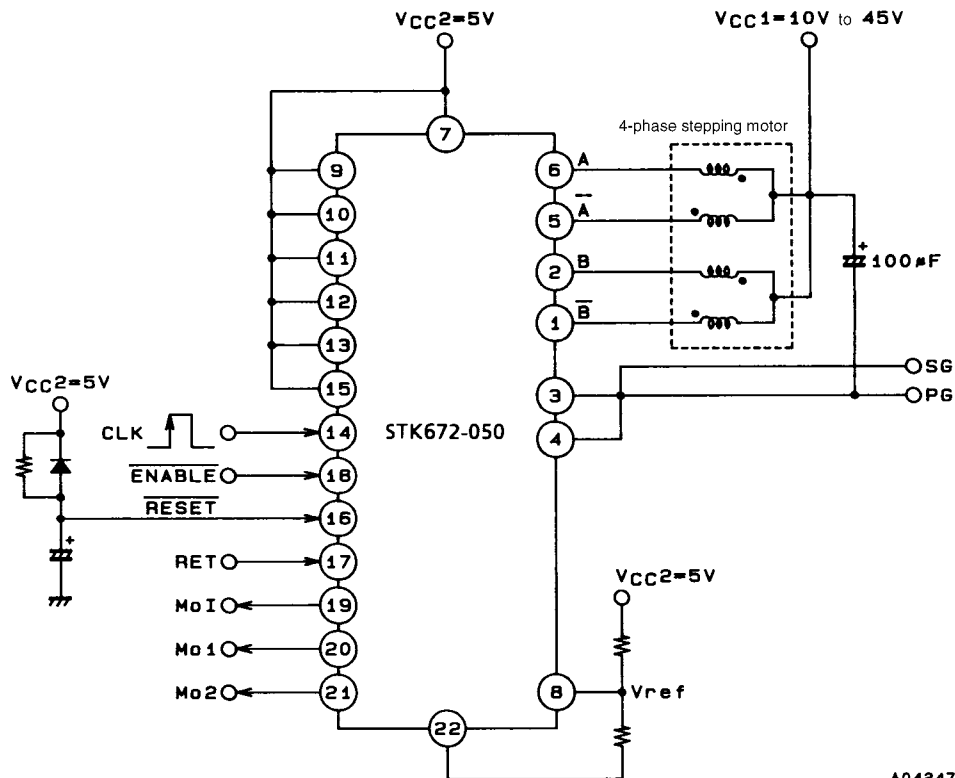
Note: All tests are made using a constant-voltage supply.
The current division ratio shows the design value.

Equivalent Block Diagram



Sample Application Circuit

2W1-2 phase excitation (microstep operation)



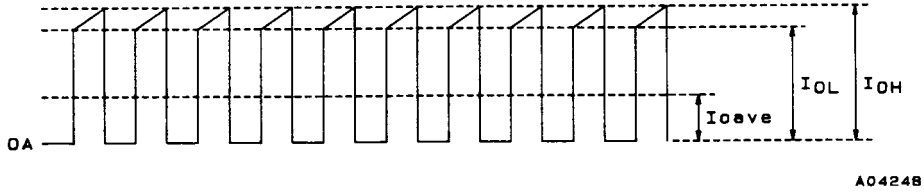
Motor Current Calculation

The motor current I_{OH} is determined by the reference voltage on pin 8 (V_{ref}). The relationship between I_{OH} and V_{ref} is given by the following equation.

$$I_{OH} = \frac{1}{3} \times V_{ref} / R_s$$

where R_s is the built-in current detection resistance ($0.2\Omega \pm 3\%$).

The motor current ranges from the current due to the frequency duty set by the oscillator (0.05 to 0.1A) to the allowable operating range maximum of $I_{OH} = 3.0A$.



Motor current waveform

Function Tables

| M1 | M2 | M3 | Excitation | Phase switching CLK edge timing |
|----|----|----|-------------|---------------------------------|
| 0 | 0 | 0 | Phase 1-2 | Rising and falling edge |
| 0 | 1 | 0 | Phase 2W1-2 | |
| 1 | 0 | 0 | Phase W1-2 | |
| 1 | 1 | 0 | Phase 4W1-2 | |
| 0 | 0 | 1 | Phase 2 | Rising edge only |
| 0 | 1 | 1 | Phase W1-2 | |
| 1 | 0 | 1 | Phase 1-2 | |
| 1 | 1 | 1 | Phase 2W1-2 | |

| Input | Active level |
|--------|--------------|
| ENABLE | Low |
| RESET | Low |

| Mo1 | Mo2 | Output |
|-----|-----|-----------|
| 0 | 0 | \bar{A} |
| 0 | 1 | B |
| 1 | 0 | A |
| 1 | 1 | \bar{B} |

| CWB | Direction |
|-----|-----------|
| 0 | Forward |
| 1 | Reverse |

Design material

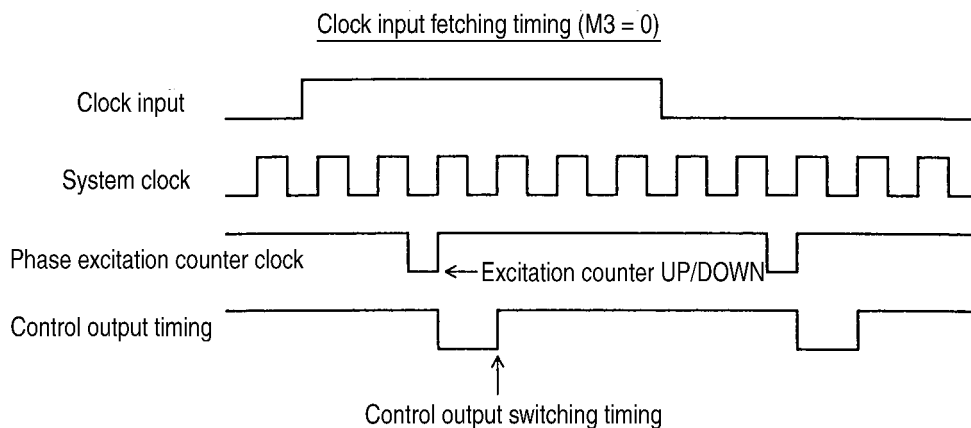
1. Explanation of input pins

| Pin No. | Name | Function | Pin format |
|-----------|------------|--|--|
| 14 | CLK | Phase switching clock | CMOS Schmitt configuration with pull-up resistor |
| 15 | CWB | Setting of rotation direction (CW/CCW) | CMOS Schmitt configuration with pull-up resistor |
| 17 | RETURN | Phase origin forced return | CMOS Schmitt configuration with pull-up resistor |
| 18 | ENABLE | Output cut-off | CMOS Schmitt configuration with pull-up resistor |
| 9, 10, 11 | M1, M2, M3 | Setting of excitation mode | CMOS Schmitt configuration with pull-up resistor |
| 12, 13 | M4, M5 | Setting of vector locus | CMOS Schmitt configuration with pull-up resistor |
| 16 | RESET | System reset | CMOS Schmitt configuration with pull-up resistor |
| 8 | Vref | Setting of current value | CMOS Schmitt configuration with pull-up resistor |

2. Functions and timing of input signals

2-1. CLK (Phase switching clock)

1. Input frequency range ■DC to 50 kHz
2. Minimum pulse width ■10 μ s
3. Duty ■40 to 60%
4. Pin format ■CMOS Schmitt configuration containing pull-up resistor (20 k Ω typical value)
5. Noise eliminating circuit with multiple stages is contained.
6. Functions
 - a. When the signal M3 is set to 1 or it is opened.
The excitation phase moves at each step at the rising edge of the clock.
 - b. When the signal M3 is set to 0.
The excitation phase moves at each step at the rising and falling edges of the clock.



2-2. CWB (Setting of rotation direction)

1. Pin format ■CMOS Schmitt configuration containing pull-up resistor (20k Ω , typical value)
2. Function
 - a. When the signal CWB is set to 1.
It rotates clockwise.
 - b. When the signal CWB is set to 0.
It rotates counterclockwise.
3. Note ■When the signal M3 is set to 0, the CWB input signal must not be changed at the rising edge and falling edge of the clock input for the period of 5 μ s.

2-3. RETURN (It forcibly returns the phase to the origin of current excitation phase.)

- 1. Pin format ■CMOS Schmitt configuration containing pull-up resistor
(20kΩ, typical value)
- 2. Noise eliminating circuit is contained.
- 3. Function ■Forces to moves to the origin of current excitation phase by
setting the RETURN signal to high state.

2-4. $\overline{\text{ENABLE}}$ (ON/OFF control of excitation drive output A, $\overline{\text{A}}$, B, and $\overline{\text{B}}$ and selection of operation/hold state in hybrid-IC)

- 1. Pin format ■CMOS Schmitt configuration containing pull-up resistor
(20 kΩ, typical value)
- 2. Function
 - a. When the $\overline{\text{ENABLE}}$ signal is set to a high state or it is opened.
It is usually placed in the operation status.
 - b. When the $\overline{\text{ENABLE}}$ signal is set to a low state
The hybrid-IC is placed into the hold state, forcing the excitation drive output to be turned off.
At this time, the system clock of the HC stops, the H-IC is not affected if the input pin other than the reset input changes.

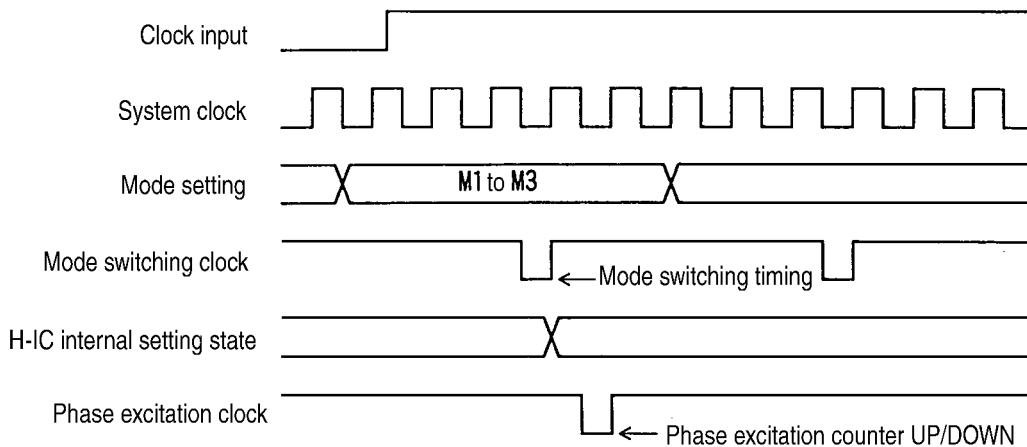
2-5. M1, M2, and M3 (Selection of excitation modes and clock input edge timing)

- 1. Pin format ■CMOS Schmitt configuration containing the pull-up resistor
(20 kΩ typical value)
- 2. Functions

| | | | | | | |
|----|----|----------------------|-----------------------|------------------------|------------------------|-----------------------------------|
| | M2 | 0 | 0 | 1 | 1 | Phase switching clock edge timing |
| M3 | M1 | 0 | 1 | 0 | 1 | |
| 1 | | 2 phase excitation | 1-2 phase excitation | W1-2 phase excitation | 2W1-2 phase excitation | Only the rising edge |
| 0 | | 1-2 phase excitation | W1-2 phase excitation | 2W1-2 phase excitation | 4W1-2 phase excitation | Rising edge and falling edge |

- 3. Valid timing of mode setting
 - The mode must not be changed within 5 μs from the rising edge and falling edge of the clock.

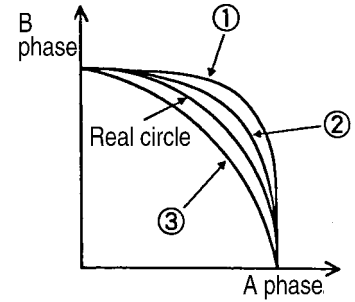
Fetching timing of mode setting



2-6. M4 and M5 (Setting of rotation vector locus at micro-step)

| | | | | |
|------|-------------|---|---|---|
| M4 | 1 | 0 | 1 | 0 |
| M5 | 1 | 0 | 0 | 1 |
| Mode | Real circle | ① | ② | ③ |

For the current division ratio, see Section 4-3.



2-7. RESET (Reset of entire system)

1. Pin format ■CMOS Schmitt configuration containing the pull-up resistor (20 kΩ typical value)
2. Function ■All circuit states are set to the initial values by setting the RESET signal to the low state (pulse width of 10 μs or more). At this time, for all modes including the excitation mode, the A and \bar{B} phases are set to the origin.

2-8. Vref(Setting of the current value used as the reference of constant current detection)

1. Pin format ■Analog input configuration
2. Function ■By applying the voltage of 2.5 V or less of the control system power source Vcc2, the constant current control can be performed over the excitation current of the motor at the 100% of the rated current value.
■The constant current can be controlled in proportional to the Vref voltage with this value specified as a high limit.

3. Explanation of output pins

| Pin No. | Name | Function | Pin format |
|---------|----------|---------------------------------|-----------------------------|
| 19 | Mo1 | Phase excitation origin monitor | CMOS standard configuration |
| 20, 21 | Mo1, Mo2 | Phase excitation state monitor | CMOS standard configuration |

4. Functions and timing of output signals

4-1. A, \bar{A} , B, and \bar{B} (Output for phase excitation use of motor)

1. Function ■In four phase two excitation mode, the interval of 3.75 μs (typical value) is set when the output signals of the phases A and \bar{A} , B and \bar{B} change.

4-2. Mo1, Mo2, and Mo1 (Monitor of excitation state)

1. Pin format ■CMOS standard configuration
2. Function ■Outputs the state of the current phase excitation output.

| Phase coordinate | A phase | B phase | \bar{A} phase | \bar{B} phase |
|------------------|---------|---------|-----------------|-----------------|
| Mo1 | 1 | 0 | 0 | 1 |
| Mo2 | 0 | 1 | 0 | 1 |

For the Mo1, 0 is output at the origin of each phase.
At other points, 1 is output.

4-3. Current division ratio based on M3, M4, and M5 Reference values

| Mode | | Real circle | ① | ② | ③ | Unit | Number of steps | | |
|------------------------|--------|-------------|--------|--------|--------|------|-----------------|-------|---------|
| Setting | M3 = 0 | M4 = 1 | M4 = 0 | M4 = 1 | M4 = 0 | | | | |
| | M3 = 1 | M5 = 1 | M5 = 0 | M5 = 1 | M5 = 0 | | | | |
| Current division ratio | 4W1-2 | | 14 | 15 | 15 | 13 | % | | 1 / 16 |
| | | 2W1-2 | 20 | 25 | 23 | 19 | | 1 / 8 | 2 / 16 |
| | | | 31 | 34 | 33 | 28 | | | 3 / 16 |
| | | 2W1-2 | 40 | 44 | 42 | 39 | | 2 / 8 | 4 / 16 |
| | | | 48 | 51 | 49 | 45 | | | 5 / 16 |
| | | 2W1-2 | 55 | 62 | 57 | 54 | | 3 / 8 | 6 / 16 |
| | | | 65 | 69 | 65 | 62 | | | 7 / 16 |
| | | 2W1-2 | 71 | 77 | 71 | 69 | | 4 / 8 | 8 / 16 |
| | | | 77 | 82 | 77 | 74 | | | 9 / 16 |
| | | 2W1-2 | 83 | 88 | 85 | 82 | | 5 / 8 | 10 / 16 |
| | | | 88 | 92 | 89 | 85 | | | 11 / 16 |
| | | 2W1-2 | 92 | 95 | 95 | 92 | | 6 / 8 | 12 / 16 |
| | | | 97 | 98 | 98 | 94 | | | 13 / 16 |
| | | 2W1-2 | 100 | 100 | 100 | 100 | | 7 / 8 | 14 / 16 |

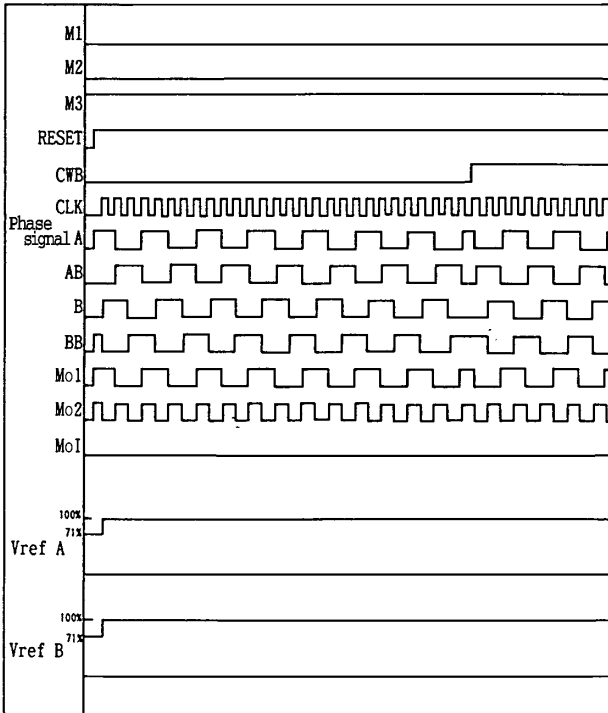
[Load conditions]

$V_{cc1} = 24V, V_{cc2} = 5V, R / L = 3.5\Omega / 3.8mH$

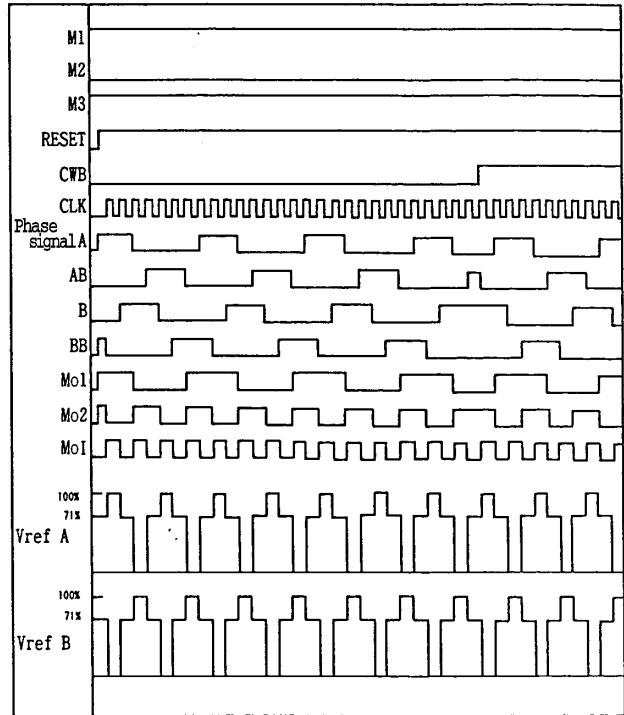
5. Phase excitation and timing chart

5-1. Rising edge operation of clock

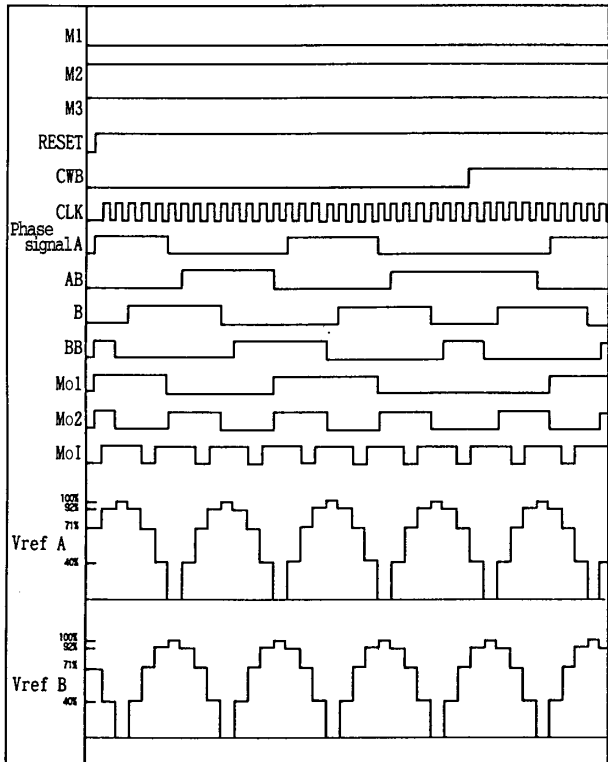
• 2 phase excitation



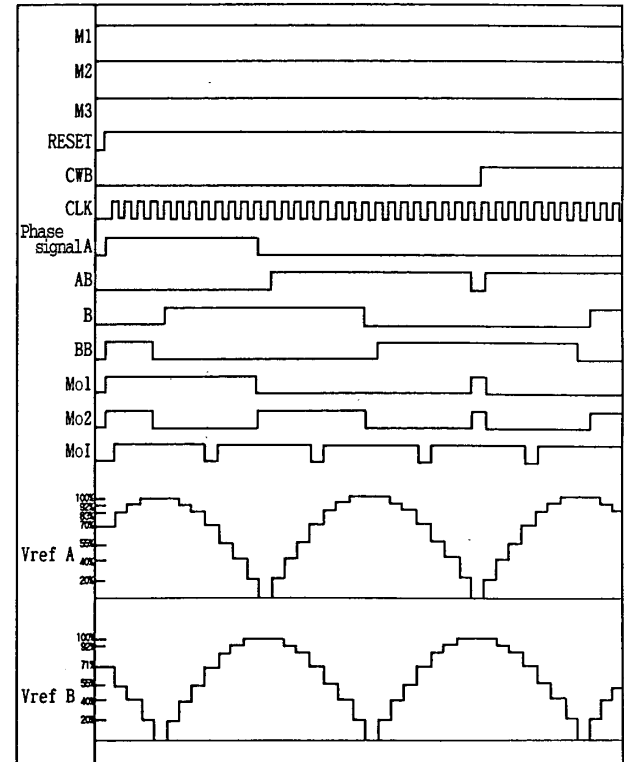
• 1-2 phase excitation



• W1-2 phase excitation

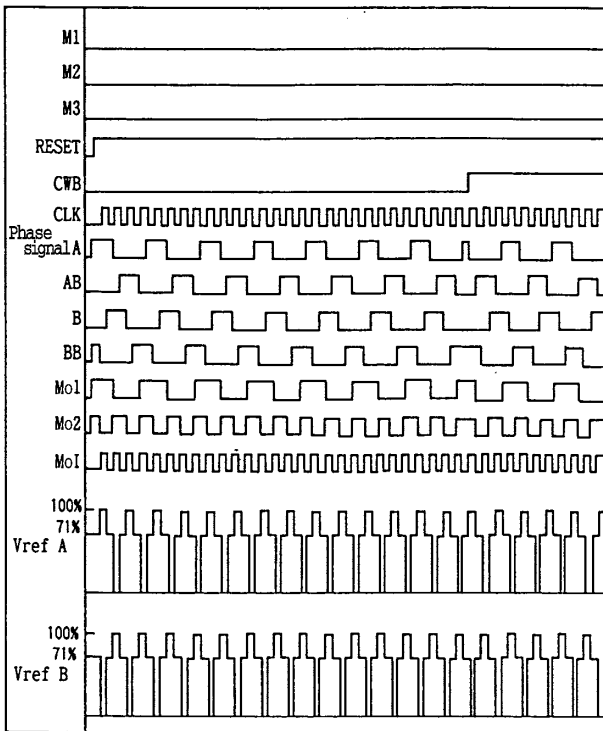


• 2W-2 phase excitation

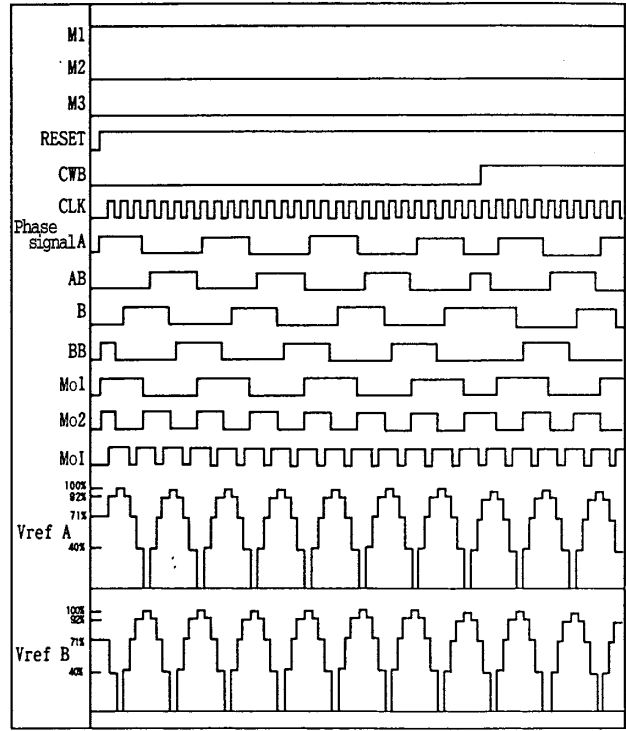


5-2. Rising edge and falling edge operation of clock

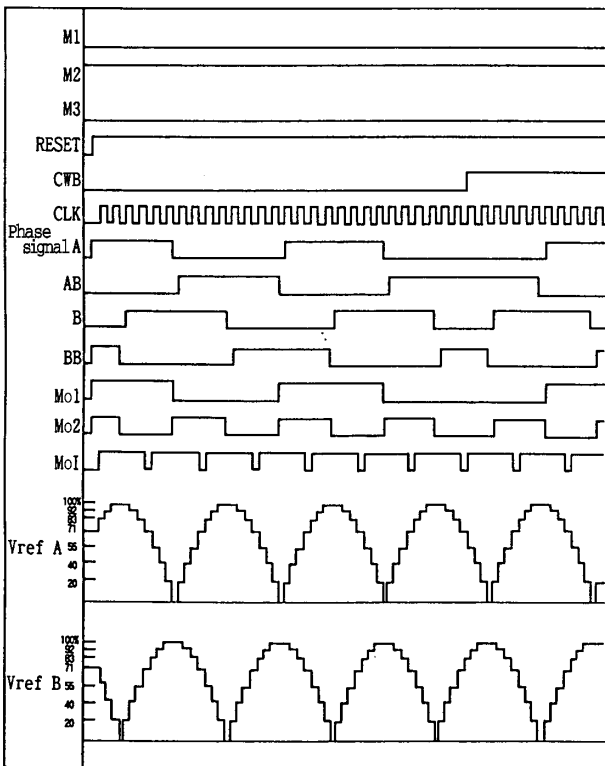
• 2 phase excitation



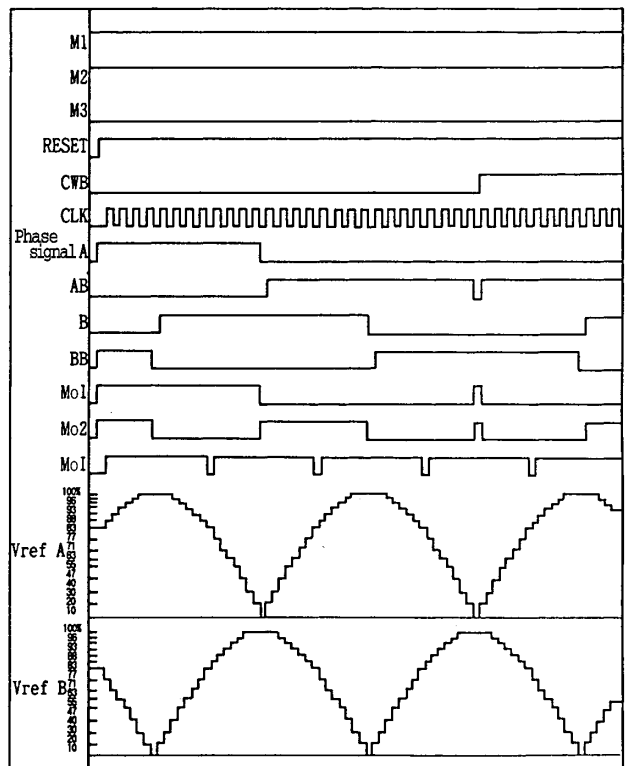
• 1-2 phase excitation



• W1-2 phase excitation



• 2W-2 phase excitation



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