



SANYO Semiconductors DATA SHEET

STK672-120-E

Thick-Film Hybrid IC
Unipolar Fixed-Current Chopper (Self-Excited PWM)
Scheme and Built-in Phase Signal Distribution IC
Two-Phase Stepping Motor Driver
(Square Wave Drive) Output Current 2.4A

Overview

The STK672-120-E is a unipolar fixed-current chopper type 2-phase stepping motor driver hybrid IC. It features power MOSFETs in the output stage and a built-in phase signal distribution IC. The incorporation of a phase distribution IC allows the STK672-120-E to control the speed of the motor based on the frequency of an external input clock signal. It supports two types of excitation for motor control: 2-phase excitation and 1-2 phase excitation. It also provides a function for switching the motor direction.

Applications

- Two-phase stepping motor drive in send/receive facsimile units
- Paper feed in copiers, industrial robots, and other applications that require 2-phase stepping motor drive

Features

- The motor speed can be controlled by the frequency of an external clock signal (the CLOCK pin signal).
- The excitation type is switched according to the state (low or high) of the MODE pin. The mode is set to 2-phase or 1-2 phase excitation on the rising edge of the clock signal.
- A motor direction switching pin (the CWB pin) is provided.
- All inputs are schmitt inputs and 40kΩ (typical: -50 to +100%) pull-up resistors are built in.
- The motor current can be set by changing the Vref pin voltage. Since a 0.165Ω current detection resistor is built in, a current of 1A is set for each 0.165V of applied voltage.
- The input frequency range for the clock signal used for motor speed control is 0 to 25kHz.
- Supply voltage ranges: $V_{CC} = 10$ to 42V, $V_{DD} = 5.0V \pm 5\%$
- This IC supports motor operating currents of up to 2.4A at $T_c = 105^\circ\text{C}$, and of up to 4.0A at $T_c = 25^\circ\text{C}$.

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STK672-120-E

Specifications

Maximum Ratings at $T_c = 25^\circ\text{C}$

| Parameter | Symbol | Conditions | Ratings | Unit |
|---------------------------------|--------------|---|--------------|------------------|
| Maximum supply voltage 1 | V_{CC} max | No signal | 52 | V |
| Maximum supply voltage 2 | V_{DD} max | No signal | -0.3 to +7.0 | V |
| Input voltage | V_{IN} max | Logic input pins | -0.3 to +7.0 | V |
| Output current | I_{OH} max | $V_{DD} = 5\text{V}$, $\text{CLOCK} \geq 200\text{Hz}$ | 4.0 | A |
| Repeated avalanche capacity | Ear max | | 36 | mJ |
| Allowable power dissipation | P_d max | With an arbitrarily large heat sink. Per MOSFET | 8.5 | W |
| Operating substrate temperature | T_c max | | 105 | $^\circ\text{C}$ |
| Junction temperature | T_j max | | 150 | $^\circ\text{C}$ |
| Storage temperature | T_{stg} | | -40 to +125 | $^\circ\text{C}$ |

Allowable Operating Ranges at $T_a = 25^\circ\text{C}$

| Parameter | Symbol | Conditions | Ratings | Unit |
|--------------------------------|-----------|--|---------------|------|
| Maximum supply voltage 1 | V_{CC} | With signals applied | 10 to 42 | V |
| Maximum supply voltage 2 | V_{DD} | With signals applied | $5.0 \pm 5\%$ | V |
| Input voltage | V_{IH} | | 0 to V_{DD} | V |
| Output current 1 | I_{OH1} | $T_c = 105^\circ\text{C}$, $\text{CLOCK} \geq 200\text{Hz}$ | 2.4 | A |
| Output current 2 | I_{OH2} | $T_c = 80^\circ\text{C}$, $\text{CLOCK} \geq 200\text{Hz}$ See the motor current (I_{OH}) derating curve | 3.0 | A |
| Clock frequency | f_{CL} | Minimum pulse width: 20 μs | 0 to 25 | kHz |
| Phase driver withstand voltage | V_{DSS} | $I_D = 1\text{mA}$ ($T_c = 25^\circ\text{C}$) | 100 min | V |

Electrical Characteristics at $T_c = 25^\circ\text{C}$, $V_{CC} = 24\text{V}$, $V_{DD} = 5\text{V}$

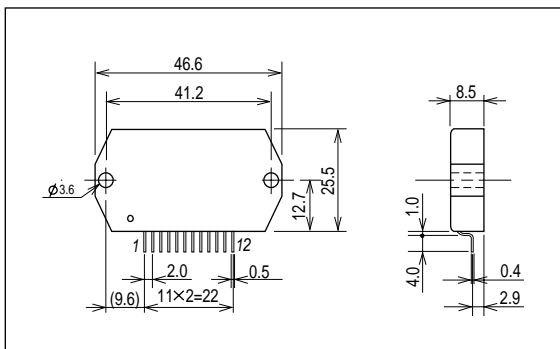
| Parameters | Symbols | Conditions | Rating | | | unit |
|------------------------------|------------|---|--------|------|------|---------------|
| | | | min | typ | max | |
| V_{DD} supply current | I_{CCO} | $\text{CLOCK} = \text{GND}$ | | 2.6 | 6 | mA |
| Output average current | I_{oave} | With $R/L = 3\Omega/3.8\text{mH}$ in each phase $V_{ref} = 0.176\text{V}$ | 0.56 | 0.62 | 0.69 | A |
| FET diode forward voltage | V_{df} | $I_f = 1\text{A}$ ($R_L = 23\Omega$) | | 1.1 | 1.7 | V |
| Output saturation voltage | V_{sat} | $R_L = 23\Omega$ | | 0.4 | 0.56 | V |
| High-level input voltage | V_{IH} | Pins 6 to 9 (4 pins) | 4.0 | | | V |
| Low-level input voltage | V_{IL} | Pins 6 to 9 (4 pins) | | | 1.0 | V |
| Input current | I_{IL} | With pins 6 to 9 at the ground level. Pull-up resistance: 40k Ω (typical) | 62 | 125 | 250 | μA |
| V_{ref} input voltage | V_{rH} | Pin 12 | 0 | | 3.5 | V |
| V_{ref} input bias current | I_{IB} | With pin 12 at 1V | | 50 | 500 | nA |

Note: A fixed-voltage power supply must be used.

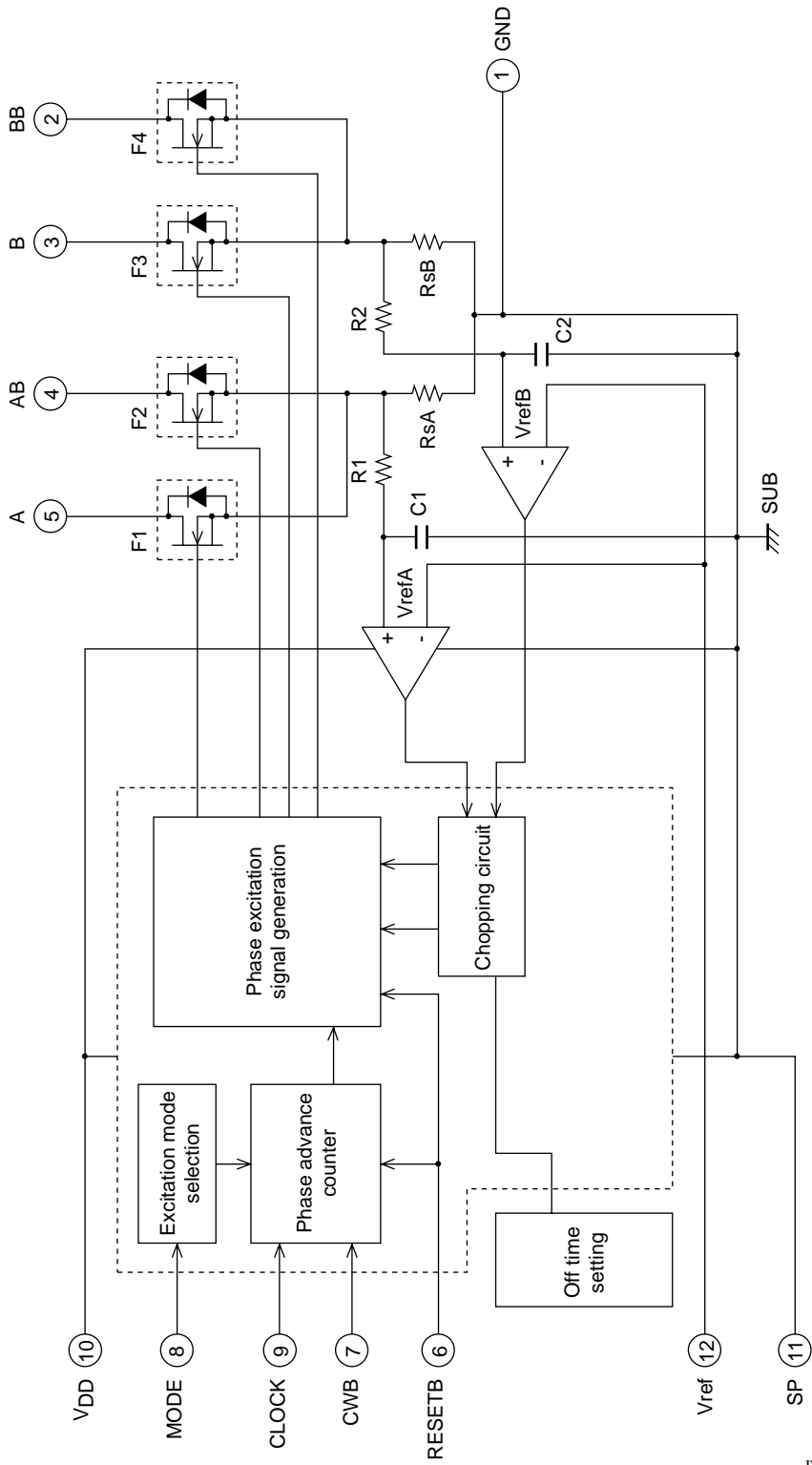
Package Dimensions

unit:mm (typ)

4167

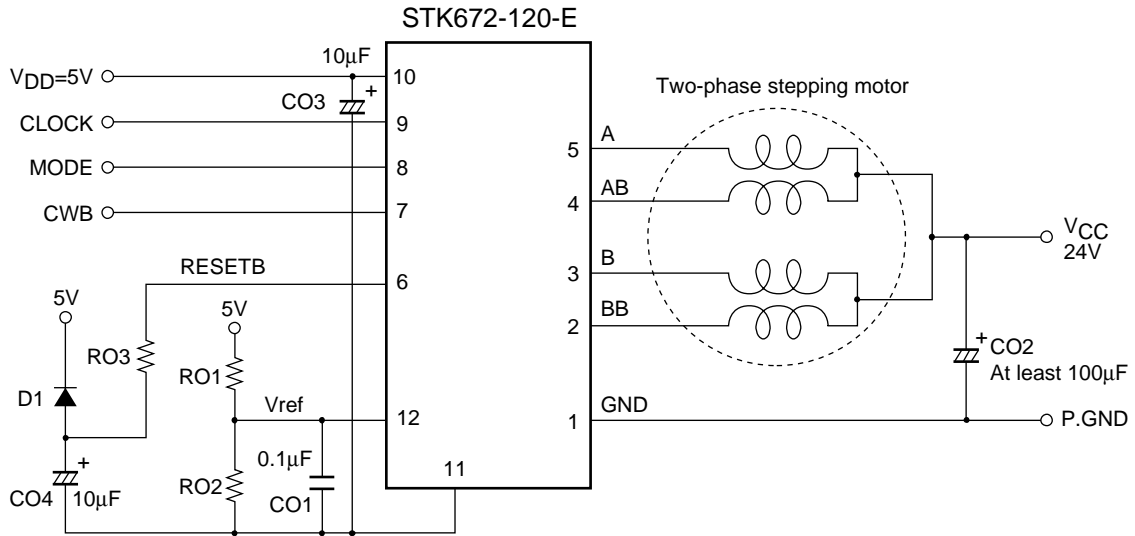


Internal Equivalent Circuit Block Diagram



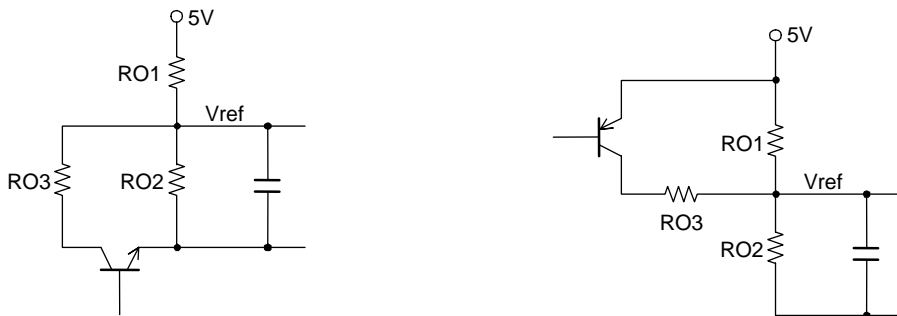
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Sample Application Circuit



ITF02597

- To minimize noise in the 5V system, locate the ground side of capacitor CO2 in the above circuit as close as possible to pin 1 of the IC.
- Insert resistor RO3 (47 to 100Ω) so that the discharge energy from capacitor CO4 is not directly applied to the CMOS IC in this hybrid device. If the diode D1 has Vf characteristics with Vf less than or equal to 0.6V (when If = 0.1A), this will be smaller than the CMOS IC input pin diode Vf. If this is the case RO3 may be replaced with a short without problem.
- Standard or HC type input levels are used for the pin 7, 8, and 9 inputs.
- If open-collector type circuits are used for the pin 7, 8, and 9 inputs, these circuit will be in the high-impedance state for high level inputs. As a result, chopping circuit noise may cause the input circuits to operate incorrectly. To prevent incorrect operation due to such noise, capacitors with values between 470 and 1000pF must be connected between pins 7 and 11, 8 and 11, and 9 and 11. (A capacitor with a value between 470 and 1000pF must be connected between pins 6 and 11 as well if an open-collector output IC is used for the RESETB pin (pin 6) input.)
- Taking the input bias current (I_B) characteristics into account, the resistor RO1 must not exceed 100kΩ.
- The following circuit (for a lowered current of over 0.2A) is recommended if the application needs to temporarily lower the motor current. Here, a value of close to 100kΩ must be used for resistor RO1 to make the transistor output saturation voltage as low as possible.



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Input Pin Functions (CMOS input levels)

| Pin | Pin No. | Function | Input conditions when operating |
|--------|---------|--|---|
| CLOCK | 9 | Reference clock for motor phase current switching | Operates on the rising edge of the signal |
| MODE | 8 | Excitation mode selection | Low: 2-phase excitation High: 1-2 phase excitation |
| CWB | 7 | Motor direction switching | Low: CW (forward) High: CCW (reverse) |
| RESETB | 6 | System reset and A, AB, B, and BB outputs cutoff. Applications must apply a reset signal for at least 20μs when power is first applied. | A reset is applied by a low level |

- A simple reset function is formed from D1, CO4, and RO3 in this application circuit. With the CLOCK input held low, when the 5V supply voltage is brought up a reset is applied if the motor output phases A and BB are driven. If the 5V supply voltage rise time is slow (over 50ms), the motor output phases A and BB may not be driven. Increase the value of the capacitor CO4 and check circuit operation again.
- See the timing chart for the concrete details on circuit operation.

Usage Notes

- 5V system input pins

[RESETB and CLOCK (Input signal timing when power is first applied)]

As shown in the timing chart, a RESETB signal input is required by the driver to operate with the timing in which the F1 gate is turned on first. The RESETB signal timing must be set up to have a width of at least 20μs, as shown below. The capacitor CO4 and the resistor RO3 in the application circuit form simple reset circuit that uses the RC time constant rising time. However, when designing the RESETB input based on CMOS levels, the application must have the timing shown in figure 1.

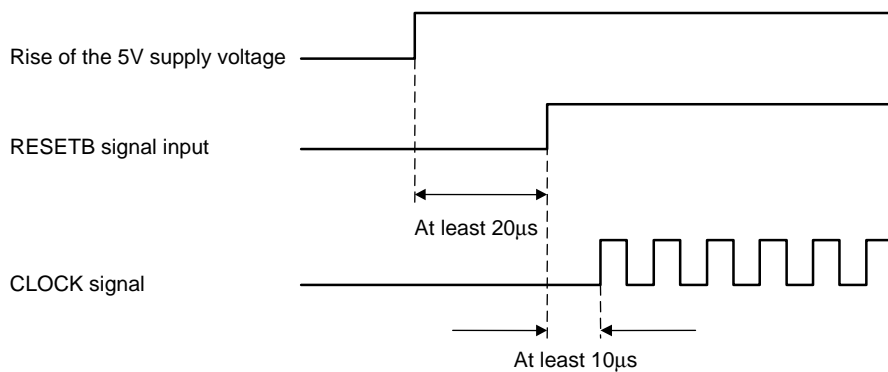


Figure 1 RESETB and CLOCK Signals Input Timing

See the timing chart for details on the CLOCK, MODE, CWB, and other input pins.

[Vref <Motor current peak value setting>]

In the sample application circuit, the peak value of the motor current (I_{OH}) is set by RO1, RO2, and V_{DD} (5V) as described by the formula below.

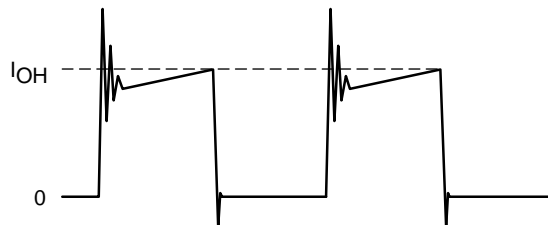


Figure 2 Motor Current I_O Flowing into the Driver IC

$I_{OH} = V_{ref} \div R_s$ Here, R_s is hybrid IC internal current detection resistor

$V_{ref} = (R02 \div (R01 + R02)) \times 5V$

STK672-120-E: $R_s = 0.165\Omega$

- Allowable motor current operating range

The motor current (I_{OH}) must be held within the range corresponding to the area under the curve shown in figure 4. For example, if the operating substrate temperature T_c is 105°C , then I_{OH} must be held under $I_{OH} = 2.4\text{A}$, and in hold mode I_{OH} must be held under $I_{OH} = 2.0\text{A}$.

- Thermal design

[Operating range in which a heat sink is not used]

Thermal design that lowers this hybrid IC's operating substrate temperature can be effective in improving end product quality. The size of the heat sink required by this hybrid IC varies with the average power dissipation P_D . The value of P_D increases as the output current increases, as shown in figure 5.

Since there are periods when current flows and periods when the current is off during actual motor operation, P_D cannot be determined from the data presented in figure 5. Therefore, we calculate P_D assuming that actual motor operation consists of repetitions of the operation shown in figure 3.

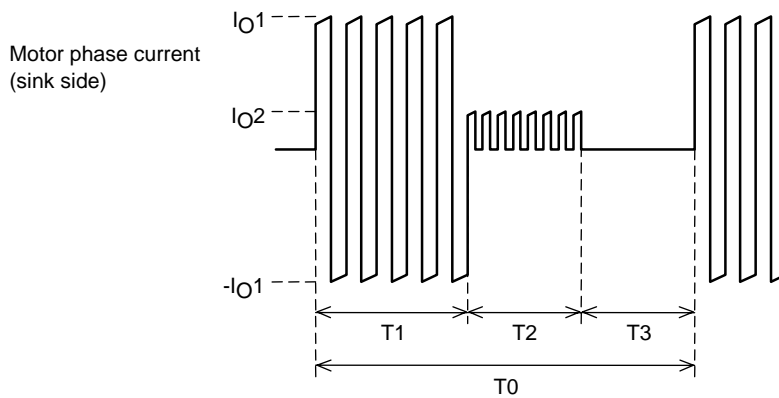


Figure 3 Motor Current Timing

$T1$: Motor rotation operation time

$T2$: Motor hold operation time

$T3$: Motor current off time

$T2$ may be reduced, depending on the application.

$T0$: Single repeated motor operating cycle

I_{O1} and I_{O2} : Motor current peak values

Due to the structure of motor windings, the phase current is a positive and negative current with a pulse form.

Note that figure 3 presents the concepts here, and that the on/off duty of the actual signals will differ.

The hybrid IC internal average power dissipation P_D can be calculated from the following formula.

$$P_D = (T1 \times P1 + T2 \times P2 + T3 \times 0) \div T0 \quad (I)$$

(Here, $P1$ is the P_D for I_{O1} and $P2$ is the P_D for I_{O2})

If the value calculated in formula (I) above is under 1.5W , then there will be no need to use a heat sink for ambient temperatures T_a up to 60°C . See figure 6 for operating substrate temperature rise data when a heat sink is not attached. If a heat sink is to be used, to lower T_c if P_D increases, use formula (II) and the graph in figure 7 to determine the size of the heat sink.

$$\theta_{c-a} = (T_c \text{ max} - T_a) \div P_D \quad (II)$$

$T_c \text{ max}$: Maximum operating substrate temperature = 105°C

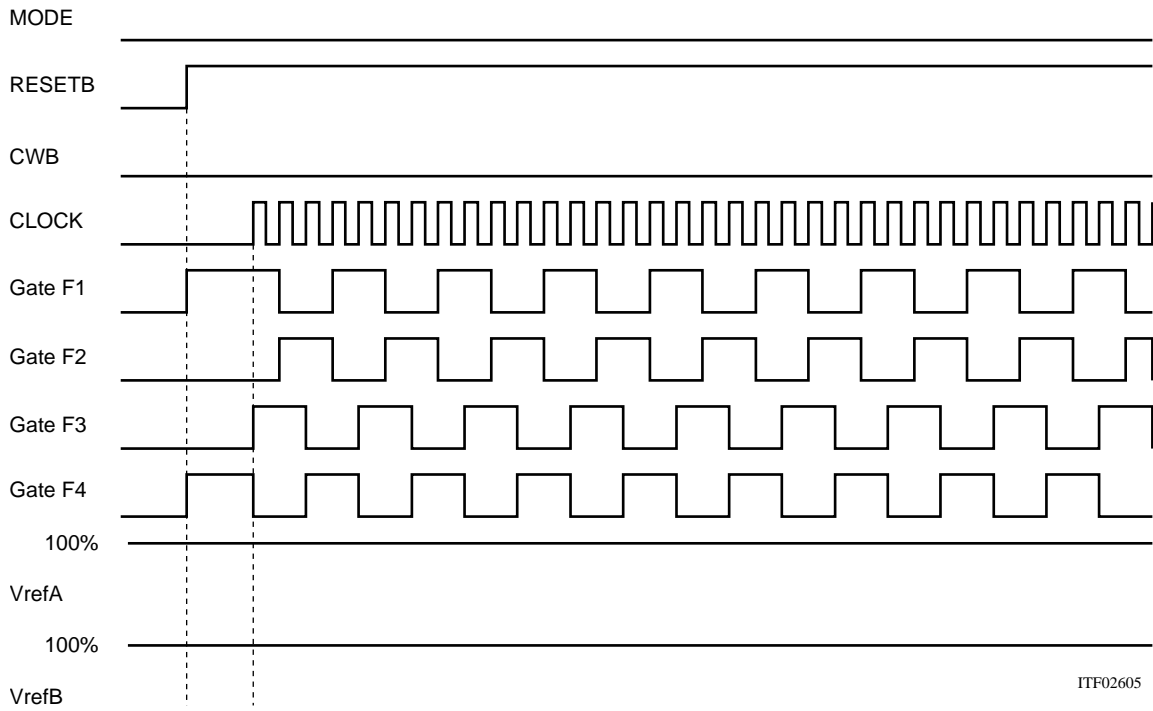
T_a : The hybrid IC ambient temperature

While formulas (I) and (II) above are adequate for thermal design, note that figure 5 is merely a single example of one operating mode for a single motor. For example, while figure 5 shows a 2-phase excitation motor, if 1-2 phase excitation is used with a 500Hz clock frequency, the drive will be turned off for 25% of the time and the loss P_D will be reduced to 75% of that in figure 5.

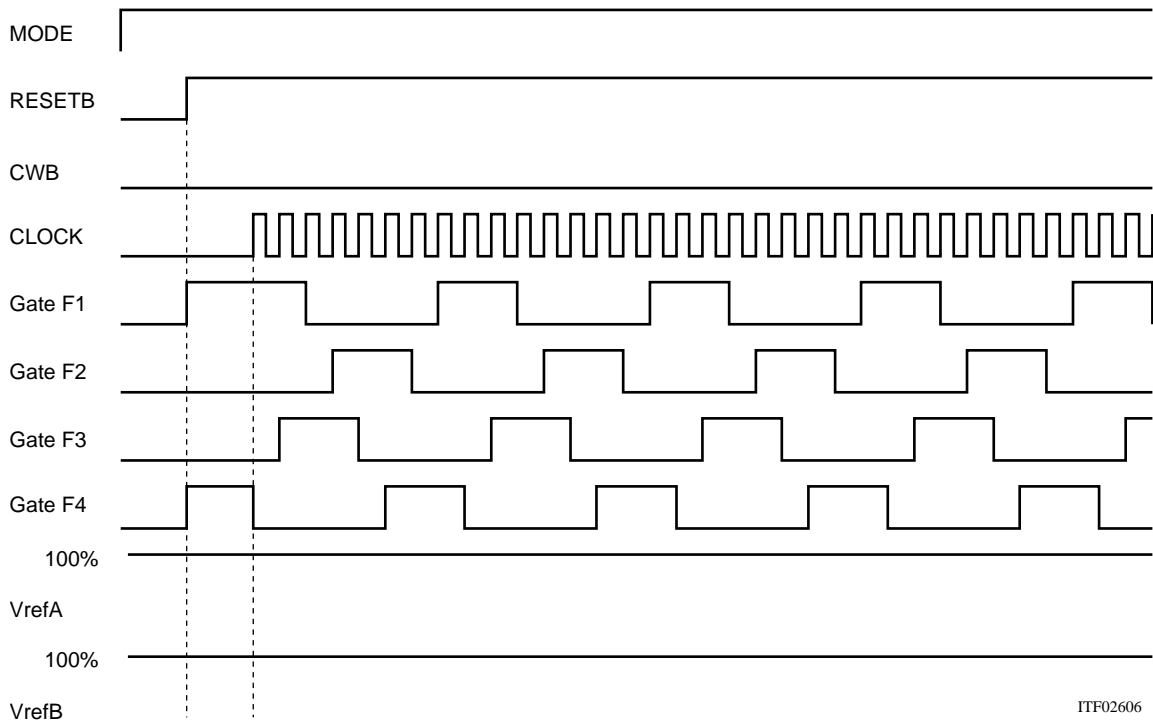
It is extremely difficult for SANYO to calculate the internal average power dissipation P_D for all possible end product conditions. After performing the above rough calculations, always install the hybrid IC in an actual end product and verify that the substrate temperature T_c does not rise above 105°C .

Timing Chart

2-phase excitation

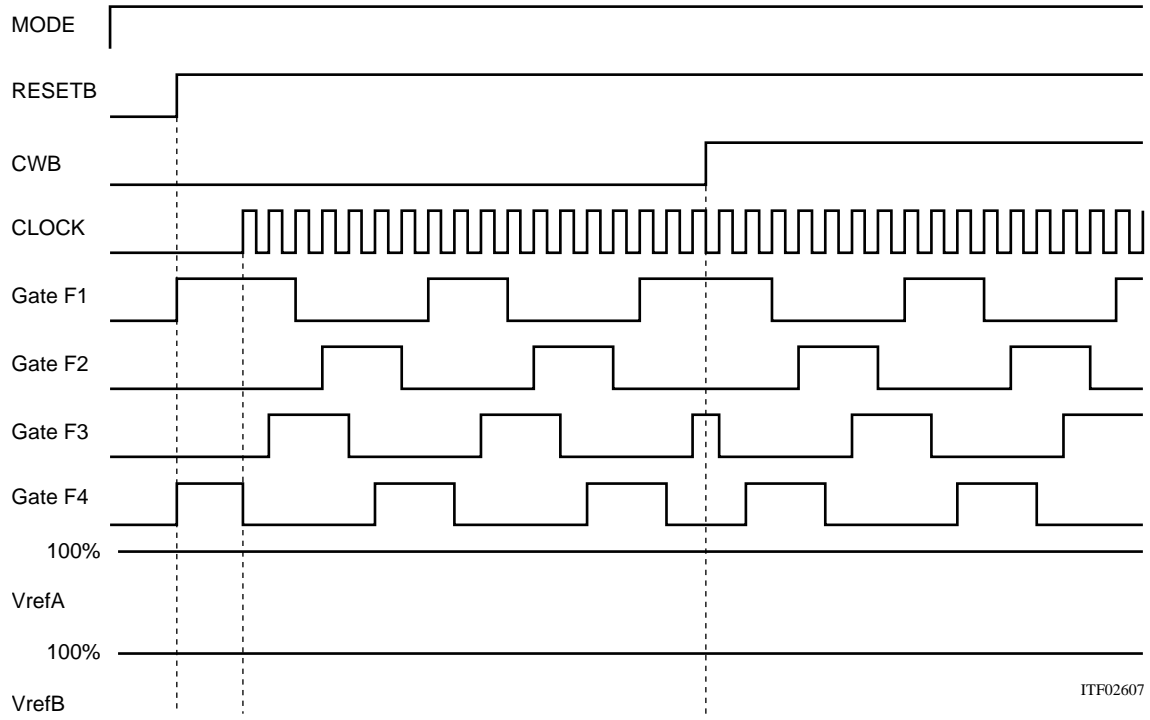


1-2 phase excitation

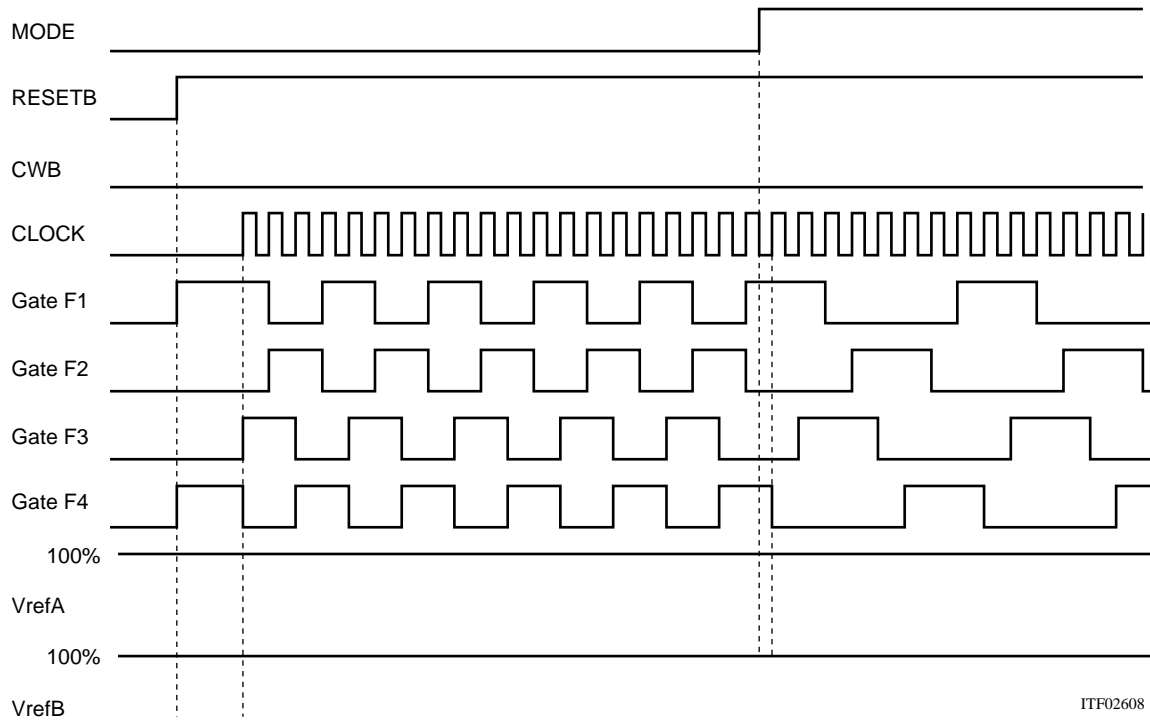


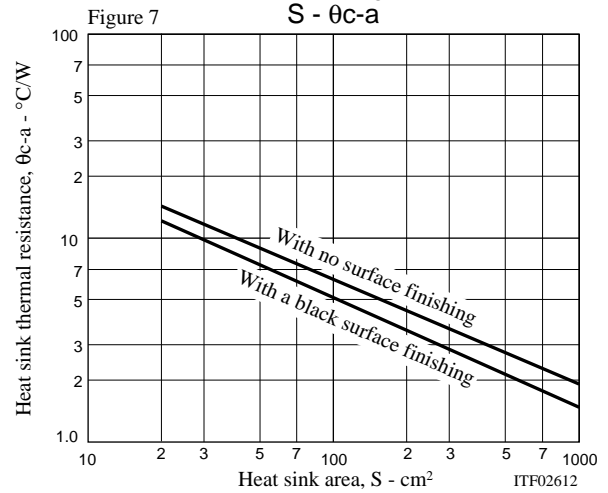
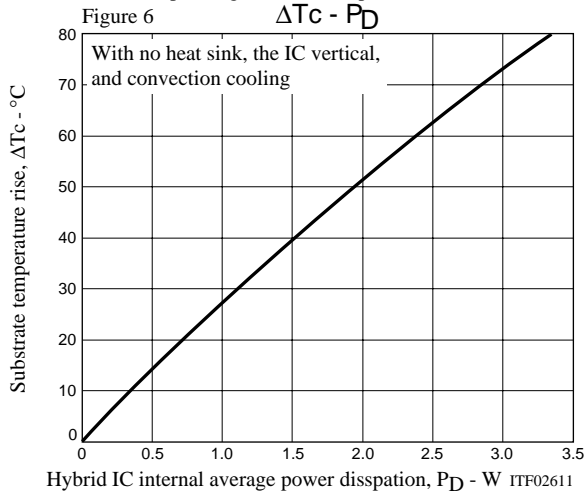
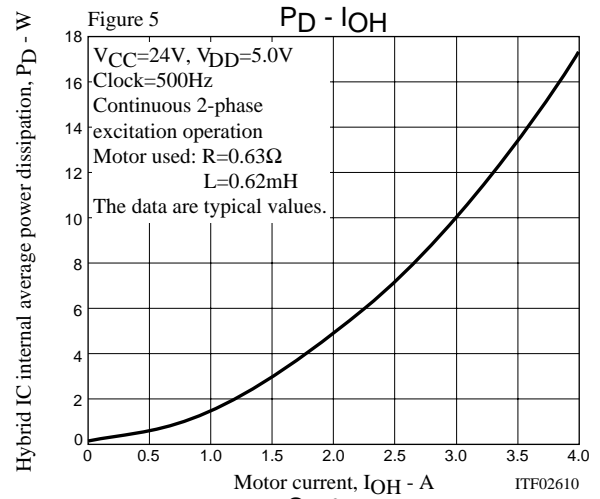
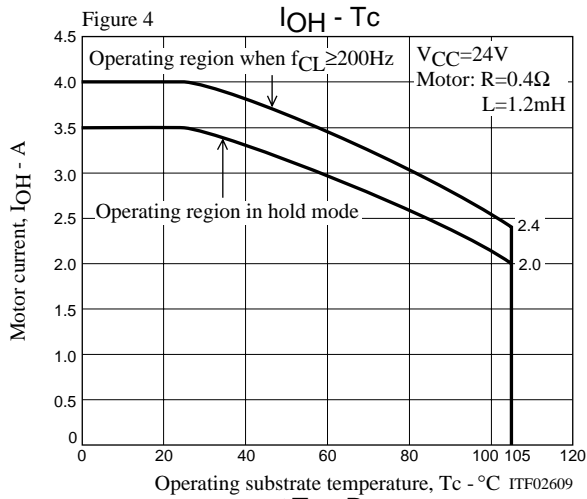
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1-2 phase excitation (CWB)



Switching from 2-phase to 1-2 phase excitation





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