STV7778S

DEFLECTION PROCESSOR FOR MULTISYNC MONITOR

HORIZONTAL

- DUAL PLL CONCEPT
- SELF-ADAPTIVE (30 TO 70kHz)
- X-RAY PROTECTION INPUT
- DC ADJUSTABLE DUTY-CYCLE
- INTERNAL 1st PLL LOCK/UNLOCK IDENTIFICATION
- WIDE RANGE DC CONTROLLED H-POSITION
- ON/OFF SWITCH (FOR PWR MANAGEMENT)
- TWO H-DRIVE POLARITIES

VERTICAL

- VERTICAL RAMP GENERATOR
- 45 TO 120Hz AGC LOOP
- DC CONTROLLED V-AMP, V-POS, S-AMP AND S-CENTERING
- ON/OFF SWITCH

B+ REGULATOR

- INTERNAL PWM GENERATOR FOR B+ CURRENT MODE STEP-UP CONVERTER
- DC ADJUSTABLE B+ VOLTAGE
- OUTPUT PULSES SYNCHRONISED ON HORIZONTAL FREQUENCY
- INTERNAL MAX CURRENT LIMITATION

EWPCC

- VERTICAL PARABOLA GENERATOR WITH DC CONTROLLED KEYSTONE AND AMPLITUDE

GENERAL

- COMPARED WITH THE STV7778, THE STV7778S HAS AN INTERNAL METAL SHIELD PROTECTION AGAINST OVERVOLTAGE.
- POS/NEG H AND V SYNC POL
- SEPARATED H AND V TTL INPUT
- SAFETY BLANKING OUTPUT

DESCRIPTION

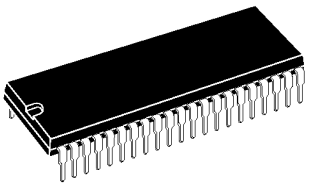
The STV7778S is a monolithic integrated circuit assembled in a 42 pins shrunk dual in line plastic package.

The goal of this IC is to control all the functions related to the horizontal and vertical deflection in a multimodes or multisync monitor.

As can be seen in the block diagram, the STV7778S includes the following functions :

- Positive or Negative sync polarities,
- Auto-sync horizontal processing,
- H-PLL lock/unlock identification,
- Auto-sync Vertical processing,
- East/West signal processing block,
- B+ controller,
- Safety blanking output.

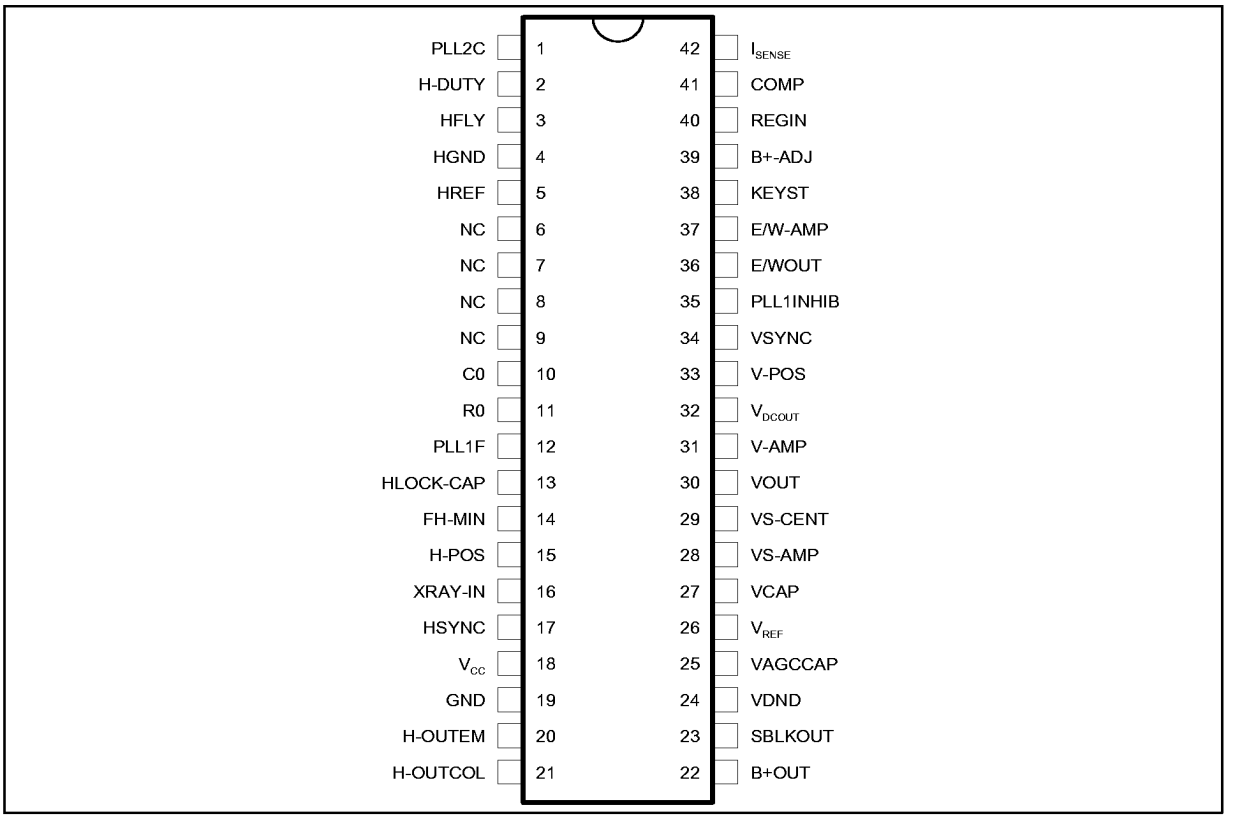
An internal metal shield give to the STV7778S more immunity against electromagnetic and electrostatic fields, and therefore, additional safety for critical applications (for example, in case of CRTs with small coated area).



SHRINK42
(Plastic Package)

ORDER CODE : STV7778S

PIN CONNECTIONS

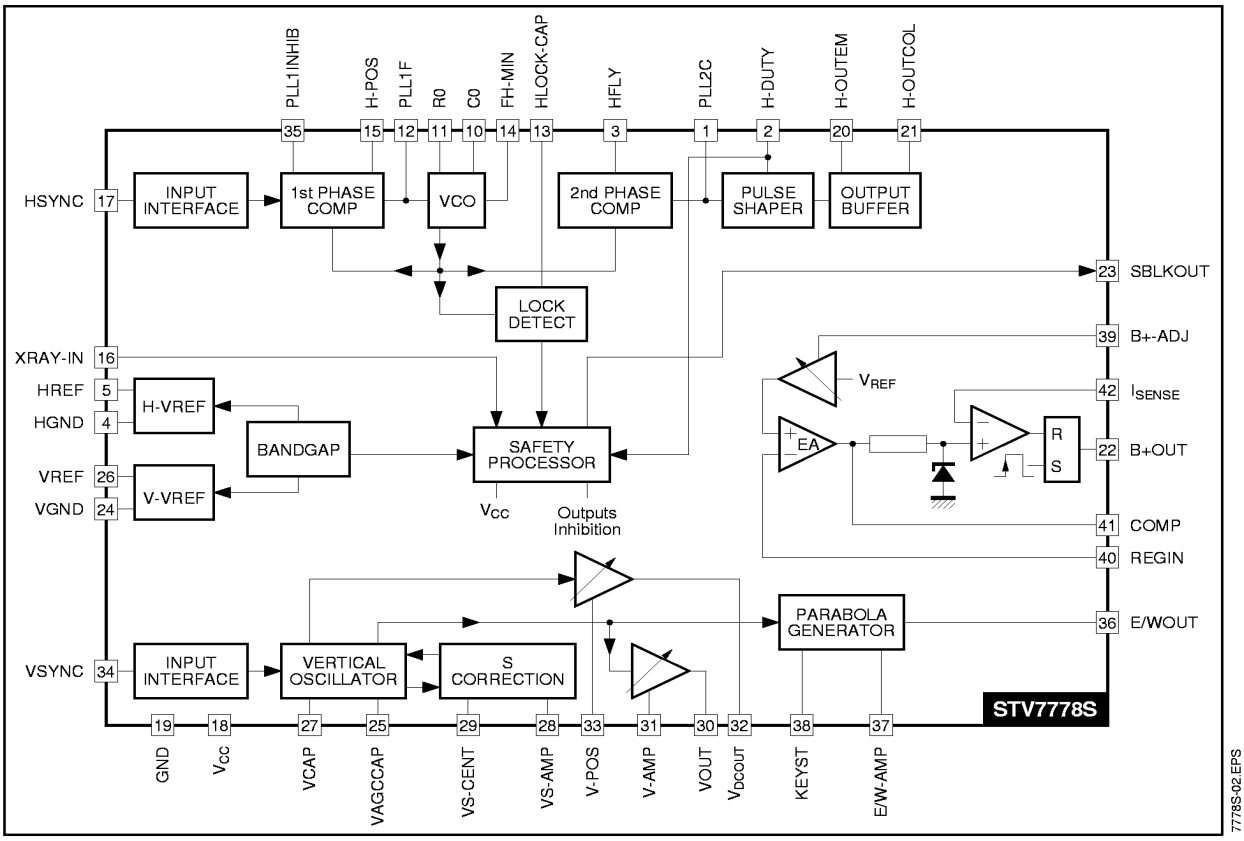


PIN-OUT DESCRIPTION

Pin N°	Name	Function
1	PLL2C	Second PLL Loop Filter
2	H-DUTY	DC Control of Horizontal Drive Output Pulse Duty-cycle. If this pin is grounded, the horizontal and vertical outputs are inhibited. By connecting a capacitor on this pin a soft-start function may be realized on h-drive output.
3	H-FLY	Horizontal Flyback Input (Positive Polarity)
4	H-GND	Horizontal Section Ground. Must be connected only to components related to H blocks.
5	H-REF	Horizontal Section Reference Voltage. Must be filtered by capacitor to Pin 4
6	NC	
7	NC	
8	NC	
9	NC	
10	C0	Horizontal Oscillator Capacitor. To be connected to Pin 4.
11	R0	Horizontal Oscillator Resistor. To be connected to Pin 4.
12	PLL1F	First PLL Loop Filter. To be connected to Pin 4.
13	HLOCK-CAP	First PLL Lock/Unlock Time Constant Capacitor. Capacitor filtering the frequency change detected on Pin13. When frequency is changing, a blanking pulse is generated on Pin 23, the duration of this pulse is proportionnal to the capacitor on Pin 13. To be connected to Pin 4.
14	FH-MIN	DC Control for Free Running Frequency Setting. Comming from DAC output or DC voltage generated by a resistor bridge connected between Pin 5 and 4.
15	H-POS	DC Control for Horizontal Centering
16	XRAY-IN	X-RAY Protection Input (with internal latch function)
17	H-SYNC	TTL Horizontal Sync Input
18	V_{CC}	Supply Voltage (12V Typical)
19	GND	Ground
20	H-OUTEM	Horizontal Drive Output (emiter of internal transistor)
21	H-OUTCOL	Horizontal Drive Output (open collector of internal transistor)
22	B+ OUT	B+ PWM Regulator Output
23	SBLK OUT	Safety Blanking Output. Activated during frequency changes, when X-RAY input is triggered or when VS is too low.
24	VGND	Vertical Section Signal Ground
25	VAGCCAP	Memory Capacitor for Automatic Gain Control Loop in Vertical Ramp Generator
26	V_{REF}	Vertical Section Reference Voltage
27	VCAP	Vertical Sawtooth Generator Capacitor
28	VS-AMP	DC Control of Vertical S Shape Amplitude
29	VS-CENT	DC Control of Vertical S Centering
30	VOUT	Vertical Ramp Output (with frequency independant amplitude and S-correction)
31	V-AMP	DC Control of Vertical Amplitude Adjustment
32	V_{DCOUT}	Vertical Position Reference Voltage Output Temperature Matched with V-AMP Output
33	V-POS	DC Control of Vertical Position Adjustment
34	VSYNC	Vertical TTL Sync Input
35	PLL1INHIB	TTL Input for PLL1 Output Current Inhibition (To be used in case of comp sync input signal)
36	E/WOUT	East/West Pincushion Correction Parabola Output
37	E/W-AMP	DC Control of East/West Pincushion Correction Amplitude
38	KEYST	DC Control of Keystone Correction
39	B+ ADJ	DC Control of B+ Adjustment
40	REGIN	Regulation Input of B+ Control Loop
41	COMP	B+ Error Amplifier Output for Frequency Compensation and Gain Setting
42	I_{SENSE}	Sensing of External B+ Switching Transistor Emiter Current

7778S-01.TBL

BLOCK DIAGRAM



ABSOLUTE MAX RATING

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage (Pin 18)		13.5	V
V_{IN}	Max Voltage on	Pins 2, 14, 15, 28, 29, 31, 33, 37, 38, 39 Pin 3 Pins 17, 34 Pin 40 Pin 42 Pin 16	8 1.8 6 8 8 6	V
VESD	ESD Succeptibility Human Body Model, 100pF Discharge through 1.5kΩ EIAJ Norm, 200pF Discharge through 0Ω		 2 300	 kV V
T_{stg}	Storage Temperature		-40, +150	°C
T_j	Max Operating Junction Temperature		150	°C
T_{oper}	Operating Temperature		0, +70	°C

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THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ (j-a)}$	Junction-Ambient Thermal Resistance	Max.	65	°C/W

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HORIZONTAL SECTION
Operating conditions

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
VCO						
R0min	Oscillator Resistor Min Value	Pin 11	6			kΩ
C0min	Oscillator Capacitor Min Value	Pin 10	390			pF
Fmax	Maximum Oscillator Frequency				70	kHz
HsVR	Horizontal Sync Input Voltage	Pin 17	0		5.5	V
INPUT SECTION						
MinD	Minimum Input Pulses Duration	Pin 17	1			µS
Mduty	Maximum Input Signal Duty Cycle	Pin 17			25	%
OUTPUT SECTION						
I3m	Maximum Input Peak Current on Pin 3				2	mA
HOI1	Horizontal Drive Output Max Current	Pin 20, sourced current			20	mA
HOI2	Horizontal Drive Output Max Current	Pin 21, sunk current			20	mA
DC CONTROL VOLTAGES						
DCadj	DC Voltage Range on DC Controls	V_{REF-H} = 8V, Pins 2-14-15	2		6	V

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HORIZONTAL SECTION (continued)
Electrical Characteristics (V_{CC} = 12V, T_{amb} = 25°C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
SUPPLY AND REFERENCE VOLTAGES						
V_{CC}	Supply Voltage	Pin 18	10.8	12	13.2	V
I_{CC}	Supply Current	Pin 18, See Figure 1		40	60	mA
V_{REF-H}	Reference Voltage for Horizontal Section	Pin 5	7.4	8	8.6	V
I_{REF-H}	Max Sourced Current on V_{REF-H}	Pin 5			2	mA
V_{REF-V}	Reference Voltage for Vertical Section	Pin 26	7.4	8	8.6	V
I_{REF-V}	Max Sourced Current on V_{REF-V}	Pin 26			2	mA
INPUT SECTION/PLL1						
V_{INTH}	Hor Input Threshold Voltage Pin 17	Low level voltage High level voltage	 2		0.8	V V
V_{VCO}	VCO Control Voltage	V_{REF-H} = 8V, Pin 12	1.6		6.2	V
VCOG	VCO Gain, dF/dV Pin 12	R0 = 6.49kΩ, C0 = 680pF		15		kHz/V
Hph	Horizontal Phase Adjustment (Pin 15)	% of Hor period		±10		%
FFadj	Free Running Frequency Adjustment (Pin 14)	Without H-sync Signal		±20		%
CR	PLL1 Capture Range (F0 = 27kHz) Fh Min Fh Max	See conditions on Figure 1	 70		28	 kHz kHz
PLLinh	PLL 1 Inhibition (Pin 35) PLL ON PLL OFF	 V_{35} V_{35}	 2		0.8	V
SECOND PLL AND HORIZONTAL OUTPUT SECTION						
FBth	Flyback Input Threshold Voltage	Pin 3	0.65	0.75		V
Hjit	Horizontal Jitter				150	ppm
HDmin HDmin	Minimum Hor Drive Output Duty-cycle Maximum Hor Drive Output Duty-cycle	Pin 20 or 21, V_2 = 2V Pin 20 or 21, V_2 = 6V	 45	30 50	35	% %
HDvd	Horizontal Drive Low Level Output Voltage	V_{21}-V_{20}, Iout = 20mA, Pin 20 to GND		1.1	1.7	V
HDem	Horizontal Drive High Level Output Voltage (output on Pin 20)	Pin 21 to V_{CC}, I_{OUT} = 20mA	9.5	10		V
XRAYth	X-RAY Protection Input Threshold Voltage	Pin 16		1.6	1.8	V
ISblkO	Maximum Output Current on Safety Blanking Output	I_{23}			10	mA
VSblkO	Low-Level Voltage on Safety Blanking Output	V_{23} with I_{23} = 10mA		0.25	0.5	V
Vphi2	Internal Clamping Voltage on 2nd PLL Loop Filter Output (Pin 1)	Vmin Vmax		1.6 3.2		V V
V_{OFF}	Pin 2 Threshold Voltage to Stop H-out, V-out B+out and to Activate S-BLK.OFF Mode when $V_2 < V_{OFF}$	V_2		1		V

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B+ SECTION
Operating Conditions

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
EAOI	Maximum Error Amplifier Output Current	Sourced by Pin 41 Sunk by Pin 41			0.5 2	mA mA
FeedRes	Minimum Feedback Resistor	Resistor between Pins 40 and 41	5			kΩ

7778S-06.TBL

Electrical Characteristics (V_{CC} = 12V, T_{amb} = 25°C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
OLG	Error Amplifier Open Loop Gain	At low frequency (see Note 1)		85		dB
UGBW	Unity Gain Bandwidth	(see Note 1)		6		MHz
IRI	Regulation Input Bias Current	Current sourced by Pin 40 (PNP base)		0.2		µA
EAOI	Maximum Guaranted Error Amplifier Output Current	Current sourced by Pin 41 Current sink by Pin 41	0.5 2			mA mA
CSG	Current Sense Input Voltage Gain	Pin 42		3		
MCEth	Max Curent Sense Input Threshold Voltage	Pin 42		1.2		V
ISI	Current Sense Input Bias Current	Current sunk by Pin 42 (NPN base)		1		µA
Tonmax	Maximum External Power Transistor on Time	% of H-period, @ f0 = 27kHz		75		%
B+OSV	B+ Output Low Level Saturation Voltage	V_{22} with I_{22} = 10mA		0.25		V
IVref	Internal Reference Voltage	On error amp (+) input for V_{39} = 4V		4.9		V
V_{REFADJ}	Internal Reference Voltage Adjustment	2V < V_{39} < 6V		±14		%

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EAST WEST PARABOLA GENERATOR
Electrical Characteristics (V_{CC} = 12V, T_{amb} = 25°C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Vsym	Parabola Symetry Adjustment Capability (for Keystone Adjustment ; with Pin 38)	See Figure 2 ; Internal voltage V_{38} = 2V V_{38} = 4V V_{38} = 6V		 3.2 3.5 3.8		V
Kadj	Keystone Adjustment Capability B/A ratio A/B ratio	See Figure 2 ; V_{37} = 4V V_{38} = 2V V_{38} = 6V		 2.3 2.0		
Paramp	Parabola Amplitude Adjustment Capability Maximum Amplitude on Pin 36 Maximum Ratio between Max and Min	V_{38} = 4.3V, V_{28} = 2V V_{37} = 2V 2V < V_{37} < 6V	 3.3 2.4	 3.8 3	 4.3	V

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VERTICAL SECTION
Operating Conditions

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
VSVR	Vertical Sync Input Voltage	On Pin 34	0		5.5	V

7778S-09.TBL

Electrical Characteristics (V_{CC} = 12V, T_{amb} = 25°C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{BIASP}	Pin 23-28-29 Bias Current (Current sourced by PNP base)	For $V_{23\text{-}28\text{-}29}$ = 2V		2		µA
I_{BIASN}	Pin 31 Bias Current (Current sunk by NPN base)	For V_{31} = 6V		0.5		µA
VSth	Vertical Sync Input Threshold Voltage	Pin 34; High-level Low-level	2		 0.8	V V
VSBI	Vertical Sync Input Bias Current (Current Sourced by PNP Base)	V_{34} = 0.8V		1		µA
V_{RB}	Voltage at Ramp Bottom Point	On Pin 27		2/8		$V_{REF\text{-}V}$
V_{RT}	Voltage at Ramp Top Point (with Sync)	On Pin 27		5/8		$V_{REF\text{-}V}$
V_{RTF}	Voltage at Ramp Top Point (without Sync)	On Pin 27		VRT-0.1		V
I_{R27}	Output Current Range on Pin 27 during Ramp Charging Time. Current to Charge Capacitor between Pin 27 and Ground	V_{28} = 2V (Note 2), 2V < V_{27} < 5V Min current Max current	 100	 15 135	 20	 µA µA
VSW	Minimum Vertical Sync Pulse Width	Pin 34	5			µS
VSmDut	Vertical Sync Input Maximum Duty-cycle	Pin 34			15	%
VSTD	Vertical Sawtooth Discharge Time Duration	On Pin 27, with 150nF cap		85		µS
VFRF	Vertical Free Running Frequency (V_{28} = 2V)	Measured on Pin 27, Cosc (Pin27) = 150nF		100		Hz
ASFR	AUTO-SYNC Frequency (see Note 3)	With C_{27} = 150nF ±5%	50		120	Hz
RATD	Ramp Amplitude Thermal Drift	On Pin 30 (see Note 1), (0°C < T_{amb} < 70°C)		100		ppm/°C
RAFD	Ramp Amplitude Drift Versus Frequency	V_{31} = 6V, C_{27} = 150nF, 50Hz < F < 120Hz		200		ppm/Hz
Rlin	Ramp Linearity on Pin 27 $\Delta I_{27}/I_{27}$	V_{28} = 2V, V_{25} = X = 4.3V, 2.5V < V_{27} < 4.5V		0.5		%
Rload	Minimum Load on Pin 25 for less than 1% Vertical Amplitude Drift		50			MΩ
Vpos	Vertical Position Adjustment Voltage on Pin 32	V_{33} = 2V V_{33} = 4V V_{33} = 6V	 3.65	3.2 3.5 3.8	3.3	V V V
I_{VPOS}	Max Current on Vertical Position Control Output (Pin 32)			±2		mA
Vor	Vertical Output Voltage (on Pin 30) (Peak to Peak Voltage on Pin 30)	V_{31} = 2V V_{31} = 4V V_{31} = 6V	 3.75	2 3 4	2.2	V V V
V_{OUTDC}	DC Voltage on Vertical Output (Pin30)	See Note 4		7/16		$V_{REF\text{-}V}$
V0I	Vertical Output Maximum Output Current	On Pin 30		±5		mA
dVS	Max Vertical S-Correction Amplitude (V_{28} = 2V Inhibits S-CORR; V_{28} = 6V gives Maximum S-CORR) (see Figure 3)	ΔV/V30pp at T/4 ΔV/V30pp at 3T/4		-4 +4		% %
Ccorr	C-Correction Adjustment Range Voltage on Pin 27 for Maximum Slope on the Ramp (with S-Correction) (see Figure 4)	V_{29} = 2V V_{29} = 4V V_{29} = 6V		3 3.5 4		V V V

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Notes : 1. These parameters are not tested on each unit. They are measured during our internal qualification procedure which includes characterization on batches comming from corners of our processes and also temperature characterization.
2. When 2V are applied on Pin 28 (Vertical S-Correction control), then the S-Correction is inhibited, consequently the sawtooth have a linear shape.
3. It is the frequency range for which the VERTICAL OSCILLATOR will automatically synchronize, using a single capacitor value on Pin 27 and with a constant ramp amplitude.
4. Typically 3.5V for Vertical reference voltage typical value (8V).

Figure 1 : Testing Circuit

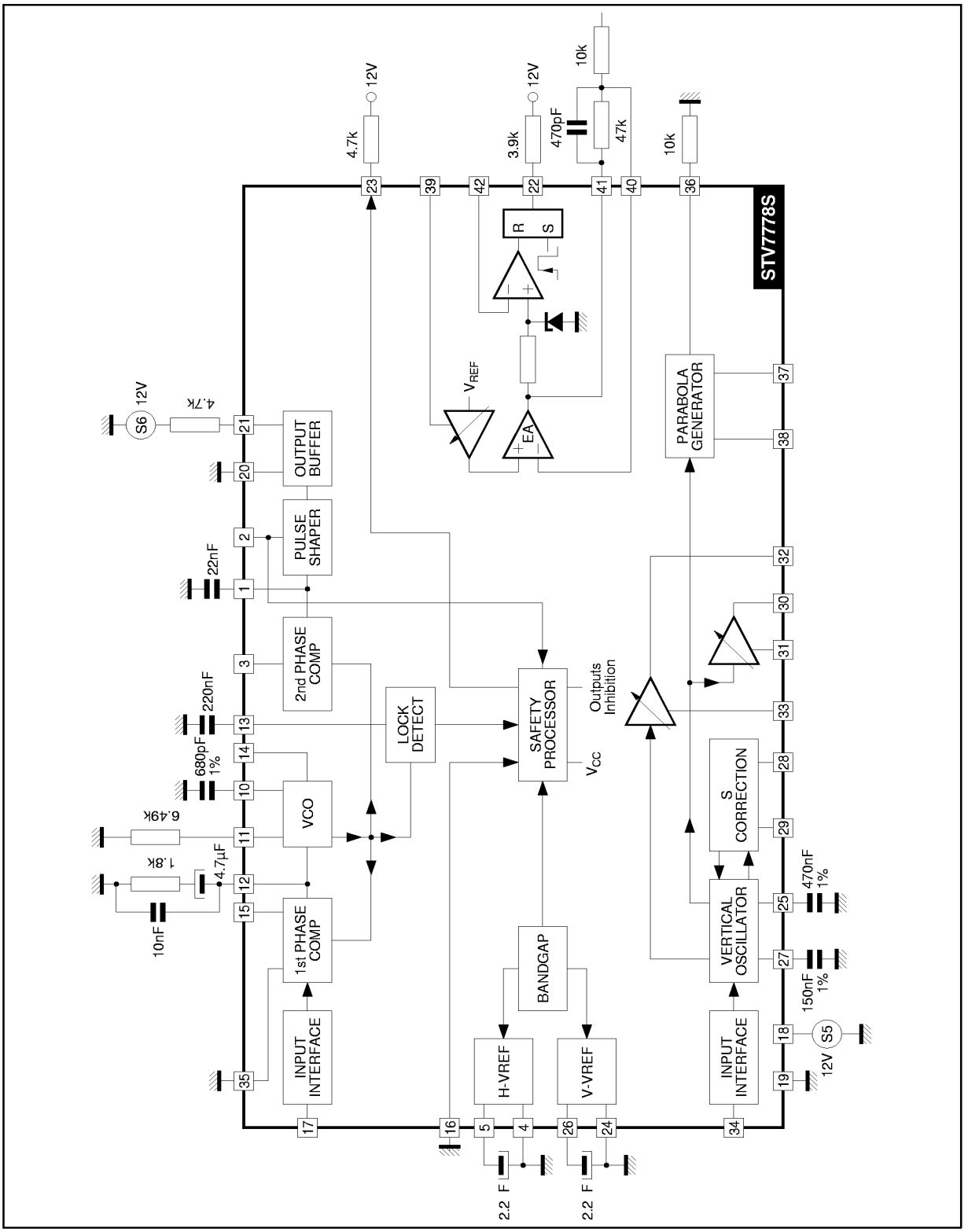


Figure 2 : Keystone Adjustment

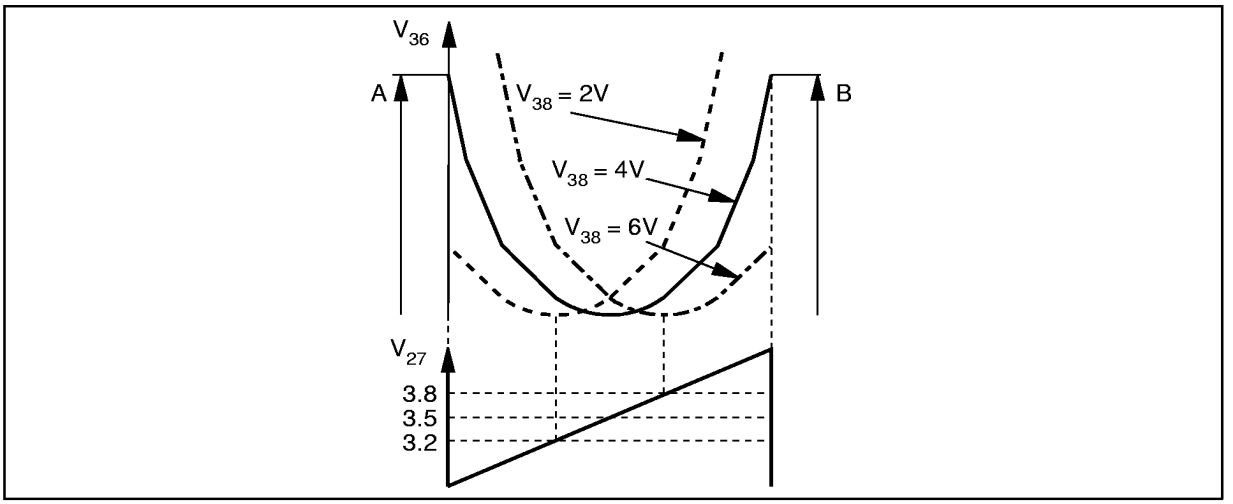


Figure 3 : S Amplitude Adjustment

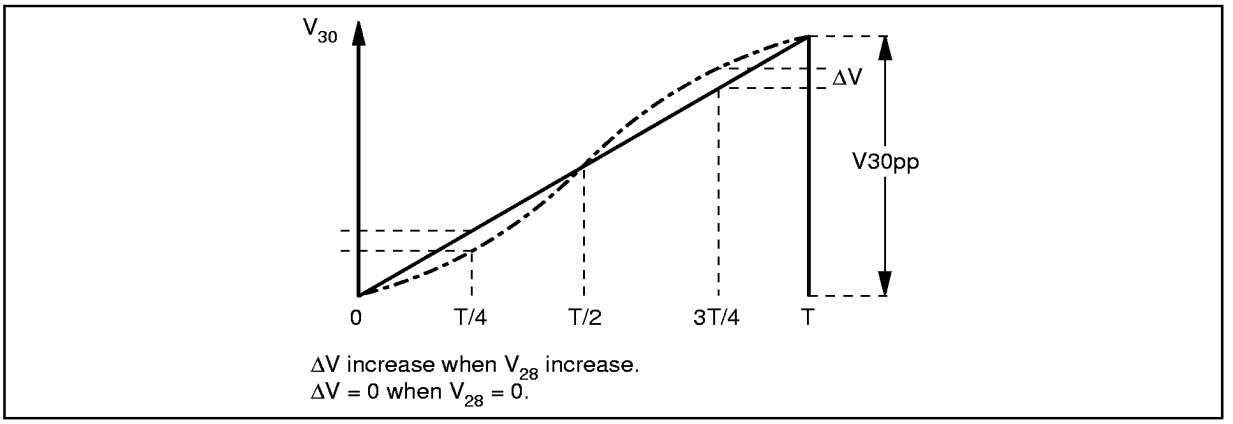
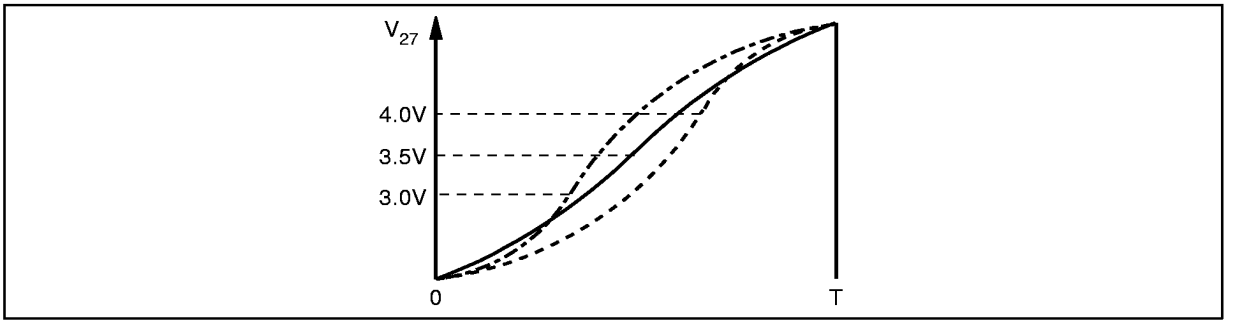
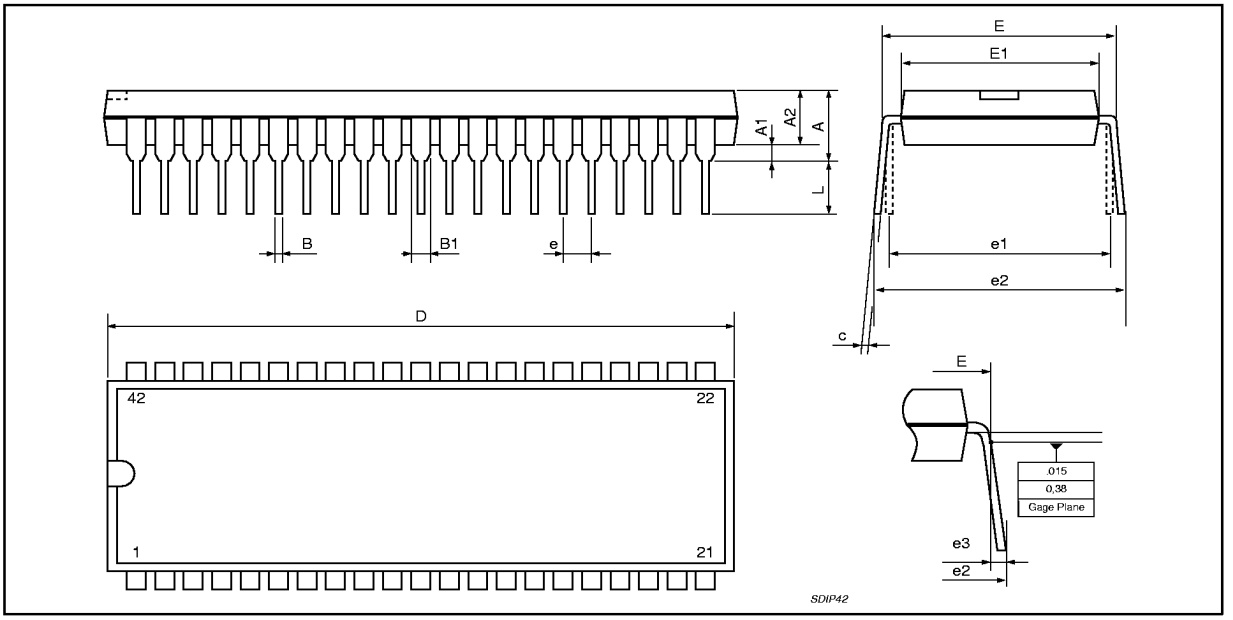


Figure 4 : C Correction Adjustment



PACKAGE MECHANICAL DATA
42 PINS - PLASTIC PACKAGE



PMSDIP42.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5.08			0.200
A1	0.51			0.020		
A2	3.05	3.81	4.57	0.120	0.150	0.180
B	0.36	0.46	0.56	0.0142	0.0181	0.0220
B1	0.76	1.02	1.14	0.030	0.040	0.045
c	0.23	0.25	0.38	0.0090	0.0098	0.0150
D	37.85	38.10	38.35	1.490	1.5	1.510
E	15.24		16.00	0.60		0.629
E1	12.70	13.72	14.48	0.50	0.540	0.570
e		1.778			0.070	
e1		15.24			0.60	
e2			18.54			0.730
e3			1.52			0.060
L	2.54	3.30	3.56	0.10	0.130	0.140

SDIP42.TBL