## FEATURES

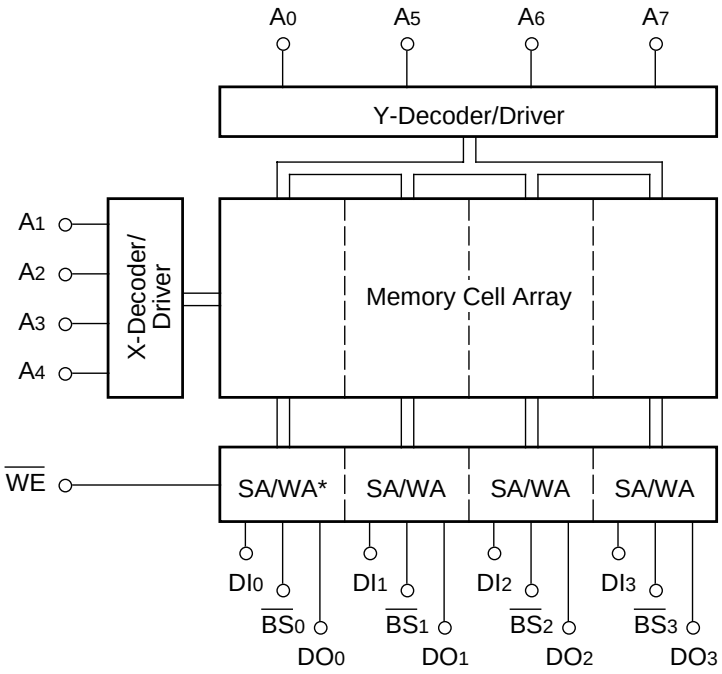
- **Address access time, $t_{AA}$: 3/4/5/7ns max.**
- **Block select access time, $t_{AB}$: 2ns max.**
- **Write pulse width, tww: 3ns min.**
- **Edge rate, tr/tf: 500ps typ.**
- **Write recovery times under 5ns**
- **Power supply current, $I_{EE}$: –250mA, –200mA for –5/7ns**
- **Superior immunity against alpha particles provides virtually no soft error sensitivity**
- **Built with advanced ASSET™ technology**
- **Fully compatible with industry standard 10K/100K ECL I/O levels**
- **Noise margins improved with on-chip voltage and temperature compensation**
- **Open emitter output for easy memory expansion**
- **Includes popular Block Select function allowing individual read/write control over blocks**
- **ESD protection of 2000V**
- **Available in 24-pin flatpack and 28-pin PLCC and MLCC packages**

## DESCRIPTION

The Synergy SY10/100/101422 are 1024-bit Random Access Memories (RAMs), designed with advanced Emitter Coupled Logic (ECL) circuitry. The devices are organized as 256-words-by-4-bits and meet the standard 10K/100K family signal levels. The SY100422 is also supply voltage-compatible with 100K ECL, while the SY101422 operates from 10K ECL supply voltage (–5.2V). All feature on-chip voltage and temperature compensation for improved noise margin.

The SY10/100/101422 employ proprietary circuit design techniques and Synergy's proprietary ASSET advanced bipolar technology to achieve extremely fast access, write pulse width and write recovery times. ASSET uses proprietary technology concepts to achieve significant reduction in parasitic capacitance while improving device packing density. Synergy's circuit design techniques, coupled with ASSET, result not only in ultra-fast performance, but also allow device operation at reduced power levels with virtually no soft error sensitivity and with outstanding device reliability in volume production.

## BLOCK DIAGRAM



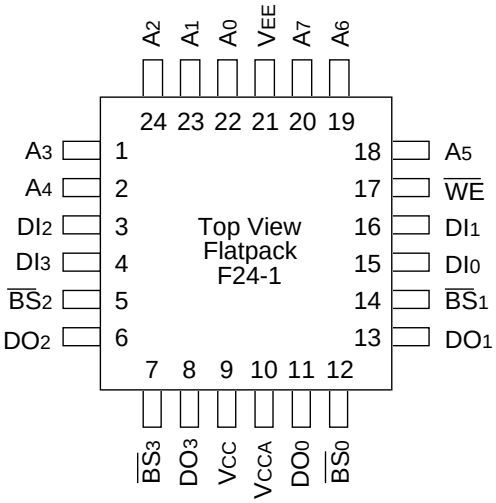

* SA = Sense Amplifier
WA = Write Amplifier

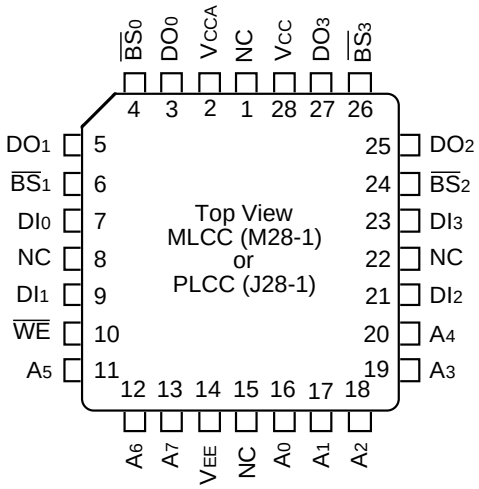




Rev.: E Amendment: /0
Issue Date: August,1999

## PIN CONFIGURATIONS




## PIN NAMES

| Label | Function |
|---|---|
| $A_0$ - $A_7$ | Address Inputs |
| $\overline{BS}_0$ - $\overline{BS}_3$ | Block Select ($\overline{BS}$) |
| $\overline{WE}$ | Write Enable |
| $DI_0$ - $DI_3$ | Data Input ($D_{IN}$) |
| $DO_0$ - $DO_3$ | Data Output ($D_{OUT}$) |
| $V_{CC}$ | GND (0V) |
| $V_{CCA}$ | Output GND (0V) |
| $V_{EE}$ | Supply Voltage |

## TRUTH TABLE

| Input | | | Output | Mode |
|---|---|---|---|---|
| $\overline{BS}$ | $\overline{WE}$ | $D_{IN}$ | | |
| H | X | X | L | Disabled |
| L | L | H | L | Write “H” |
| L | L | L | L | Write “L” |
| L | H | X | $D_{OUT}$ | Read |

**NOTE:**
H = High Voltage Level
L = Low Voltage Level
X = Don’t Care

## FUNCTIONAL DESCRIPTION

The Synergy SY10/100/101422 are 1024-bit RAMs organized as four 256-by-1-bit blocks with each block having its own Block Select ($\overline{BS}$) control signal that functions essentially like a unique chip select for the Block. The four blocks and Block Selects together make the device a 256 x 4-bit RAM. Memory cell selection is achieved by using the 8 address bits designated as $A_0$ through $A_7$. Each of the $2^8$ possible input address combinations corresponds to a unique word location in memory. The active low Block Select ($\overline{BS}$) control signals are provided for memory expansion and for independent control of each of the four 256 x 1-bit blocks of memory. The active low Write Enable ($\overline{WE}$) controls the read and write operation on the selected block or blocks. Data resident on the $D_{IN}$ inputs ($DI_0$ through $DI_3$) is written into the addressed location only when $\overline{WE}$ and the Block Select ($\overline{BS}$) associated with each of the $D_{IN}$ bits is held LOW. This allows control of the Write operation to any one, two, three or all four of the input data bits. In order to perform a read operation, $\overline{WE}$ is held high, the Block Select ($\overline{BS}$) associated with each of the four output blocks is held low, and the non-inverted output data at the addressed location is transferred to $D_{OUT}$ ($DO_0$ through $DO_3$) to be read out. This allows control of the Read operation to any one, two, three or all four of the output blocks. Open emitter outputs are provided for maximum flexibility and memory expansion by allowing output wire-OR connections. External termination of 50Ω to –2.0V or an equivalent circuit must be used to provide the specified output levels.

All outputs are forced to a logic LOW level when the RAM is being written into ($\overline{WE}$ = LOW). The output (or outputs) associated with a block (or blocks) of memory can be forced to a logic LOW low level by deselecting that block (or blocks) with its respective Block Select input ($\overline{BS_0}$ – $\overline{BS_3}$ = HIGH).

## ABSOLUTE MAXIMUM RATINGS(1)

| Symbol | Rating | Value | Unit |
|---|---|---|---|
| $V_{EE}$ | $V_{EE}$ Pin Potential to $V_{CC}$ Pin | +0.5 to –7.0 | V |
| $V_{IN}$ | Input Voltage | +0.5 to $V_{EE}$ | V |
| $I_{OUT}$ | DC Output Current (Output High) | –30 | mA |
| $T_C$ | Temperature Under Bias | –55 to +125 | °C |
| $T_{store}$ | Storage Temperature | –65 to +150 | °C |

**NOTE:**

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

## GUARANTEED OPERATING CONDITIONS

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Supply Voltage(1) | 10K | $V_{EE}$ | –5.46 | –5.2 | –4.94 | V |
| Case Temperature | | $T_C$ | 0 | — | 75 | °C |
| Supply Voltage(1) | 100K | $V_{EE}$ | –4.8 | –4.5 | –4.2 | V |
| Case Temperature | | $T_C$ | 0 | — | 85 | °C |
| Supply Voltage(1) | 101K | $V_{EE}$ | –5.46 | –5.2 | –4.94 | V |
| Case Temperature | | $T_C$ | 0 | — | 85 | °C |

**NOTE:**

1. Referenced to $V_{CC}$.

## RISE AND FALL TIME

| Parameter | Code(1) | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Output Rise Time | F<br>S | $t_r$ | — | 500<br>1500 | — | ps |
| Output Fall Time | F<br>S | $t_f$ | — | 500<br>1500 | — | ps |

**NOTE:**

1. F = Fast Edge Rate
   S = Standard Edge Rate

## CAPACITANCE

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Input Pin Capacitance | $C_{IN}$ | — | 4 | — | pF |
| Output Pin Capacitance | $C_{OUT}$ | — | 5 | — | pF |

## 10K DC ELECTRICAL CHARACTERISTICS

$V_{CC}$ = 0V; $T_C$ = 0°C to +75°C; $V_{EE}$ = –5.2V; Airflow > 2.5m/s; Output Load = 50Ω to –2.0V

| Symbol | Parameter | Tc | Min. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage | 0°C<br>+25°C<br>+75°C | –1000<br>–960<br>–900 | –840<br>–810<br>–720 | mV | $V_{IN}$ = $V_{IH}$ Max. or $V_{IL}$ Min. |
| $V_{OL}$ | Output Low Voltage | 0°C<br>+25°C<br>+75°C | –1870<br>–1850<br>–1830 | –1665<br>–1650<br>–1625 | mV | $V_{IN}$ = $V_{IH}$ Max. or $V_{IL}$ Min. |
| $V_{OHC}$ | Output High Voltage | 0°C<br>+25°C<br>+75°C | –1020<br>–980<br>–920 | —<br>—<br>— | mV | $V_{IN}$ = $V_{IH}$ Min. or $V_{IL}$ Max. |
| $V_{OLC}$ | Output Low Voltage | 0°C<br>+25°C<br>+75°C | —<br>—<br>— | –1645<br>–1630<br>–1605 | mV | $V_{IN}$ = $V_{IH}$ Min. or $V_{IL}$ Max. |
| $V_{IH}$ | Input High Voltage | 0°C<br>+25°C<br>+75°C | –1145<br>–1105<br>–1045 | –840<br>–810<br>–720 | mV | Guaranteed Input Voltage High for All Inputs |
| $V_{IL}$ | Input Low Voltage | 0°C<br>+25°C<br>+75°C | –1870<br>–1850<br>–1830 | –1490<br>–1475<br>–1450 | mV | Guaranteed Input Voltage Low for All Inputs |
| $I_{IH}$ | Input High Current | 0°C to+ 75°C | 0.0 | 20 | µA | $V_{IN}$ = $V_{IH}$ Max. |
| $I_{IL}$ | Input Low Current | 0°C to +75°C | –2 | 2 | µA | $V_{IN}$ = $V_{IL}$ Min. |
| $I_{IL}$ | $\overline{BS}$ Input Low Current | 0°C to +75°C | 30 | 170 | µA | $V_{IN}$ = $V_{IL}$ Min. |
| $I_{IH}$ | $\overline{BS}$ Input High Current | 0°C to +75°C | 40 | 220 | µA | $V_{IN}$ = $V_{IH}$ Max. |
| $I_{IL}$ | $\overline{WE}$ Input Low Current | 0°C to +75°C | –2 | 35 | µA | $V_{IN}$ = $V_{IL}$ Min. |
| $I_{IH}$ | $\overline{WE}$ Input High Current | 0°C to +75°C | 0.0 | 60 | µA | $V_{IN}$ = $V_{IH}$ Max. |
| $I_{EE}$ | Power Supply Current -3ns, -4ns<br>Power Supply Current -5ns, -7ns | 0°C to +75°C | –250<br>–200 | —<br>— | mA | All Inputs and Outputs Open |

## 100K/101K DC ELECTRICAL CHARACTERISTICS

$V_{CCA}$ = 0V  $V_{EE}$ = –4.5V (100K)  $T_C$ = 0°C to +85°C  Airflow > 2.5m/s
$V_{CC}$ = 0V  $V_{EE}$ = –5.2V (101K)  Output Load = 50Ω to –2.0V

| Symbol | Parameter | Min. | Max. | Unit | Condition |
|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage | –1025 | –880 | mV | $V_{IN}$ = $V_{IH}$ Max. or $V_{IL}$ Min. |
| $V_{OL}$ | Output Low Voltage | –1810 | –1620 | mV | $V_{IN}$ = $V_{IH}$ Max. or $V_{IL}$ Min. |
| $V_{OHC}$ | Output High Voltage | –1035 | — | mV | $V_{IN}$ = $V_{IH}$ Min. or $V_{IL}$ Max. |
| $V_{OLC}$ | Output Low Voltage | — | –1610 | mV | $V_{IN}$ = $V_{IH}$ Min. or $V_{IL}$ Max. |
| $V_{IH}$ | Input High Voltage | –1165 | –880 | mV | Guaranteed Input Voltage High for All Inputs |
| $V_{IL}$ | Input Low Voltage | –1810 | –1475 | mV | Guaranteed Input Voltage Low for All Inputs |
| $I_{IH}$ | Input High Current | 0.0 | 20 | µA | $V_{IN}$ = $V_{IH}$ Max. |
| $I_{IL}$ | Input Low Current | –2 | 2 | µA | $V_{IN}$ = $V_{IL}$ Min. |
| $I_{IL}$ | $\overline{BS}$ Input Low Current | 30 | 170 | µA | $V_{IN}$ = $V_{IL}$ Min. |
| $I_{IH}$ | $\overline{BS}$ Input High Current | 40 | 220 | µA | $V_{IN}$ = $V_{IH}$ Max. |
| $I_{IL}$ | $\overline{WE}$ Input Low Current | –2 | 35 | µA | $V_{IN}$ = $V_{IL}$ Min. |
| $I_{IH}$ | $\overline{WE}$ Input High Current | 0.0 | 60 | µA | $V_{IN}$ = $V_{IH}$ Max. |
| $I_{EE}$ | Power Supply Current -3ns, -4ns<br>Power Supply Current -5ns, -7ns | –250<br>–200 | —<br>— | mA | All Inputs and Outputs Open |

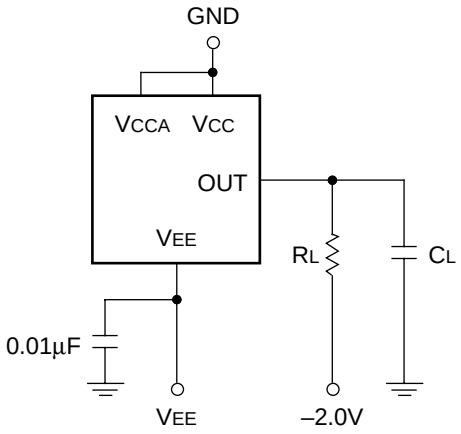
# AC ELECTRICAL CHARACTERISTICS

## AC TEST CONDITIONS

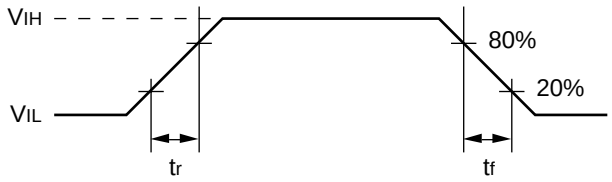
$V_{CC} = V_{CCA} = 0V$ Output Load = 50Ω to –2.0V
$V_{EE} = –5.2V \pm 5\%$(10K) $T_C$ = 0°C to +75°C (10K)
$V_{EE} = –4.5V \pm 0.3V$(100K) $T_C$ = 0°C to +85°C (100K/101K)
$V_{EE} = –5.2V \pm 5\%$(101K) Airflow > 2.5m/s

| | $T_C$ | $V_{IH}$ | $V_{IL}$ |
|---|---|---|---|
| 10K | 0°C<br>+25°C<br>+75°C | –0.933V<br>–0.90V<br>–0.863V | –1.733V<br>–1.70V<br>–1.663V |
| 100/101K | 0°C to +85°C | –0.90V | –1.70V |

**Loading Condition**




**Input Pulse**




$t_r = t_f$ = 1.0ns typ.

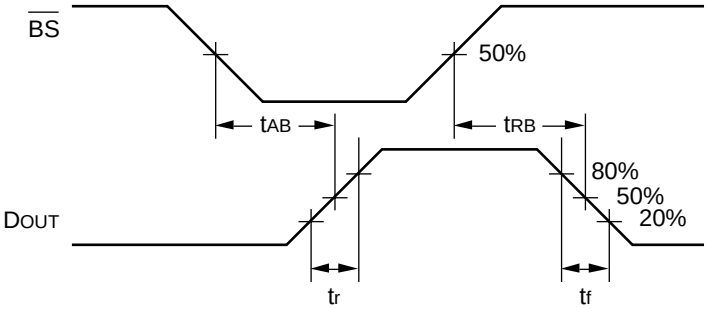
OUTPUT LOAD: $R_L$ = 50Ω
$C_L$ = 5pF* (typ.)
* (Modeled as 50Ω transmission line terminated to –2V.)

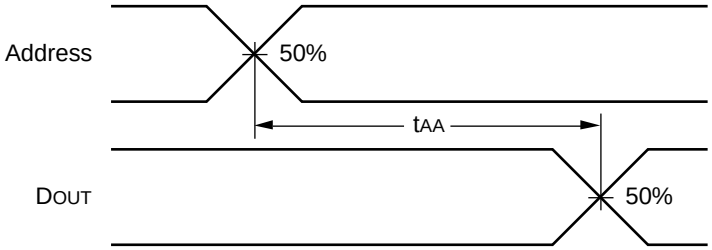
**NOTE:** All timing measurements referenced to 50% input levels.

## READ CYCLE

| Symbol | | Parameter | SY10422-3 SY100422-3 SY101422-3 | | SY10422-4 SY100422-4 SY101422-4 | | SY10422-5 SY100422-5 SY101422-5 | | SY10422-7 SY100422-7 SY101422-7 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{AA}$ | TAVQV | Address Access Time | — | 3 | — | 4 | — | 5 | — | 7 | ns |
| $t_{AB}$ | TBSLQV | Block Select Access Time | — | 2 | — | 2 | — | 3 | — | 3 | ns |
| $t_{RB}$ | TBSHQL | Block Select Recovery Time | — | 2 | — | 2 | — | 3 | — | 3 | ns |

## READ CYCLE TIMING DIAGRAM

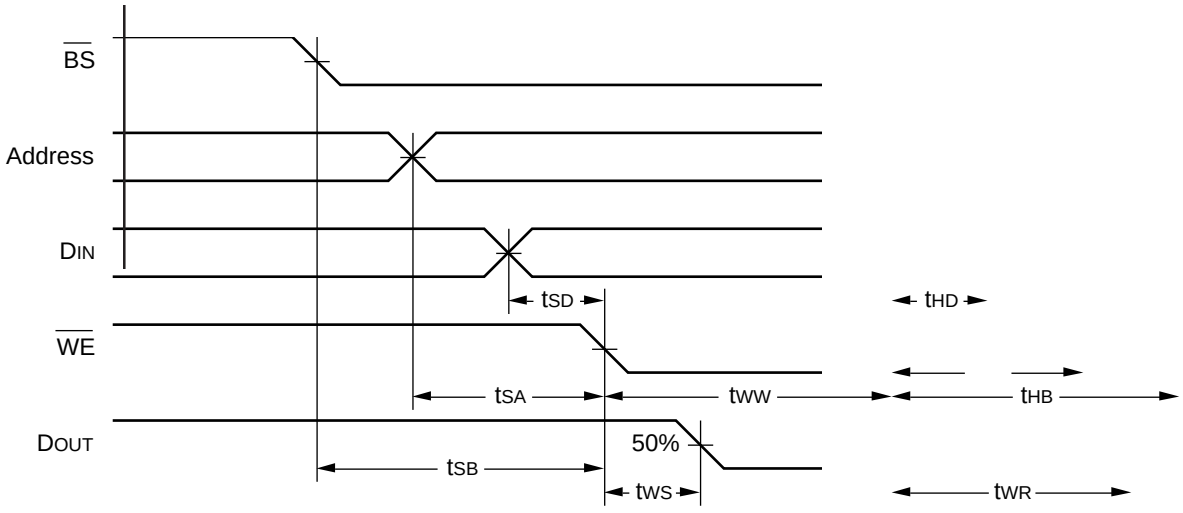


## READ CYCLE

| Symbol | | Parameter | SY10422-3 SY100422-3 SY101422-3 | | SY10422-4 SY100422-4 SY101422-4 | | SY10422-5 SY100422-5 SY101422-5 | | SY10422-7 SY100422-7 SY101422-7 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{WW}$ | TWLWH | Write Pulse Width | 3 | — | 4 | — | 5 | — | 5 | — | ns |
| $t_{WS}$ | TWLQL | Write Disable Time | — | 3 | — | 4 | — | 4 | — | 4 | ns |
| $t_{WR}$ | TWHQV | Write Recovery Time | — | 3 | — | 4 | — | 4 | — | 4 | ns |
| $t_{SA}$ | TAVWL | Address Set-Up Time | 1 | — | 1 | — | 1 | — | 1 | — | ns |
| $t_{SB}$ | TBSLWL | Block Select Set-Up Time | 0 | — | 0 | — | 1 | — | 1 | — | ns |
| $t_{SD}$ | TDVWL | Data Set-Up Time | 0 | — | 0 | — | 1 | — | 1 | — | ns |
| $t_{HA}$ | TWHAX | Address Hold Time | 1 | — | 1 | — | 1 | — | 1 | — | ns |
| $t_{HB}$ | TWHBSX | Block Select Hold Time | 1 | — | 1 | — | 1 | — | 1 | — | ns |
| $t_{HD}$ | TWHDX | Data Hold Time | 1 | — | 1 | — | 1 | — | 1 | — | ns |

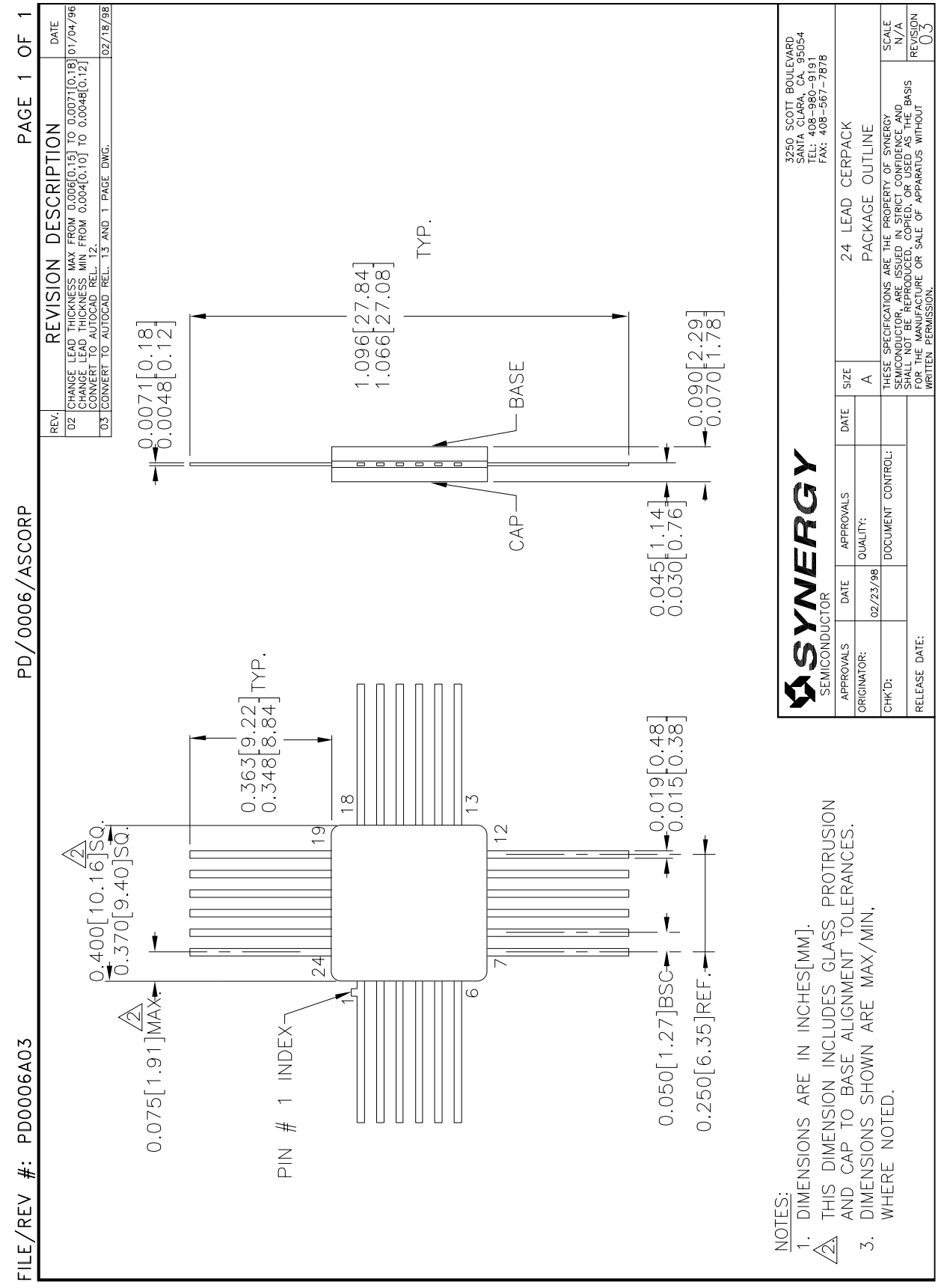
## WRITE CYCLE TIMING DIAGRAM



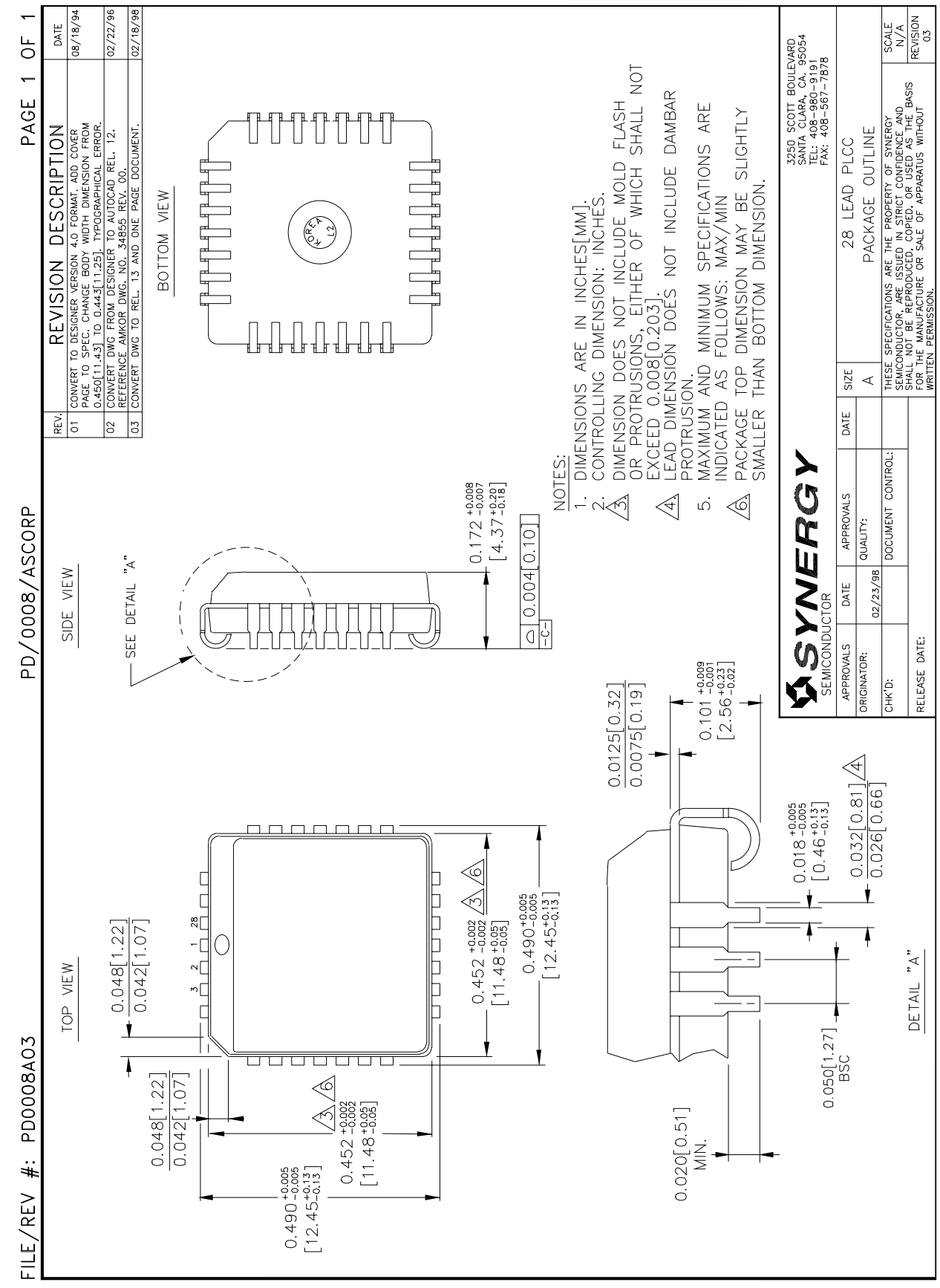
## PRODUCT ORDERING CODE

| Speed (ns) | Ordering Code | Edge Rate | Package Type | Operating Range |
|---|---|---|---|---|
| 3 | SY10/100/101422-3FCF<br>SY10/100/101422-3MCF | Fast<br>Fast | F24-1<br>M28-1 | Commercial<br>Commercial |
| 4 | SY10/100/101422-4FCF<br>SY10/100/101422-4MCF | Fast<br>Fast | F24-1<br>M28-1 | Commercial<br>Commercial |
| 5 | SY10/100/101422-5FCS<br>SY10/100/101422-5JCS | Standard<br>Standard | F24-1<br>J28-1 | Commercial<br>Commercial |
| 7 | SY10/100/101422-7FCS<br>SY10/100/101422-7JCS | Standard<br>Standard | F24-1<br>J28-1 | Commercial<br>Commercial |

## 24 LEAD CERPACK (F24-1)



## 28 LEAD PLASTIC LEADED CHIP CARRIER (J28-1)



## 28 LEAD METAL QUAD PLASTIC LEADER CHIP CARRIER (M28-1)