

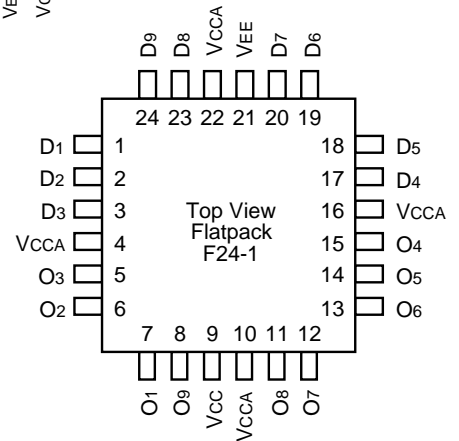
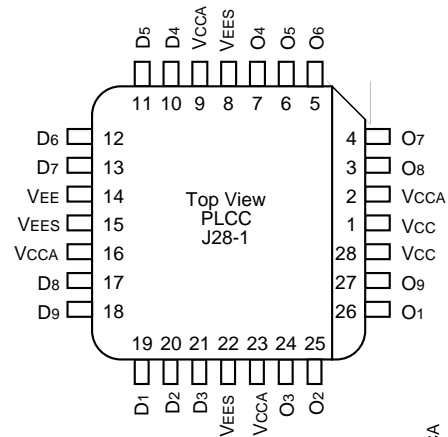
**FEATURES**

- Max. propagation delay of 700ps
- IEE min. of -55mA
- Extended supply voltage option:  
VEE = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- Internal 75KΩ input pull-down resistors
- 70% faster than Fairchild 300K at lower power
- Function and pinout compatible with Fairchild F100K
- Available in 24-pin CERPACK and 28-pin PLCC packages

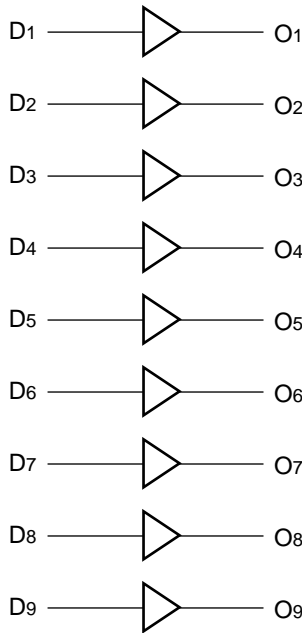
**DESCRIPTION**

The SY100S322 is an ultra-fast buffer designed for use in high-performance ECL systems. The device provides nine non-inverting buffers with single-ended outputs. The inputs on the device have 75KΩ pull-down resistors.

**PIN CONFIGURATIONS**



**BLOCK DIAGRAM**



**PIN NAMES**

Pin	Function
D1 – D9	Data Inputs
O1 – O9	Data Outputs
VEES	VEE Substrate
VCCA	Vcco for ECL Outputs

## LOGIC EQUATION

$O_n = D_n, n = 1 \text{ to } 9$

## DC ELECTRICAL CHARACTERISTICS

$V_{EE} = -4.2\text{V}$  to  $-5.5\text{V}$  unless otherwise specified,  $V_{CC} = V_{CCA} = \text{GND}$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
$I_{IH}$	Input HIGH Current	—	—	200	$\mu\text{A}$	$V_{IN} = V_{IH} (\text{Max.})$
$I_{EE}$	Power Supply Current	-55	-41	-25	mA	Inputs Open

## AC ELECTRICAL CHARACTERISTICS

### CERPACK

$V_{EE} = -4.2\text{V}$  to  $-5.5\text{V}$  unless otherwise specified,  $V_{CC} = V_{CCA} = \text{GND}$

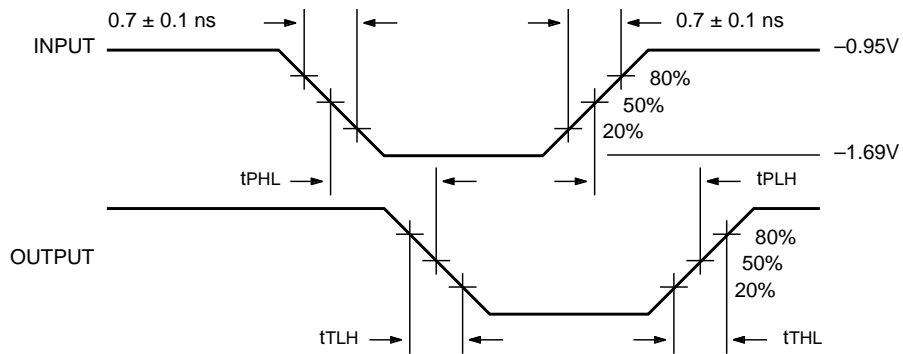
Symbol	Parameter	$T_A = 0^\circ\text{C}$		$T_A = +25^\circ\text{C}$		$T_A = +85^\circ\text{C}$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
$t_{PLH}$ $t_{PHL}$	Propagation Delay Data to Output	300	800	300	800	300	800	ps	
$t_{TLH}$ $t_{THL}$	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

### PLCC

$V_{EE} = -4.2\text{V}$  to  $-5.5\text{V}$  unless otherwise specified,  $V_{CC} = V_{CCA} = \text{GND}$

Symbol	Parameter	$T_A = 0^\circ\text{C}$		$T_A = +25^\circ\text{C}$		$T_A = +85^\circ\text{C}$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
$t_{PLH}$ $t_{PHL}$	Propagation Delay Data to Output	300	700	300	700	300	700	ps	
$t_{TLH}$ $t_{THL}$	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

**TIMING DIAGRAM**



**Propagation Delay and Transition Times**

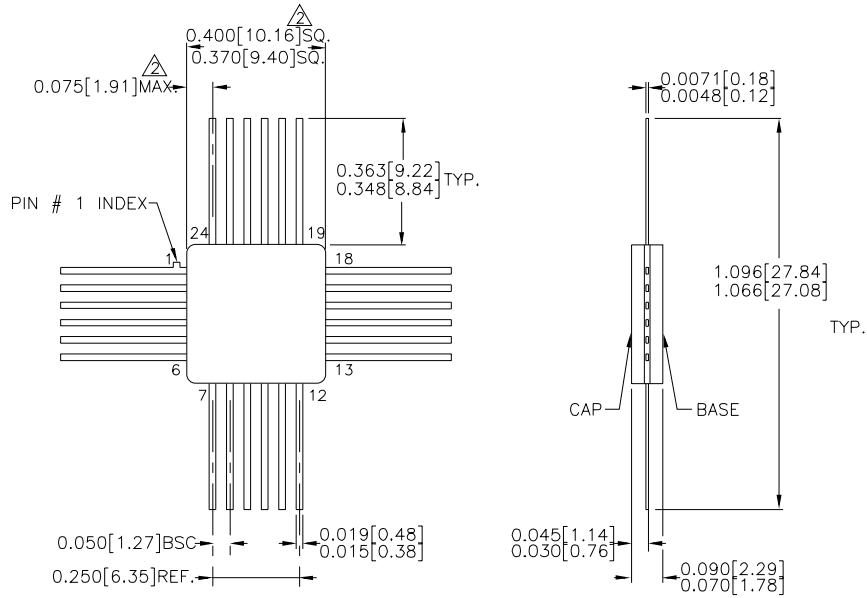
**NOTE:**

$V_{EE} = -4.2$  V to  $-5.5$  V unless otherwise specified,  $V_{CC} = V_{CCA} = GND$

**PRODUCT ORDERING CODE**

Ordering Code	Package Type	Operating Range
SY100S322FC	F24-1	Commercial
SY100S322JC	J28-1	Commercial
SY100S322JCTR	J28-1	Commercial

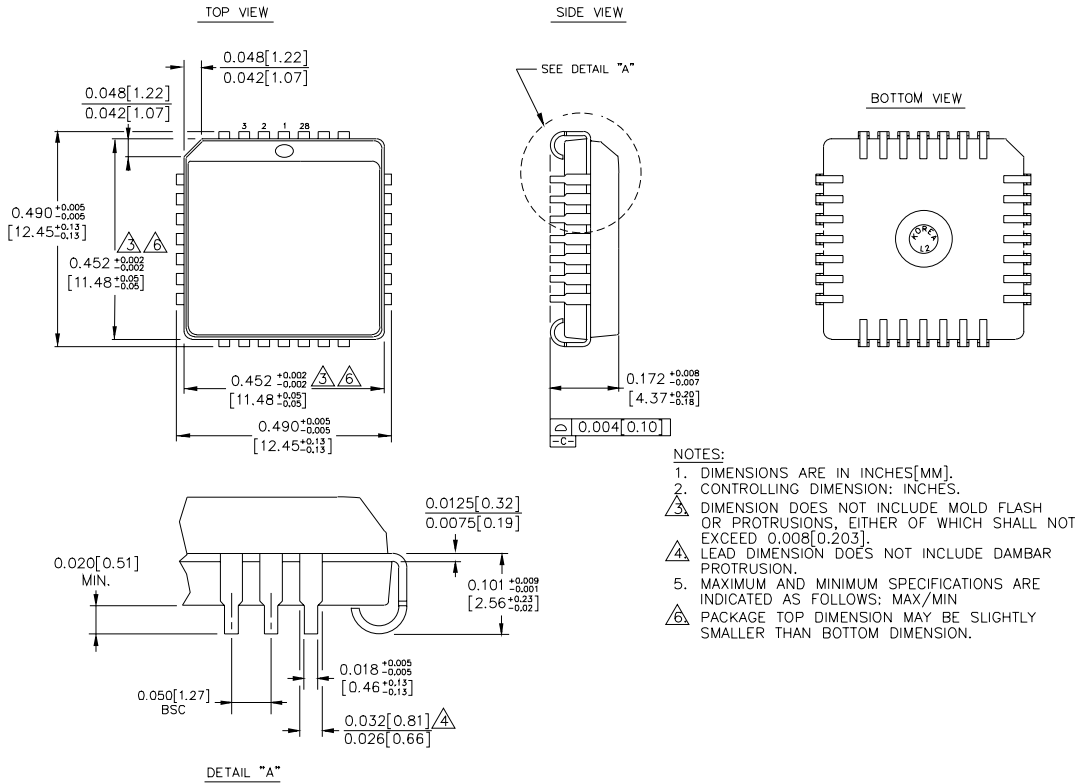
**24 LEAD CERPACK (F24-1)**



- NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
  2. THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.
  3. DIMENSIONS SHOWN ARE MAX/MIN, WHERE NOTED.

Rev. 03

**28 LEAD PLCC (J28-1)**



Rev. 03

**MICREL-SYNERGY 3250 SCOTT BOULEVARD SANTA CLARA CA 95054 USA**

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