

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

# TC74VCX162841FT

## Low-Voltage 20-Bit D-Type Latch with 3.6-V Tolerant Inputs and Outputs

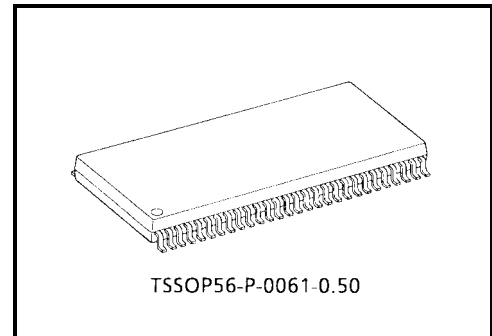
The TC74VCX162841FT is a high-performance CMOS 20-bit D-type latch. Designed for use in 1.8-V, 2.5-V or 3.3-V systems, it achieves high-speed operation while maintaining the CMOS low power dissipation.

It is also designed with overvoltage tolerant inputs and outputs up to 3.6 V.

The TC74VCX162841FT can be used as two 10-bit latches or one 20-bit latch. The 20 latches are transparent D-type latches. The device has noninverting data (D) inputs and provides true data at its outputs. While the latch-enable (1LE or 2LE) input is high, the Q outputs of the corresponding 10-bit latch follow the D inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs. When the OE input is high, the outputs are in a high-impedance state. This device is designed to be used with 3-state memory address drivers, etc.

The 26- $\Omega$  series resistor helps reducing output overshoot and undershoot without external resistor.

All inputs are equipped with protection circuits against static discharge.

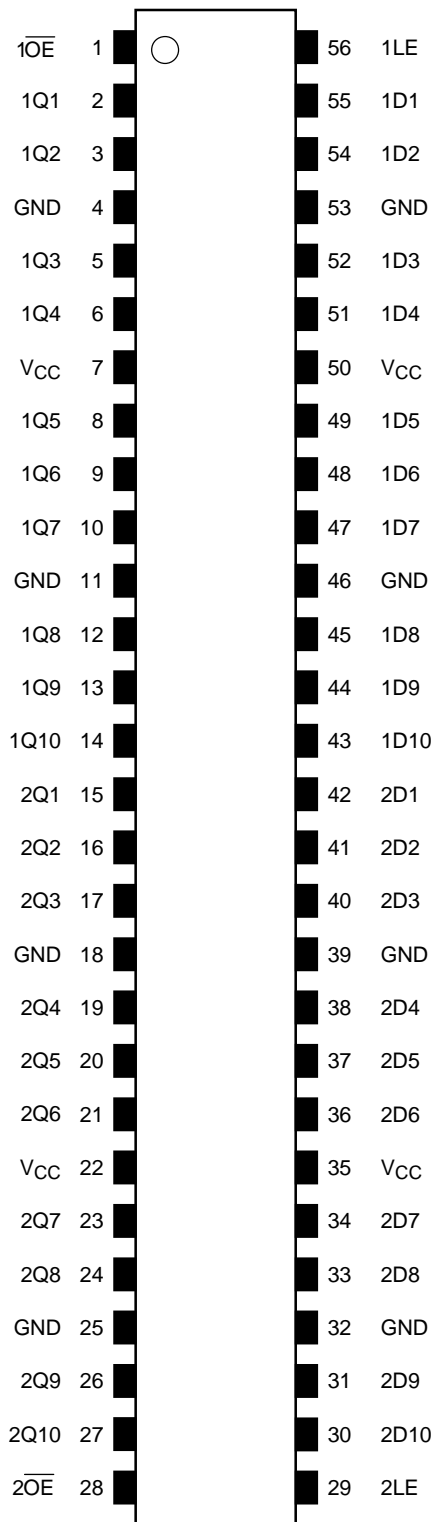


Weight: 0.25g (typ.)

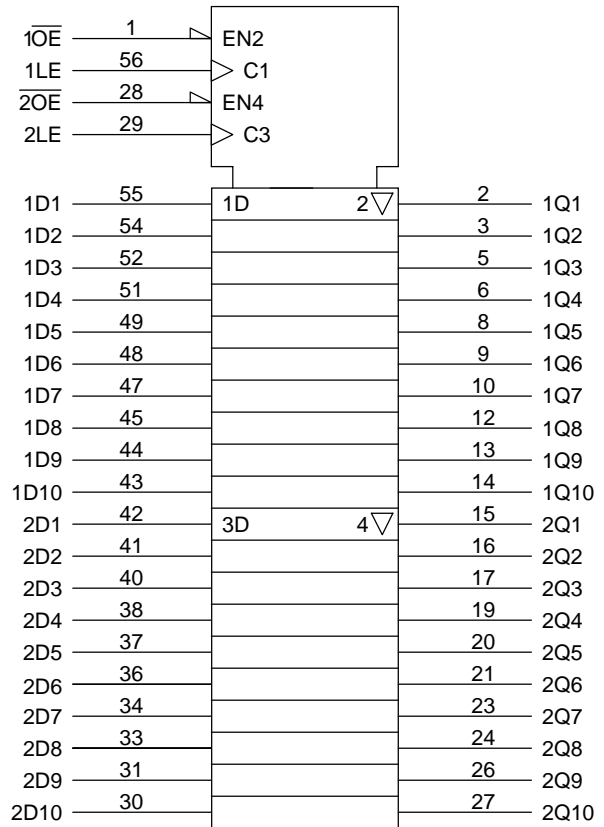
### Features

- 26- $\Omega$  series resistors on outputs
- Low-voltage operation:  $V_{CC} = 1.8$  to 3.6 V
- High-speed operation:  $t_{pd} = 3.9$  ns (max) ( $V_{CC} = 3.0$  to 3.6 V)  
:  $t_{pd} = 4.8$  ns (max) ( $V_{CC} = 2.3$  to 2.7 V)  
:  $t_{pd} = 9.6$  ns (max) ( $V_{CC} = 1.8$  V)
- Output current:  $I_{OH}/I_{OL} = \pm 12$  mA (min) ( $V_{CC} = 3.0$  V)  
:  $I_{OH}/I_{OL} = \pm 8$  mA (min) ( $V_{CC} = 2.3$  V)  
:  $I_{OH}/I_{OL} = \pm 4$  mA (min) ( $V_{CC} = 1.8$  V)
- Latch-up performance:  $\pm 300$  mA
- ESD performance: Machine model  $> \pm 200$  V  
: Human body model  $> \pm 2000$  V
- Package: TSSOP (thin shrink small outline package)
- 3.6-V tolerant function and power-down protection provided on all inputs and outputs

## Pin Assignment (top view)



## IEC Logic Symbol



## Truth Table (each 10-bit latch)

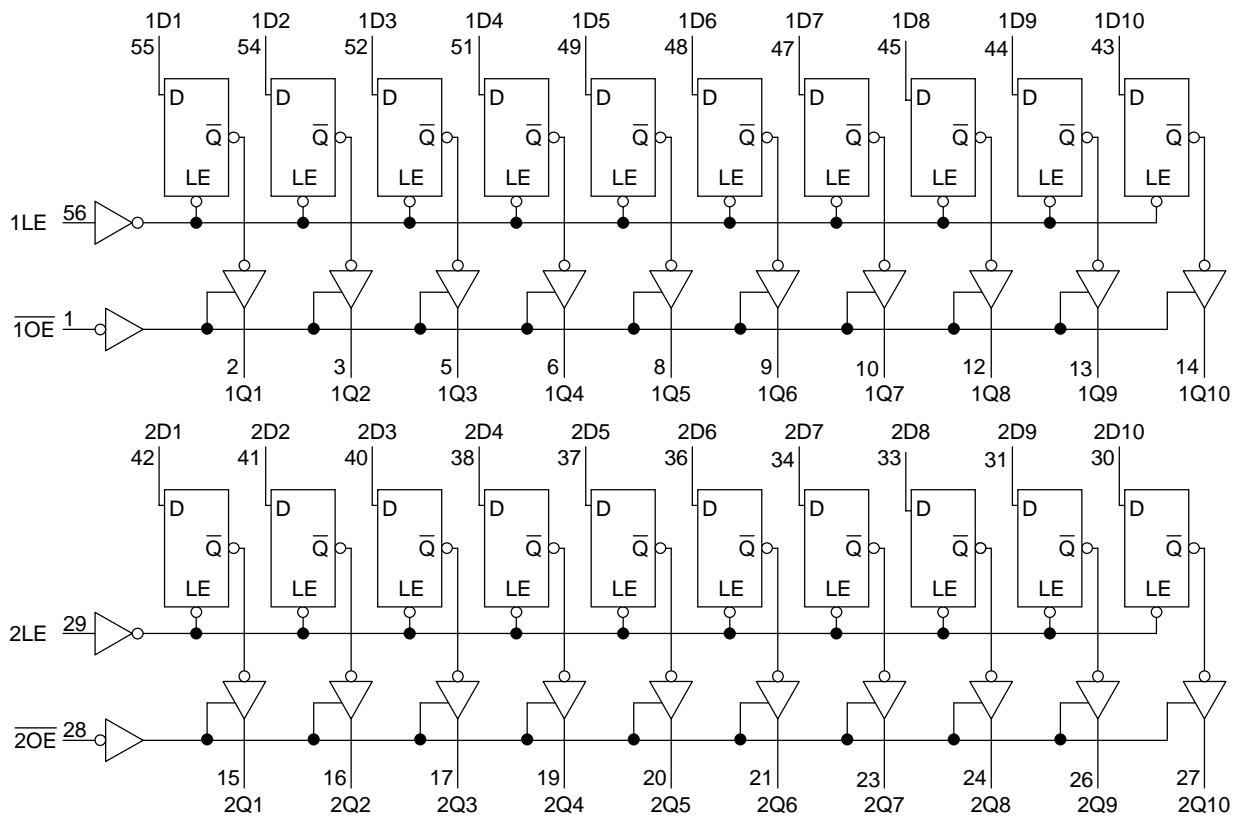
Input			Output Q
$\overline{OE}$	LE	D	
L	H	H	H
L	H	L	L
L	L	X	Qn
H	X	X	Z

X: Don't care

Z: High impedance

Qn: Q outputs are latched at the time when the LE input is taken to a low logic level.

## System Diagram



## Maximum Ratings

Characteristics	Symbol	Rating	Unit
Power supply voltage	$V_{CC}$	-0.5 to 4.6	V
DC input voltage	$V_{IN}$	-0.5 to 4.6	V
DC output voltage	$V_{OUT}$	-0.5 to 4.6 (Note 1)	V
		-0.5 to $V_{CC} + 0.5$ (Note 2)	
Input diode current	$I_{IK}$	-50	mA
Output diode current	$I_{OK}$	$\pm 50$ (Note 3)	mA
DC output current	$I_{OUT}$	$\pm 50$	mA
Power dissipation	$P_D$	400	mW
DC $V_{CC}$ /ground current per supply pin	$I_{CC}/I_{GND}$	$\pm 100$	mA
Storage temperature	$T_{stg}$	-65 to 150	$^{\circ}C$

Note 1: OFF state

Note 2: High or low state.  $I_{OUT}$  absolute maximum rating must be observed.

Note 3:  $V_{OUT} < GND$ ,  $V_{OUT} > V_{CC}$

## Recommended Operating Range

Characteristics	Symbol	Rating	Unit
Power supply voltage	$V_{CC}$	1.8 to 3.6	V
		1.2 to 3.6 (Note 4)	
Input voltage	$V_{IN}$	-0.3 to 3.6	V
Output voltage	$V_{OUT}$	0 to 3.6 (Note 5)	V
		0 to $V_{CC}$ (Note 6)	
Output current	$I_{OH}/I_{OL}$	$\pm 12$ (Note 7)	mA
		$\pm 8$ (Note 8)	
		$\pm 4$ (Note 9)	
Operating temperature	$T_{opr}$	-40 to 85	$^{\circ}C$
Input rise and fall time	$dt/dv$	0 to 10 (Note 10)	ns/V

Note 4: Data retention only

Note 5: OFF state

Note 6: High or low state

Note 7:  $V_{CC} = 3.0$  to  $3.6$  V

Note 8:  $V_{CC} = 2.3$  to  $2.7$  V

Note 9:  $V_{CC} = 1.8$  V

Note 10:  $V_{IN} = 0.8$  to  $2.0$  V,  $V_{CC} = 3.0$  V

**Electrical Characteristics**

**DC Characteristics (Ta = -40 to 85°C, 2.7 V < VCC ≤ 3.6 V)**

Characteristics		Symbol	Test Condition		VCC (V)	Min	Max	Unit
Input voltage	H-level	V <sub>IH</sub>	—		2.7 to 3.6	2.0	—	V
	L-level	V <sub>IL</sub>	—		2.7 to 3.6	—	0.8	
Output voltage	H-level	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -100 μA	2.7 to 3.6	V <sub>CC</sub> - 0.2	—	V
				I <sub>OH</sub> = -6 mA	2.7	2.2	—	
				I <sub>OH</sub> = -8 mA	3.0	2.4	—	
				I <sub>OH</sub> = -12 mA	3.0	2.2	—	
	L-level	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 100 μA	2.7 to 3.6	—	0.2	
				I <sub>OL</sub> = 6 mA	2.7	—	0.4	
				I <sub>OL</sub> = 8 mA	3.0	—	0.55	
				I <sub>OL</sub> = 12 mA	3.0	—	0.8	
Input leakage current		I <sub>IN</sub>	V <sub>IN</sub> = 0 to 3.6 V		2.7 to 3.6	—	±5.0	μA
3-state output OFF state current		I <sub>OZ</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> = 0 to 3.6 V		2.7 to 3.6	—	±10.0	μA
Power-off leakage current		I <sub>OFF</sub>	V <sub>IN</sub> , V <sub>OUT</sub> = 0 to 3.6 V		0	—	10.0	μA
Quiescent supply current		I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		2.7 to 3.6	—	20.0	μA
			V <sub>CC</sub> ≤ (V <sub>IN</sub> , V <sub>OUT</sub> ) ≤ 3.6 V		2.7 to 3.6	—	±20.0	
Increase in I <sub>CC</sub> per input		ΔI <sub>CC</sub>	V <sub>IH</sub> = V <sub>CC</sub> - 0.6 V		2.7 to 3.6	—	750	

**DC Characteristics (Ta = -40 to 85°C, 2.3 V ≤ VCC ≤ 2.7 V)**

Characteristics		Symbol	Test Condition		VCC (V)	Min	Max	Unit
Input voltage	H-level	V <sub>IH</sub>	—		2.3 to 2.7	1.6	—	V
	L-level	V <sub>IL</sub>	—		2.3 to 2.7	—	0.7	
Output voltage	H-level	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -100 μA	2.3 to 2.7	V <sub>CC</sub> - 0.2	—	V
				I <sub>OH</sub> = -4 mA	2.3	2.0	—	
				I <sub>OH</sub> = -6 mA	2.3	1.8	—	
				I <sub>OH</sub> = -8 mA	2.3	1.7	—	
	L-level	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 100 μA	2.3 to 2.7	—	0.2	
				I <sub>OL</sub> = 6 mA	2.3	—	0.4	
				I <sub>OL</sub> = 8 mA	2.3	—	0.6	
Input leakage current		I <sub>IN</sub>	V <sub>IN</sub> = 0 to 3.6 V		2.3 to 2.7	—	±5.0	μA
3-state output OFF state current		I <sub>OZ</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> = 0 to 3.6 V		2.3 to 2.7	—	±10.0	μA
Power-off leakage current		I <sub>OFF</sub>	V <sub>IN</sub> , V <sub>OUT</sub> = 0 to 3.6 V		0	—	10.0	μA
Quiescent supply current		I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		2.3 to 2.7	—	20.0	μA
			V <sub>CC</sub> ≤ (V <sub>IN</sub> , V <sub>OUT</sub> ) ≤ 3.6 V		2.3 to 2.7	—	±20.0	

## DC Characteristics (Ta = -40 to 85°C, 1.8 V ≤ VCC < 2.3 V)

Characteristics		Symbol	Test Condition		VCC (V)	Min	Max	Unit
Input voltage	H-level	V <sub>IH</sub>	—		1.8 to 2.3	0.7 × V <sub>CC</sub>	—	V
	L-level	V <sub>IL</sub>	—		1.8 to 2.3	—	0.2 × V <sub>CC</sub>	
Output voltage	H-level	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -100 μA	1.8	V <sub>CC</sub> - 0.2	—	V
				I <sub>OH</sub> = -4 mA	1.8	1.4	—	
	L-level	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 100 μA	1.8	—	0.2	
				I <sub>OL</sub> = 4 mA	1.8	—	0.3	
Input leakage current		I <sub>IN</sub>	V <sub>IN</sub> = 0 to 3.6 V		1.8	—	±5.0	μA
3-state output OFF state current		I <sub>OZ</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> = 0 to 3.6 V		1.8	—	±10.0	μA
Power-off leakage current		I <sub>OFF</sub>	V <sub>IN</sub> , V <sub>OUT</sub> = 0 to 3.6 V		0	—	10.0	μA
Quiescent supply current		I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		1.8	—	20.0	μA
			V <sub>CC</sub> ≤ (V <sub>IN</sub> , V <sub>OUT</sub> ) ≤ 3.6 V		1.8	—	±20.0	

## AC Characteristics (Ta = -40 to 85°C, input: tr = tf = 2.0 ns, CL = 30 pF, RL = 500 Ω)

Characteristics	Symbol	Test Condition	VCC (V)	Min	Max	Unit
Propagation delay time (D-Q)	t <sub>pLH</sub> t <sub>pHL</sub>	Figure 1, Figure 2	1.8	1.5	9.6	ns
			2.5 ± 0.2	0.8	4.8	
			3.3 ± 0.3	0.6	3.9	
Propagation delay time (LE-Q)	t <sub>pLH</sub> t <sub>pHL</sub>	Figure 1, Figure 2	1.8	1.5	9.8	ns
			2.5 ± 0.2	0.8	5.8	
			3.3 ± 0.3	0.6	4.4	
3-state output enable time	t <sub>pZL</sub> t <sub>pZH</sub>	Figure 1, Figure 3	1.8	1.5	9.8	ns
			2.5 ± 0.2	0.8	5.9	
			3.3 ± 0.3	0.6	4.3	
3-state output disable time	t <sub>pLZ</sub> t <sub>pHZ</sub>	Figure 1, Figure 3	1.8	1.5	8.8	ns
			2.5 ± 0.2	0.8	4.9	
			3.3 ± 0.3	0.6	4.3	
Minimum pulse width (LE)	t <sub>w</sub> (H)	Figure 1, Figure 2	1.8	4.0	—	ns
			2.5 ± 0.2	1.5	—	
			3.3 ± 0.3	1.5	—	
Minimum setup time	t <sub>s</sub>	Figure 1, Figure 2	1.8	2.5	—	ns
			2.5 ± 0.2	1.5	—	
			3.3 ± 0.3	1.5	—	
Minimum hold time	t <sub>h</sub>	Figure 1, Figure 2	1.8	1.0	—	ns
			2.5 ± 0.2	1.0	—	
			3.3 ± 0.3	1.0	—	
Output to output skew	t <sub>osLH</sub> t <sub>osHL</sub>	(Note 11)	1.8	—	0.5	ns
			2.5 ± 0.2	—	0.5	
			3.3 ± 0.3	—	0.5	

For C<sub>L</sub> = 50 pF, add approximately 300 ps to the AC maximum specification.

Note 11: Parameter guaranteed by design.

$$(t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|)$$

**Dynamic Switching Characteristics**

(Ta = 25°C, input: tr = tf = 2.0 ns, CL = 30 pF, RL = 500 Ω)

Characteristics	Symbol	Test Condition		Typ.	Unit	
			VCC (V)			
Quiet output maximum dynamic VOL	VOLP	VIH = 1.8 V, VIL = 0 V	(Note 12)	1.8	0.15	V
		VIH = 2.5 V, VIL = 0 V	(Note 12)	2.5	0.25	
		VIH = 3.3 V, VIL = 0 V	(Note 12)	3.3	0.35	
Quiet output minimum dynamic VOL	VOLV	VIH = 1.8 V, VIL = 0 V	(Note 12)	1.8	-0.15	V
		VIH = 2.5 V, VIL = 0 V	(Note 12)	2.5	-0.25	
		VIH = 3.3 V, VIL = 0 V	(Note 12)	3.3	-0.35	
Quiet output minimum dynamic VOH	VOHV	VIH = 1.8 V, VIL = 0 V	(Note 12)	1.8	1.55	V
		VIH = 2.5 V, VIL = 0 V	(Note 12)	2.5	2.05	
		VIH = 3.3 V, VIL = 0 V	(Note 12)	3.3	2.65	

Note 12: Parameter guaranteed by design.

**Capacitive Characteristics (Ta = 25°C)**

Characteristics	Symbol	Test Condition		Typ.	Unit	
			VCC (V)			
Input capacitance	CIN	—		1.8, 2.5, 3.3	6	pF
Output capacitance	CO	—		1.8, 2.5, 3.3	7	pF
Power dissipation capacitance	CPD	fIN = 10 MHz	(Note 13)	1.8, 2.5, 3.3	20	pF

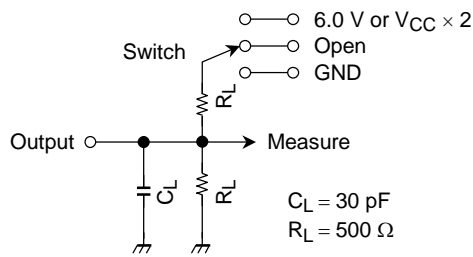
Note 13: CPD is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/20 \text{ (per bit)}$$



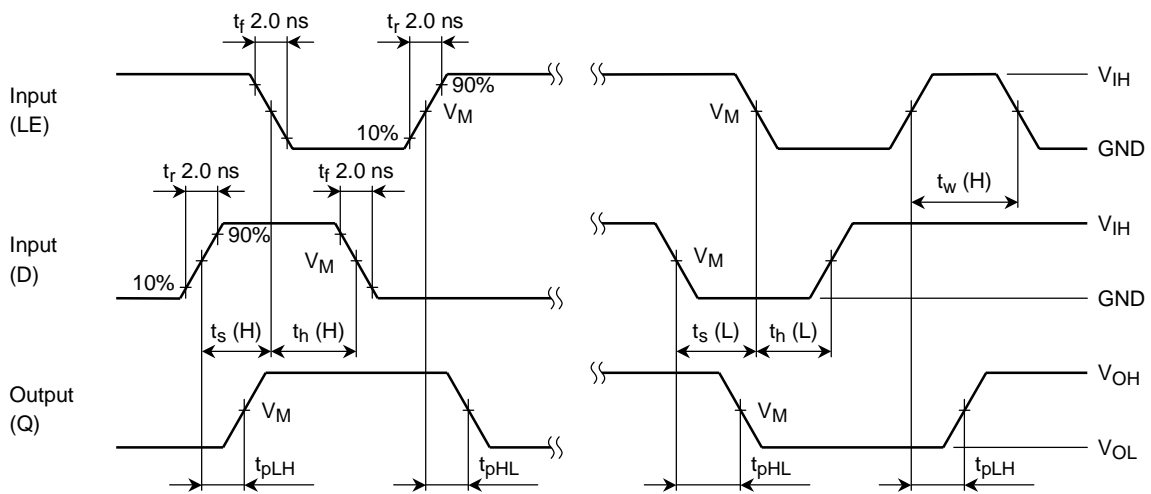
**AC Test Circuit**



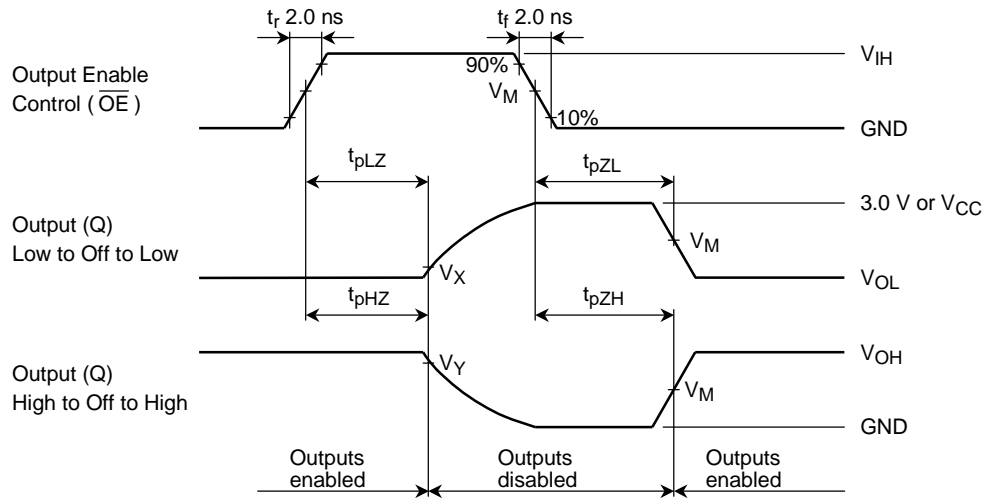
Parameter	Switch
$t_{pLH}, t_{pHL}$	Open
$t_{pLZ}, t_{pZL}$	6.0 V @ $V_{CC} = 3.3 \pm 0.3 \text{ V}$ $V_{CC} \times 2$ @ $V_{CC} = 2.5 \pm 0.2 \text{ V}$ @ $V_{CC} = 1.8 \text{ V}$
$t_{pHZ}, t_{pZH}$	GND

**Figure 1**  $t_{pLH}, t_{pHL}, t_w, t_s, t_h$

**AC Waveform**



**Figure 2**  $t_{pLH}, t_{pHL}, t_w, t_s, t_h$



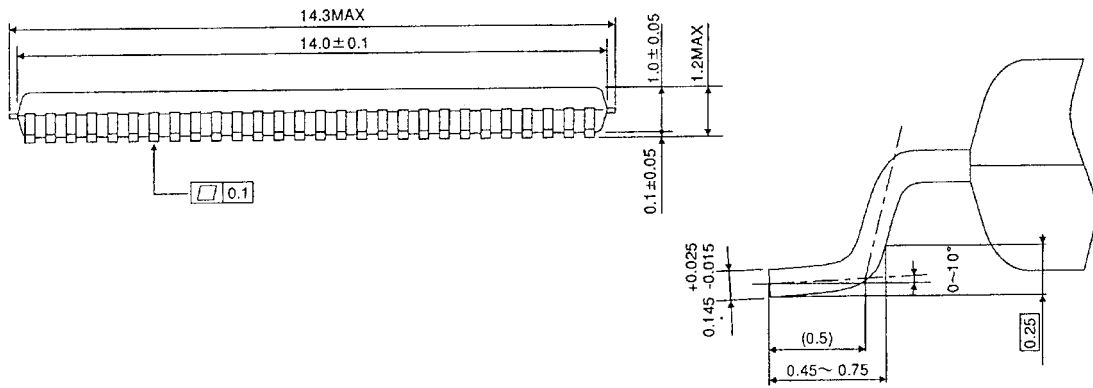
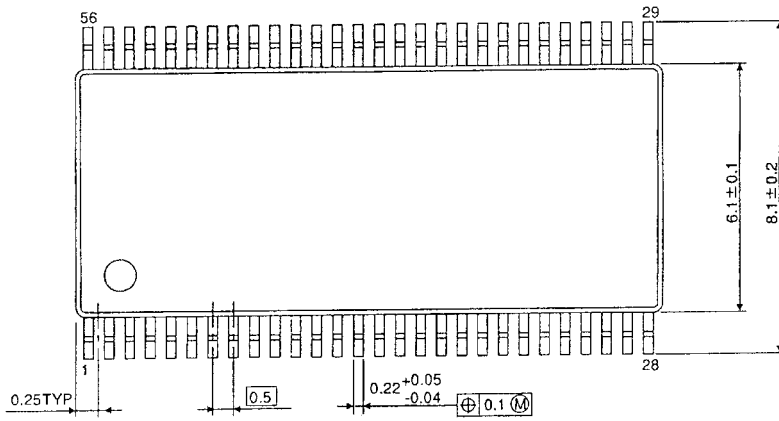
**Figure 3**  $t_{pLZ}$ ,  $t_{pHZ}$ ,  $t_{pZL}$ ,  $t_{pZH}$

Symbol	$V_{CC}$		
	$3.3 \pm 0.3 \text{ V}$	$2.5 \pm 0.2 \text{ V}$	1.8 V
$V_{IH}$	2.7 V	$V_{CC}$	$V_{CC}$
$V_M$	1.5 V	$V_{CC}/2$	$V_{CC}/2$
$V_X$	$V_{OL} + 0.3 \text{ V}$	$V_{OL} + 0.15 \text{ V}$	$V_{OL} + 0.15 \text{ V}$
$V_Y$	$V_{OH} - 0.3 \text{ V}$	$V_{OH} - 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$

**Package Dimensions**

TSSOP56-P-0061-0.50

Unit : mm



Weight: 0.25 g (typ.)

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000707EBA

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