FOUR-, SIX-, AND EIGHT-CHANNEL EMI FILTERS WITH INTEGRATED ESD PROTECTION

Check for Samples: TPD4F003, TPD6F003, TPD8F003

FEATURES

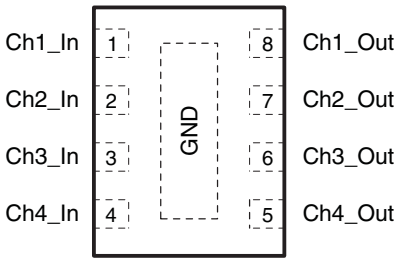
- **Four-, Six-, and Eight-Channel EMI Filtering for Data Ports**
- **–3 dB Bandwidth 200 MHz**
- **Greater than 25dB attenuation at 1 GHz**
- **Robust ESD Protection Exceeds IEC61000-4-2 (Level 4)**
  - **±15-kV Human-Body Model (HBM)**
  - **±12-kV IEC 61000-4-2 Contact Discharge**
  - **±20-kV IEC 61000-4-2 Air-Gap Discharge**
- **Pi-Style (C-R-C) Filter Configuration (R = 100 Ω, C_{TOTAL} = 17 pF)**
- **Low 10-nA Leakage Current**
- **Space-Saving DQD Packages and Flow-Through Pin Mapping Provide Optimum Filter Performance**

APPLICATIONS

- **LCD Display Interfaces**
- **Cell Phones**
- **SVGA Video Connections**
- **Personal Digital Assistants (PDAs)**

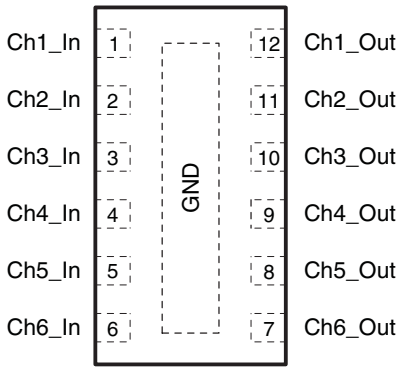
DQD PACKAGE
(TOP VIEW)

TPD4F003



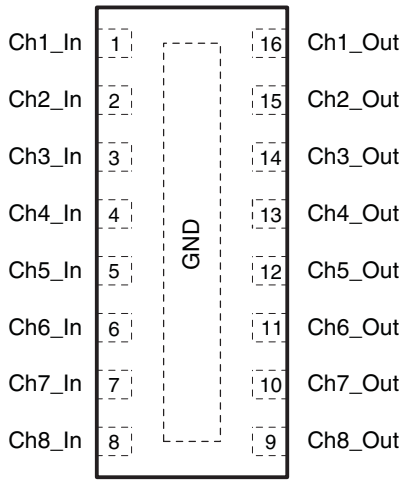
1.7 mm x 1.35 mm x 0.75 mm
(0.4-mm pitch)

TPD6F003



2.5 mm x 1.35 mm x 0.75 mm
(0.4-mm pitch)

TPD8F003



3.3 mm x 1.35 mm x 0.75 mm
(0.4-mm pitch)

DESCRIPTION/ORDERING INFORMATION

The TPD4F003, TPD6F003, and TPD8F003 are 4-, 6-, and 8-channel EMI filters in space-saving 0.4-mm pitch DQD packages. The low-pass filter arrays reduce EMI emissions and provide system level ESD protection.

Because of its small package and easy-to-use pin assignments, the TPDxF003 filters ar suitable for a wide array of applications such as mobile handsets, PDAs, video consoles, notebook computers, etc. In particular, these filters are ideal for EMI filtering and protecting data lines from ESD at the LCD display, keypad, and memory interfaces.

The TPDxF003 are highly integrated device designed to suppress EMI/RFI noise in all systems subjected to electromagnetic interferences. These filter series include an ESD protection circuitry which prevents damage to the application when subjected to ESD stress far exceeding IEC 61000-4-2 (Level 4).

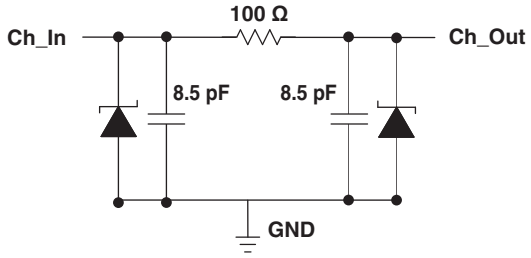
The TPDxF003 is specified for –40°C to 85°C operation.

ORDERING INFORMATION

T_A	PACKAGE(1) (2)	PACKAGE DIMENSION	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	0.4-mm pitch SON	Length = 1.7 mm, Width = 1.35 mm, Pitch = 0.4 mm, Height = 0.75 mm	TPD4F003DQDR	5RS
		Length = 2.5 mm, Width = 1.35 mm, Pitch = 0.4 mm, Height = 0.75 mm	TPD6F003DQDR	47S
		Length = 3.3 mm, Width = 1.35 mm, Pitch = 0.4 mm, Height = 0.75 mm	TPD8F003DQDR	5US

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

EQUIVALENT SCHEMATIC REPRESENTATION



ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IO}	IO to GND		6	V
T_{stg}	Storage temperature range	–65	150	°C
T_J	Junction temperature		150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{BR}	DC breakdown voltage	I_{IO} = 10 μA	6			V
R	Resistance		85	100	115	Ω
C	Capacitance (C1 or C2)	V_{IO} = 2.5 V		8.5		pF
I_{IO}	Channel leakage current	V_{IO} = 3.3 V		10		nA
f_C	Cut-off frequency	Z_{SOURCE} = 50 Ω, Z_{LOAD} = 50 Ω		200		MHz

(1) Typical values are at T_A = 25°C.

ESD PROTECTION

	TYP	UNIT
Human-Body Model (HBM)	±15	kV
IEC 61000-4-2 Contact Discharge	±12	kV
IEC 61000-4-2 Air-Gap Discharge	±20	kV

TYPICAL CHARACTERISTCS

IEC Clamping Waveforms (clamp voltage measured both at Ch_Out and Ch_In)

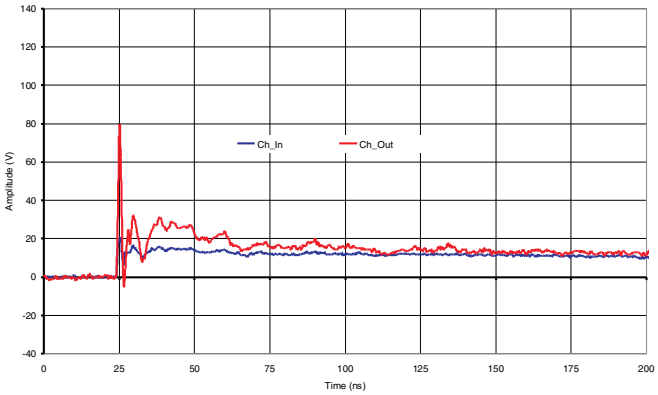


Figure 1. With 8 kV Contact ESD Stress at Ch_Out

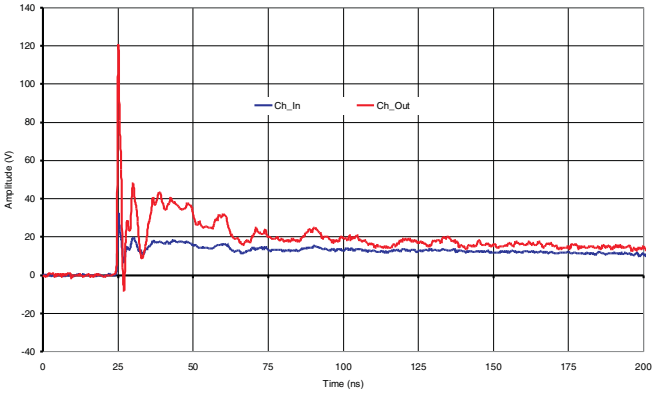


Figure 2. With 12 kV Contact ESD Stress at Ch_Out

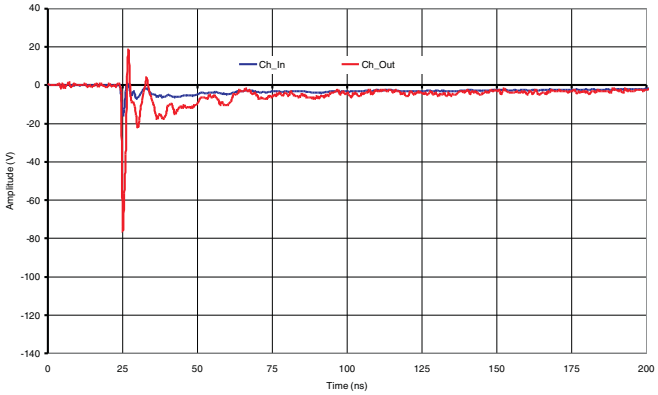


Figure 3. With -8 kV Contact ESD Stress at Ch_Out

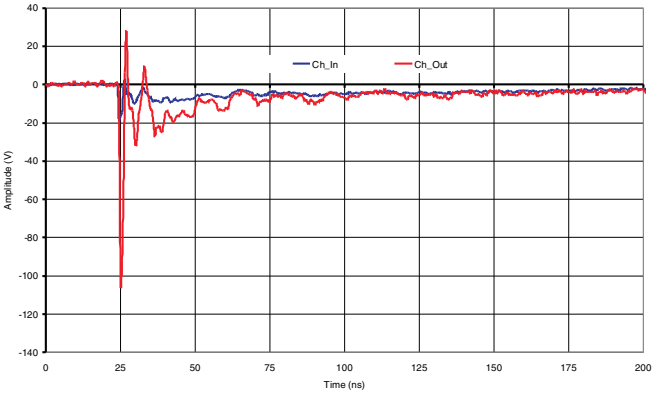


Figure 4. With -12 kV Contact ESD Stress at Ch_Out

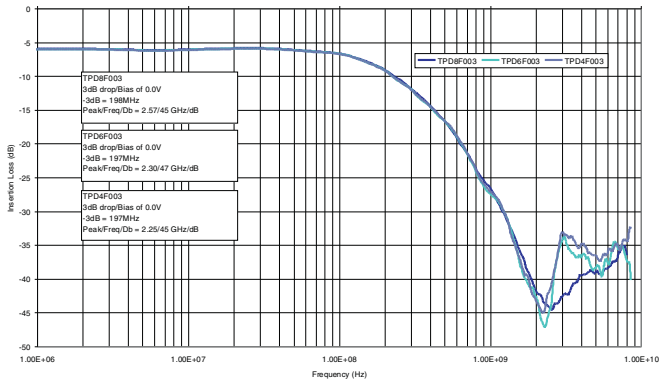


Figure 5. Frequency Response

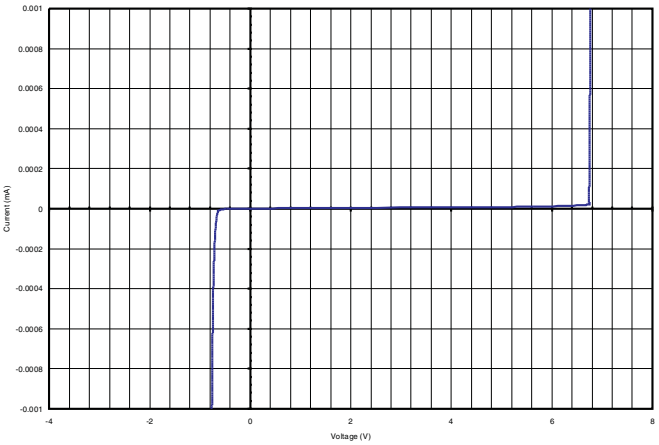


Figure 6. DC Voltage-Current Sweep Across Input/Output Pins

Channel-to-Channel Crosstalk

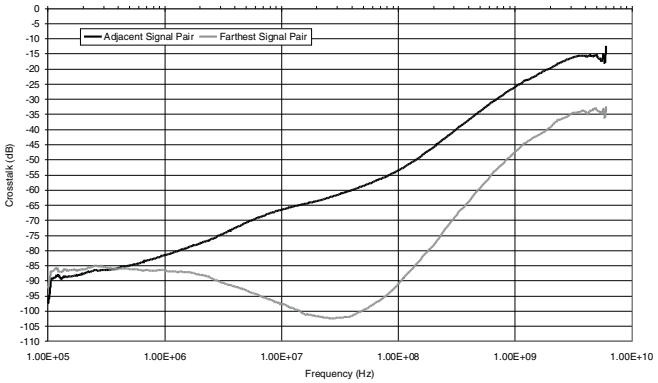


Figure 7. TPD4F003

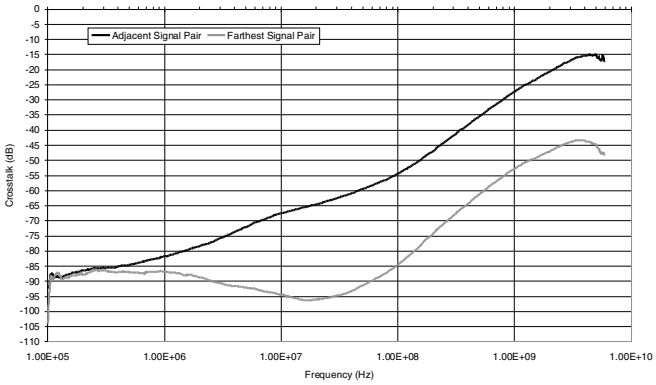


Figure 8. TPD6F003

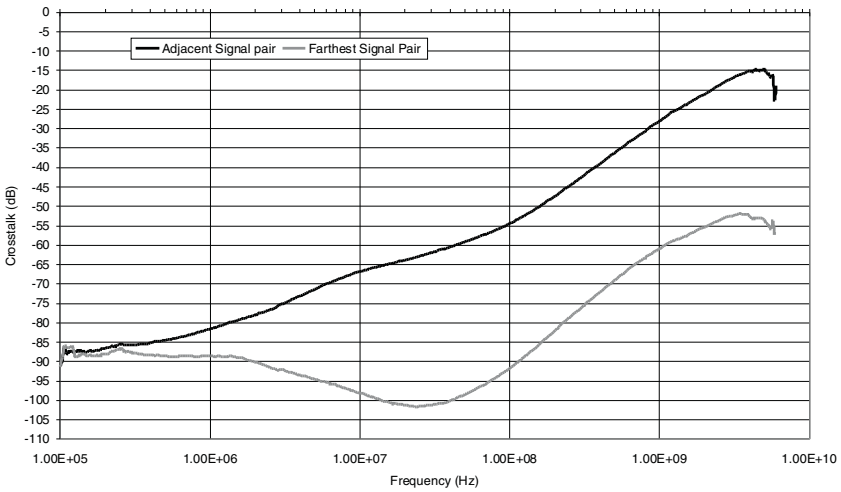


Figure 9. TPD8F003

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPD4F003DQDR	ACTIVE	WSON	DQD	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	5RS	Samples
TPD6F003DQDR	ACTIVE	WSON	DQD	12	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	47S	Samples
TPD8F003DQDR	ACTIVE	WSON	DQD	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	5US	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

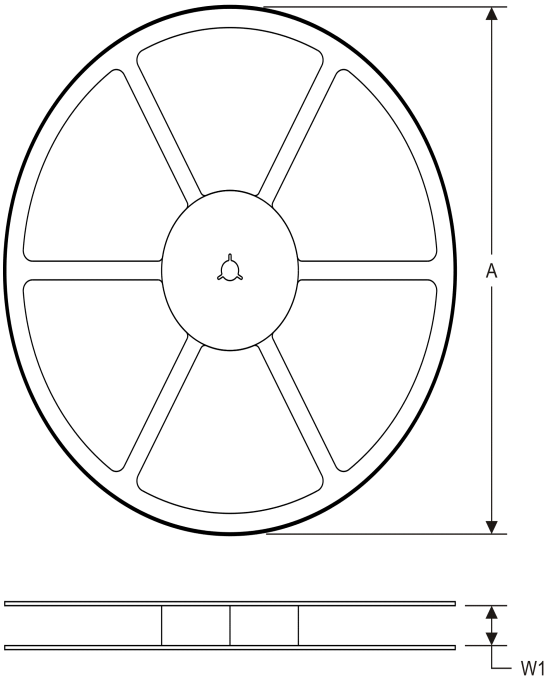
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

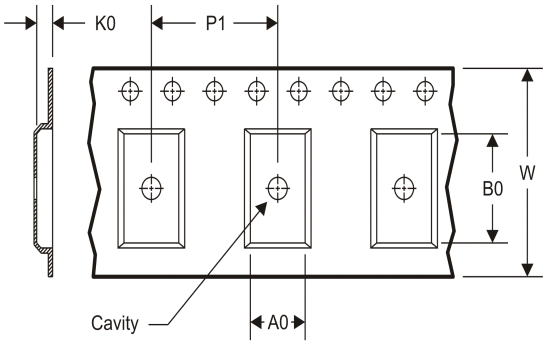
(4) Only one of markings shown within the brackets will appear on the physical device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



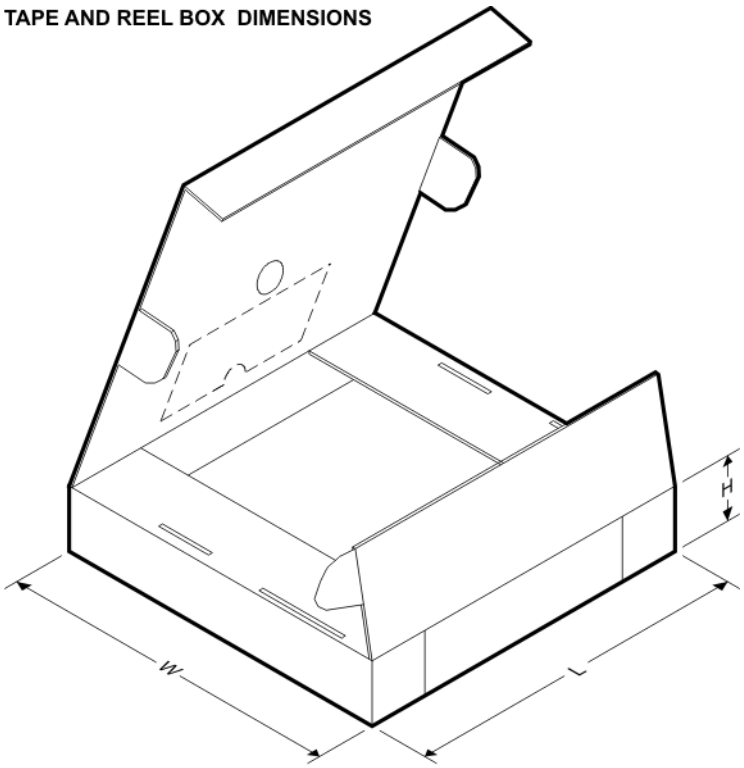
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD4F003DQDR	WSON	DQD	8	3000	180.0	8.4	1.65	2.0	0.95	4.0	8.0	Q1
TPD6F003DQDR	WSON	DQD	12	3000	180.0	8.4	1.68	2.79	0.91	4.0	8.0	Q1
TPD8F003DQDR	WSON	DQD	16	3000	330.0	12.4	1.65	3.6	0.95	4.0	12.0	Q1

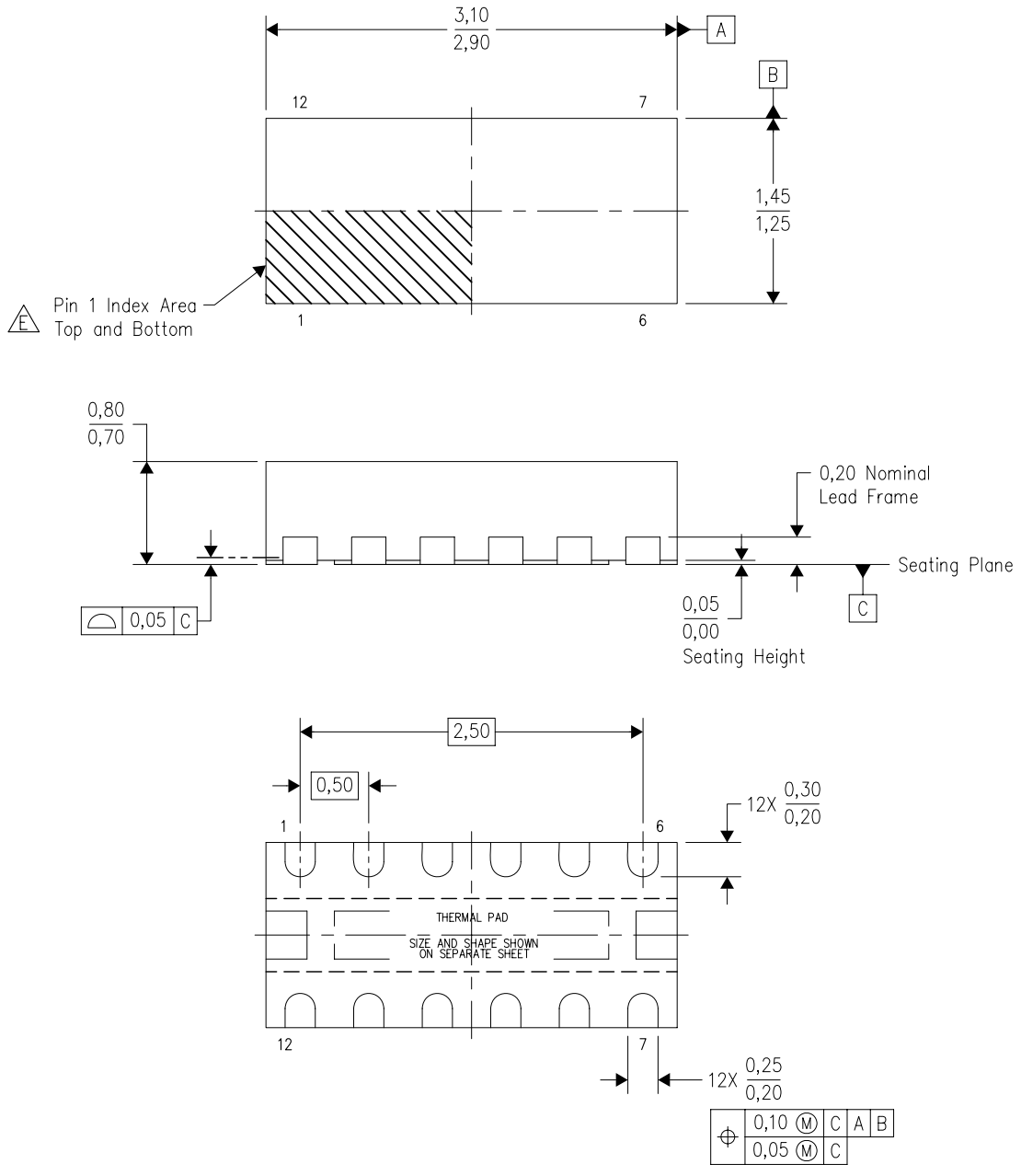
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

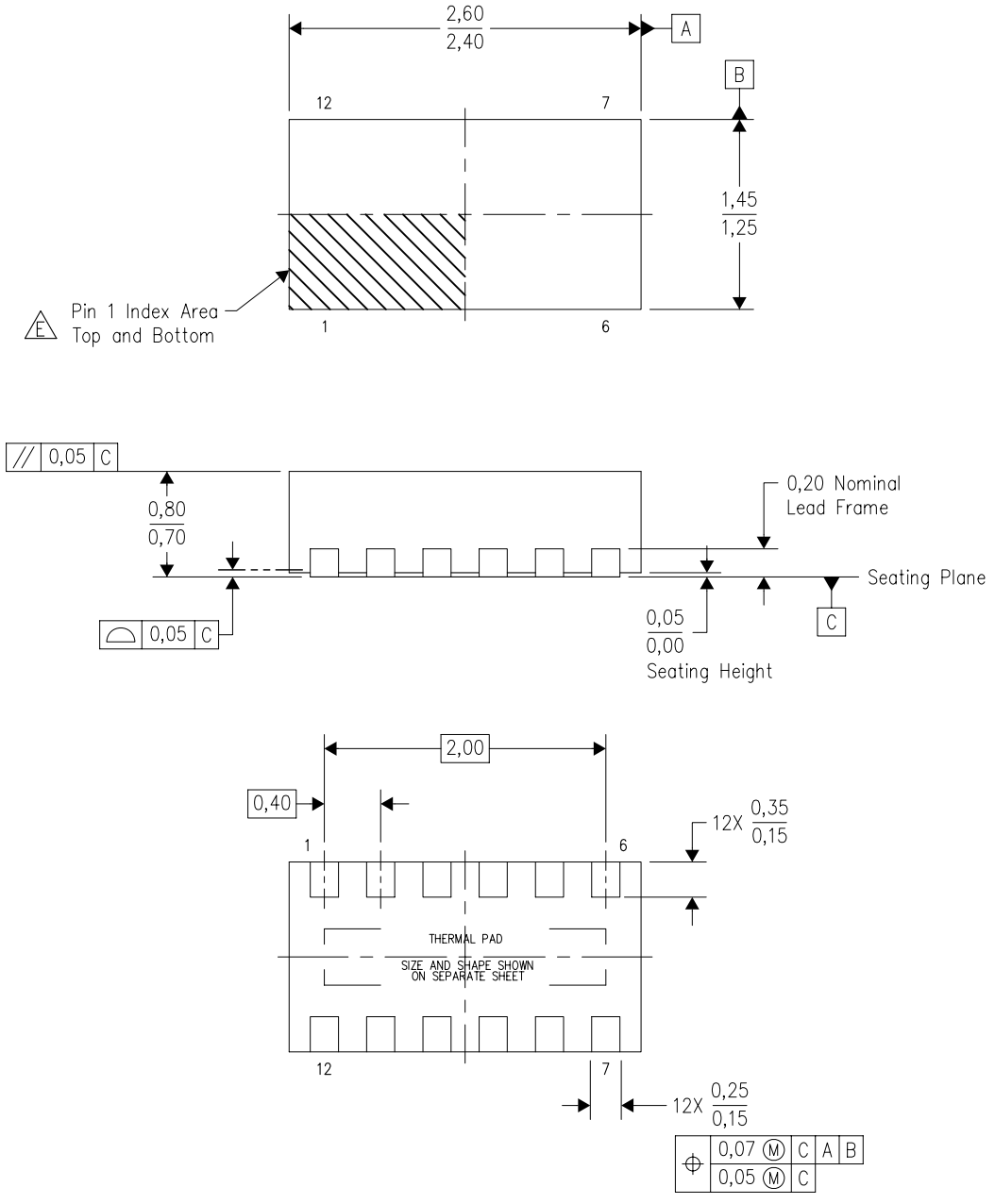
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD4F003DQDR	WSON	DQD	8	3000	202.0	201.0	28.0
TPD6F003DQDR	WSON	DQD	12	3000	202.0	201.0	28.0
TPD8F003DQDR	WSON	DQD	16	3000	358.0	335.0	35.0

DSV (R–PWSON–N12) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.

DQD (R–PWSON–N12) PLASTIC SMALL OUTLINE NO–LEAD



4209732–3/C 12/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.

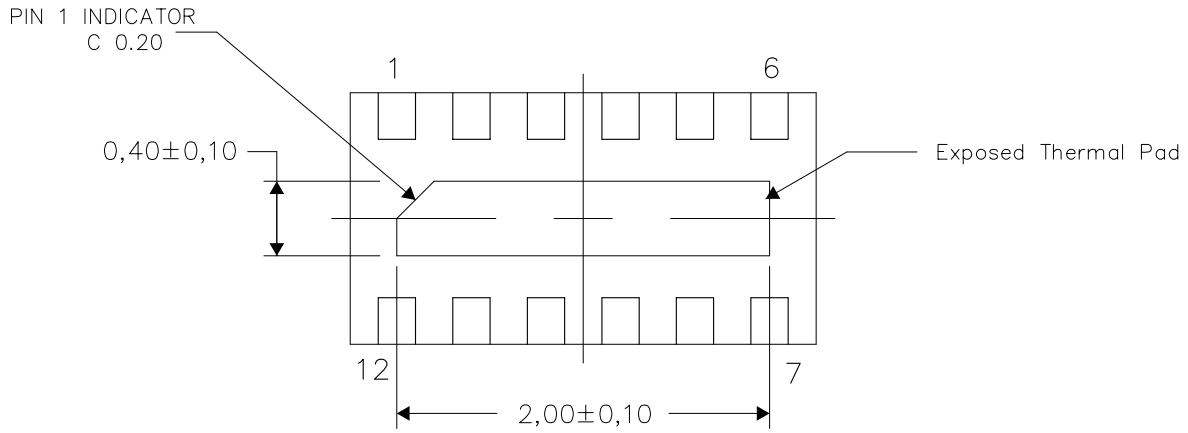
DQD (R–PWSON–N12) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



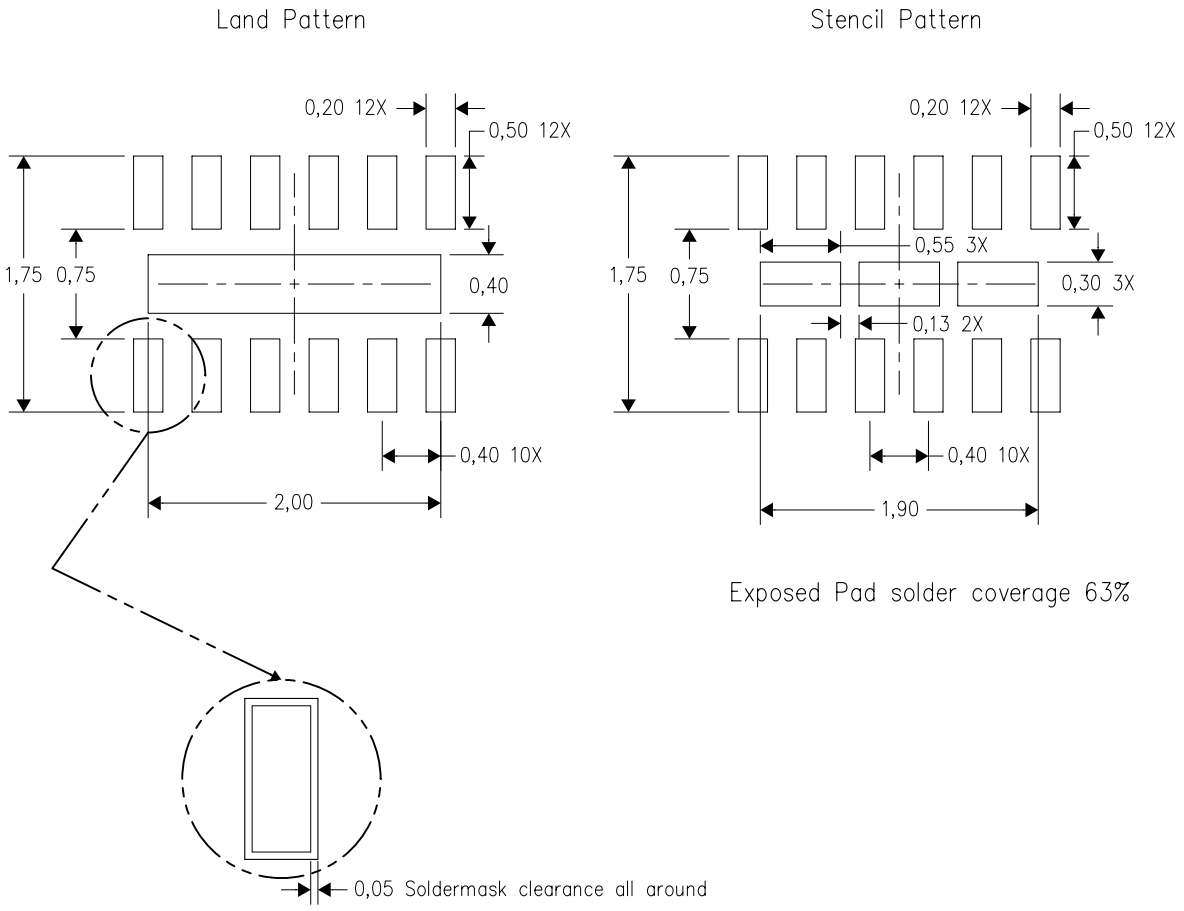
Bottom View

Exposed Thermal Pad Dimensions

4209733–3/C 12/11

NOTE: All linear dimensions are in millimeters

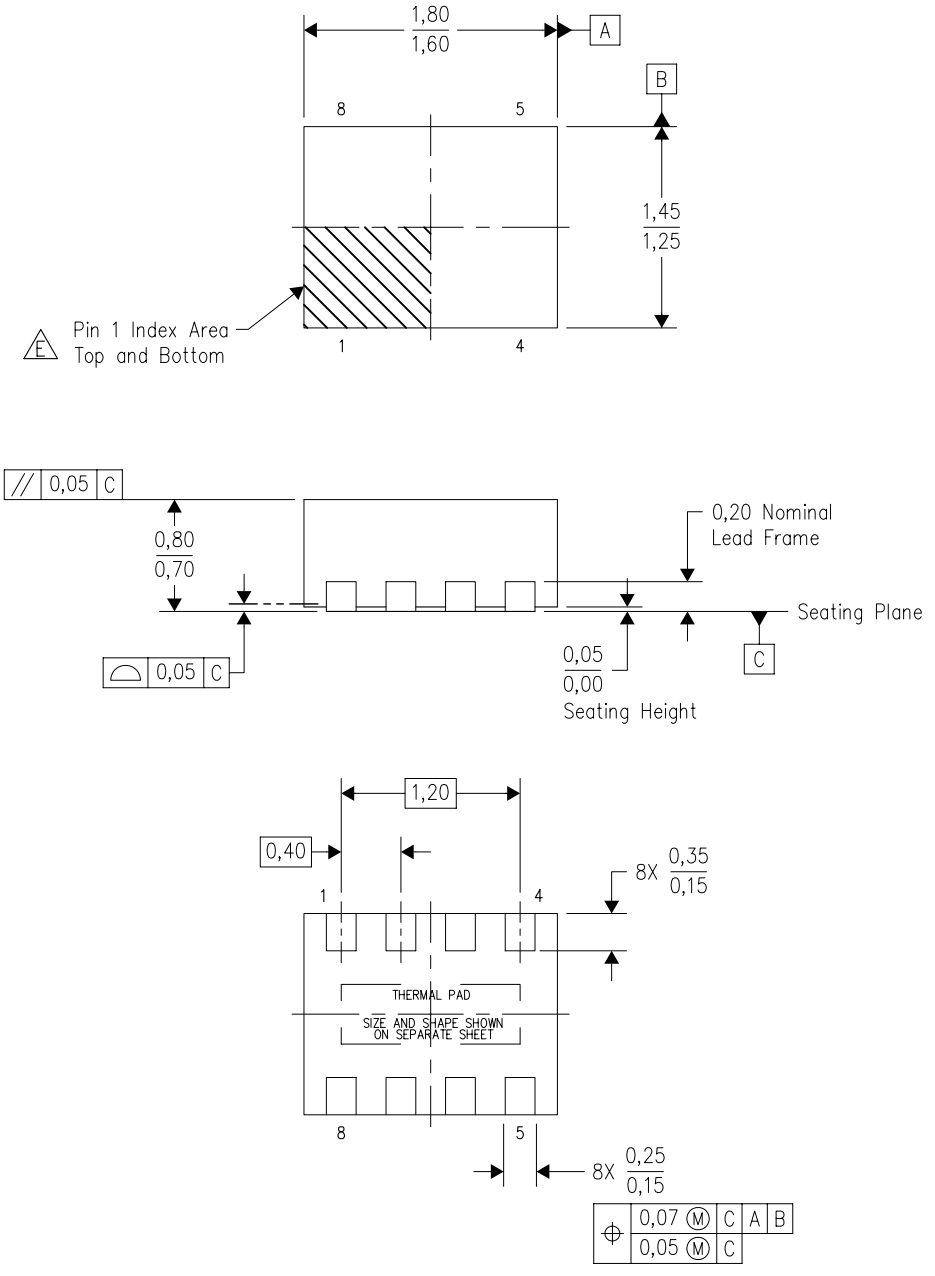
DQD (R–PWSON–N12) PLASTIC SMALL OUTLINE NO–LEAD



4211174–3/B 01/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

DQD (R–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



Bottom View

4209732–2/C 12/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.

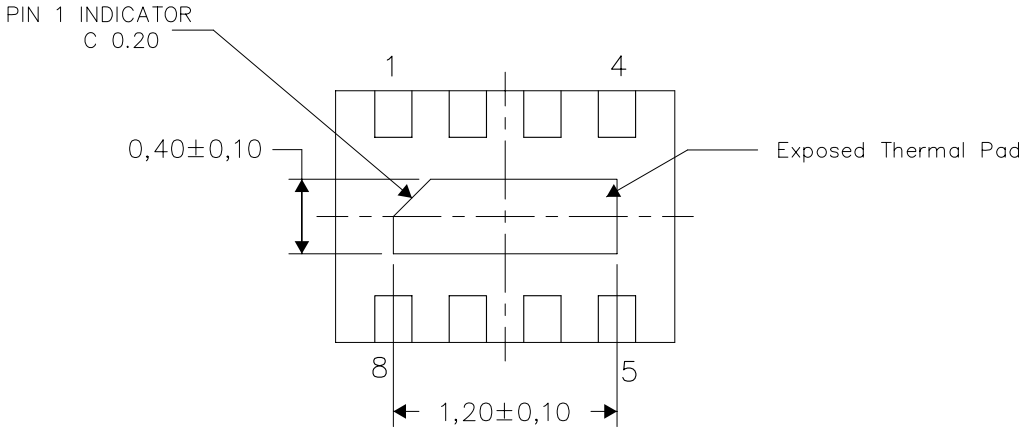
DQD (R–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

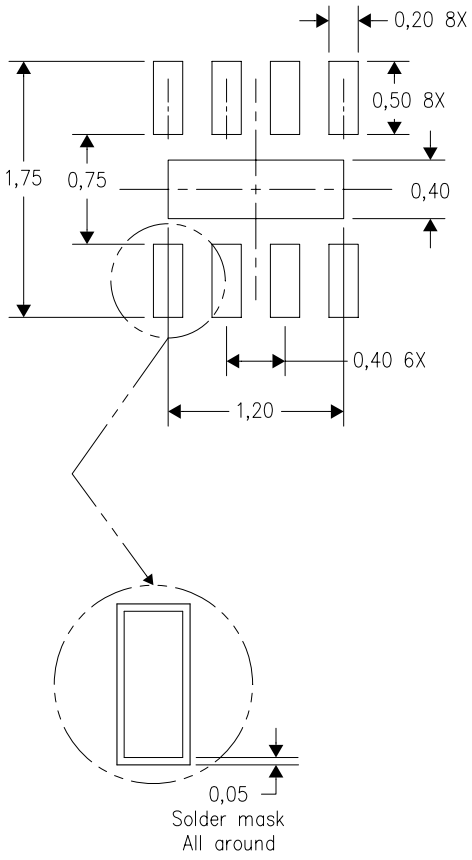
Exposed Thermal Pad Dimensions

4209733–2/C 12/11

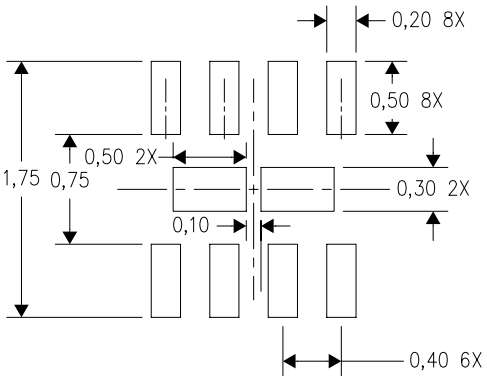
NOTE: All linear dimensions are in millimeters

DQD (R–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

Land Pattern



Stencil Pattern

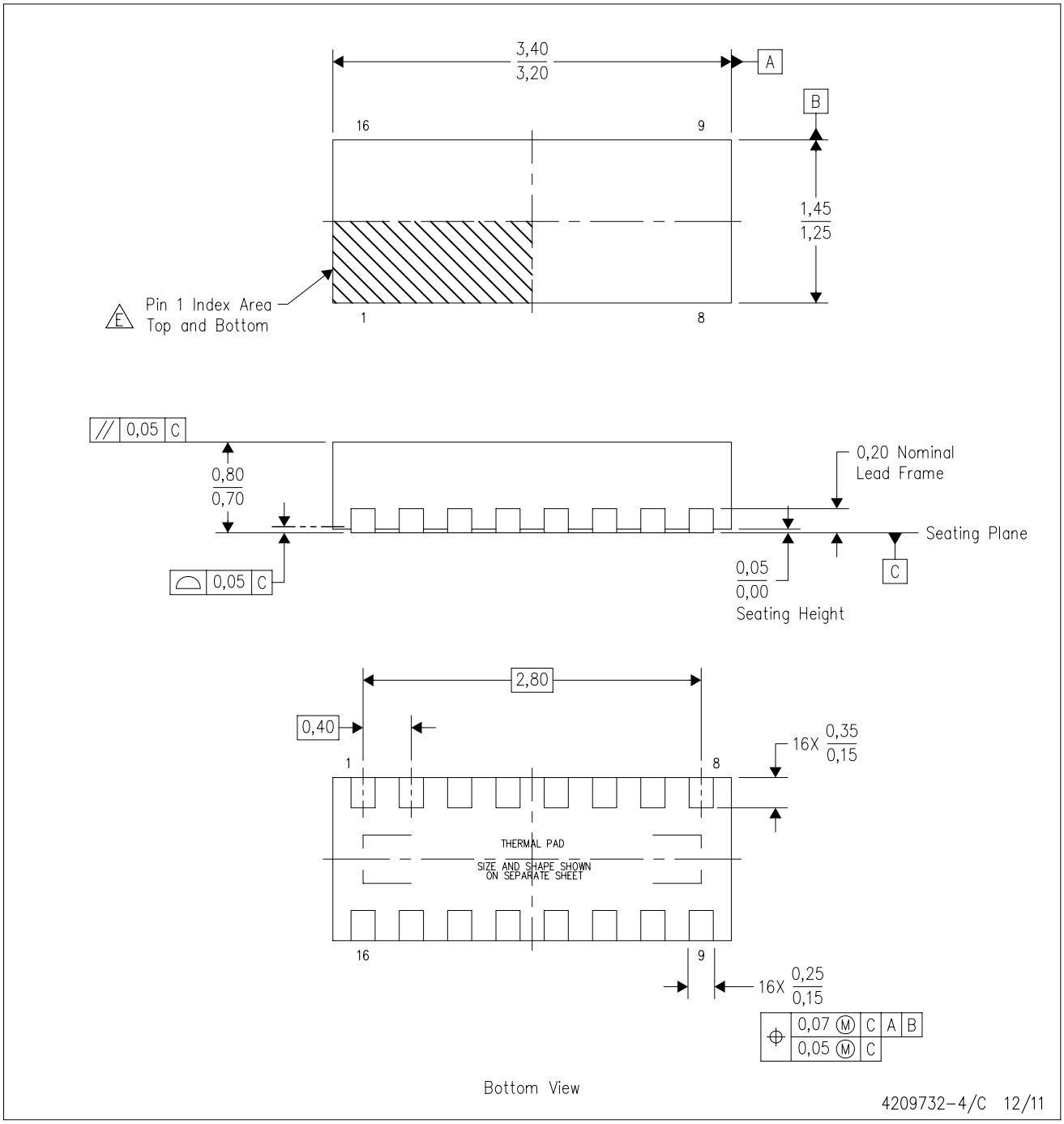


Exposed Pad solder coverage 62%

4211174–2/B 01/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

DQD (R–PWSON–N16) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.

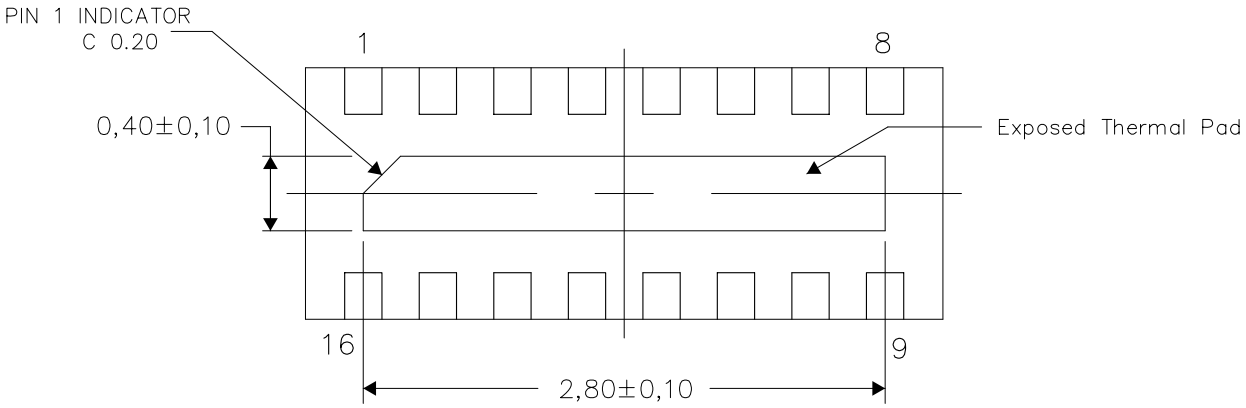
DQD (R–PWSON–N16) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



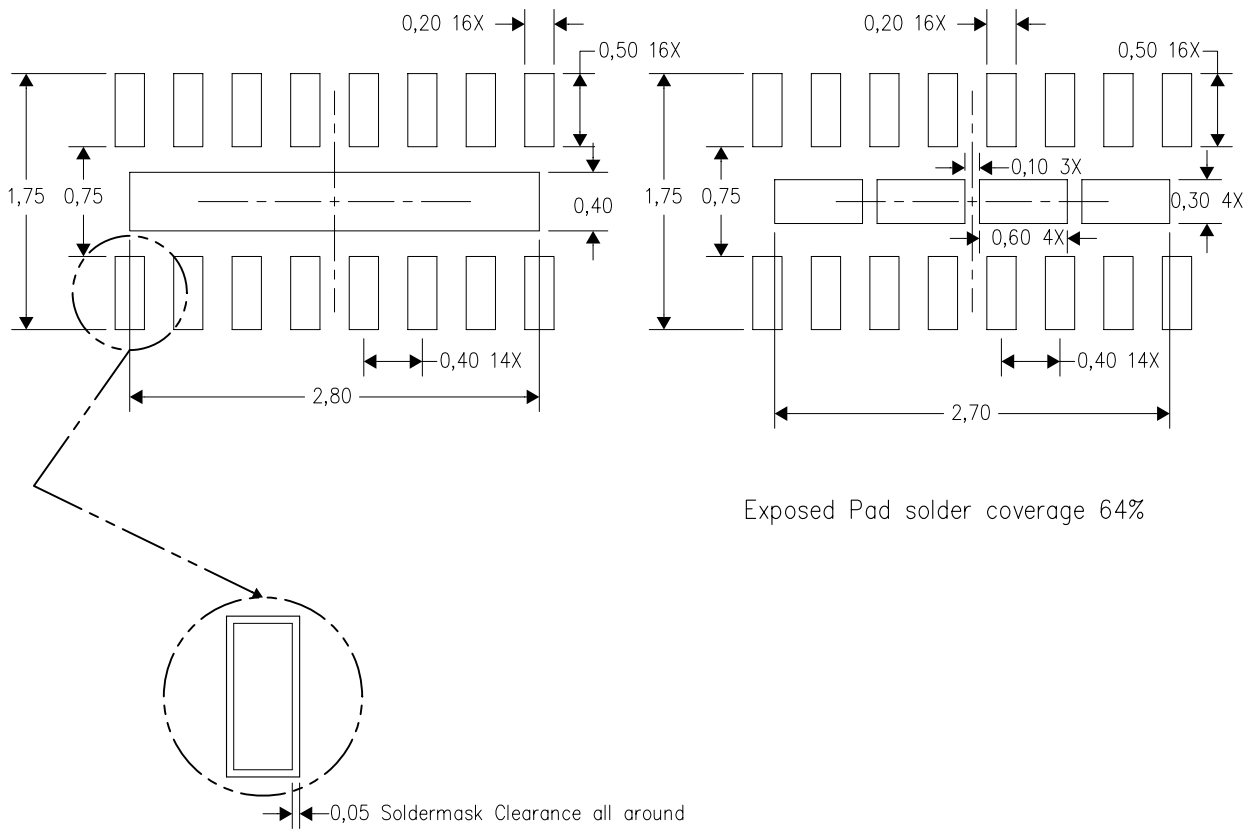
Bottom View

Exposed Thermal Pad Dimensions

4209733–4/C 12/11

NOTE: All linear dimensions are in millimeters

DQD (R–PWSON–N16) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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