PLL for DAB Tuner

Description

The U2753B-CFS is a monolithically integrated PLL circuit fabricated in TEMIC's advanced UHF5S technology. Designed for applications in DAB receivers it controls a VCO to synthesize frequencies in the range of 70 MHz to 500 MHz in a 16 kHz raster; four different reference divide factors can be selected. The lock status of the phase detector is indicated at a special output pin, six switching outputs can be addressed. An internal frequency doubler provides an output signal having twice the frequency of the reference oscillator. All functions of this IC are controlled by an I^2C bus.

Features

- Microprocessor controlled via I^2C bus
- 4 addresses selectable
- Four reference divider factors selectable: 1024, 1120, 1152, 1536
- Programmable 15-bit counter 1:2048 to 1:32767
- Three state phase detector with programmable charge pump
- Deactivation of tuning output programmable
- 6 switching outputs (open collector)
- Reference frequency doubler (open collector output)
- Lock status indication (open collector)

Package: SSO20

Block Diagram

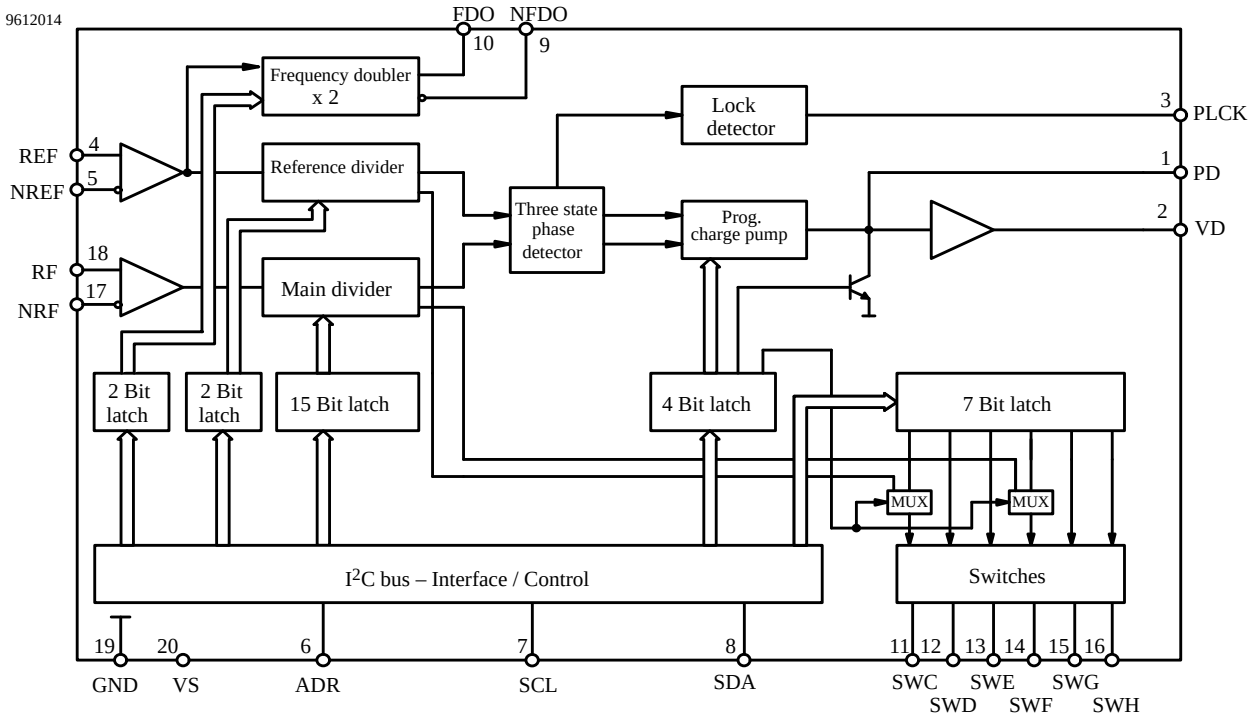


Figure 1.

Ordering and Package Information

Extended Type Number	Package	Remarks
U2753B-CFS	SSO20	
U2753B-CFSG3	SSO20	Taping according to ICE-286-3

Pin Description

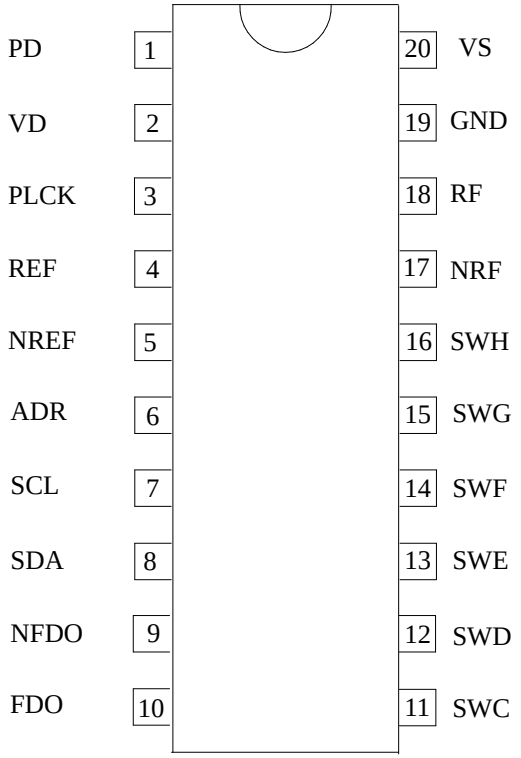


Figure 2. Pinning

Pin	Symbol	Function
1	PD	Three-state charge pump output
2	VD	Active filter output
3	PLCK	Lock indicating output (open collector)
4	REF	Reference input
5	NREF	Reference input (inverted)
6	ADR	Address selection
7	SCL	Clock (I^2C)
8	SDA	Data (I^2C)
9	NFDO	Frequency doubler output (inverted, open collector)
10	FDO	Frequency doubler output (open collector)
11	SWC	Switching output (open collector)
12	SWD	Switching output (open collector)
13	SWE	Switching output (open collector)
14	SWF	Switching output (open collector)
15	SWG	Switching output (open collector)
16	SWH	Switching output (open collector)
17	NRF	RF input (inverted)
18	RF	RF input
19	GND	Ground
20	VS	Supply voltage

Functional Description

The U2753B-C is a low power frequency synthesizer designed for applications in a DAB receiver. Its RF operation range reaches from 70 MHz up to 500 MHz. The device includes input buffers for reference and RF dividers, a reference divider, a programmable RF divider, a tri-state phase detector, a programmable charge pump, six switching outputs, a frequency doubler for the reference input signal and a control unit. The control unit has to be accessed by a micro controller via an I^2C bus. The programming information is stored in a set of internal registers. A block diagram of this circuit is shown in figure 1. Its pinning can be taken from figure 2. In figure 5 a typical application circuit is given.

Reference Divider

Four different scaling factors of the reference divider can be selected by means of the bits ‘RD1’ and ‘RD2’ in the I^2C bus instruction code: 1024, 1120, 1152 and 1536. Starting form a reference oscillator frequency of 16.38 MHz/ 17.92 MHz/ 18.432 MHz/ 24.576 MHz, these scaling factors provide a frequency raster of 16 Hz according to the DAB specification. By setting the I^2C bus bit ‘T’, a test signal representing the divided input signal can be monitored at the switching output SWC.

Main Divider

The 15-bit main divider is programmable via the I²C bus interface. Scaling factors from 2048 up to 32767 can be selected. By setting the I²C bus bit 'T', a test signal representing the divided input signal can be monitored at the switching output SWF.

When the supply voltage is switched on, both the reference divider and the programmable divider are kept in RESET state till a complete scaling factor is written onto the chip. Changes in the setting of the programmable divider become active when the corresponding I²C bus transmission has been completed. An internal synchronization procedure ensures that such changes do not become active while the charge pump is sourcing or sinking current at its output pin. This behavior allows a smooth tuning of the output frequency without disturbing the controlled VCO's frequency spectrum.

Phase Comparator and Charge Pump

The tristate phase detector causes the charge pump to source or to sink current at the output pin PD depending on the phase relation of its input signals which are provided by the reference and the main divider respectively. Four different values of this current can be selected by means of the I²C bus bits 'I50' and 'I100'. The charge pump current can be switched off using the I²C bus bit 'TRI'. A change in the setting of the charge pump current becomes active when the corresponding I²C bus transmission is completed. As described for the setting of the scaling factor of the programmable divider, an internal synchronization procedure ensures that such changes do not become active while the charge pump is sourcing or sinking current at its output pin. This behavior allows a change in the charge pump current without disturbing the controlled VCO's frequency spectrum.

A high gain amplifier (output pin: VD) which is implemented in order to construct a loop filter as shown in the application circuit can be switched off by means of the I²C bus bit 'OS'.

An internal lock detector checks if the phase difference of the input signals of the phase detector is smaller than approximately 250 ns in seven subsequent comparisons. If phase lock is detected, the open collector output pin PLCK is set 'H' (logical value). It should be noted that the output current of this pin must be limited by external circuitry as it is not limited internally. If the I²C bus bit 'TRI' is set 'H' the lock detector function is deactivated and the logical value of the PLCK output is undefined.

Switching Outputs

Six switching outputs controlled by the I²C bus bits 'SWC', 'SWD', 'SWE', 'SWF', 'SWG', 'SWH' can be used for any switching task on the fronted board. The currents of these outputs are not limited internally. They have to be limited by external circuitry.

Frequency Doubler

An internal frequency doubler provides a signal at twice the frequency of the reference signal appearing at the input pins REF and NREF. If the I²C bus bit 'OFD' = 'H' the current of its open collector outputs FDO and NFDO is doubled. The frequency doubler function can be switched off by means of the I²C bus bit 'OFD'.

The output signal of the frequency doubler is intended to be used in order to construct an LO signal for the IF circuit U2759B in a tuner module.

I²C Bus Interface / Control

Various functions can be controlled by a microprocessor-via its I²C bus interface These functions are described in the following section 'I²C bus instruction codes' and 'I²C bus functions'. By means of the ADR pin four different I²C bus addresses can be selected as described in the section 'Electrical characteristics'.

I²C Bus Instruction Codes

Description	MSB							LSB
Address byte	1	1	0	0	0	AS1	AS2	0
Divider byte 1	0	RD1	RD2	x	x	n_{14}	n_{13}	n_{12}
Divider byte 2	x	x	n_{11}	n_{10}	n_9	n_8	n_7	n_6
Divider byte 3	x	x	n_5	n_4	n_3	n_2	n_1	n_0
Control byte 1	1	x	0	OS	T	TRI	I100	I50
Control byte 2	OFD	2IFD	SWC	SWD	SWE	SWF	SWG	SWH
Control byte 3	x	0	0	0	0	0	0	0

I²C Bus Function

AS1, AS2 define the I²C bus address
RD1, RD2 define the scaling factor of the refernce divider:

RD1	RD2	Scaling factor
0	0	1120
1	0	1152
0	1	1024
1	1	1536

n_j scaling factor (SF) of programmable divider
SF = SUM (n_j 2^j)
OS OS = 'H' switches off tuning output
T for T= 'H' reference signals describing the output frequencies of refernce divider and programmable divider are monitored at SWF (main divider) and SWC (reference divider)
TRI TRI = 'H' switches off charge pump

I50, I100 define the charge pump current:

I50	I100	Charge pump Current (nominal) /µA
'L'	'L'	50
'H'	'L'	102
'L'	'H'	151
'H'	'H'	203

OFD OFD = 'H' switches off frequency
2IFD 2IFD = 'H' doubles the frequency doubler output current
SWa SWa = 'H' switches on output current

I²C bus Data Transfer

Format:
START - ADR - ACK - <instruction set> - STOP
The <instruction set> consists of a sequence of divider bytes and control bytes each followed by ACK. Divider byte i must be followed by divider byte i + 1 (control byte 1 if i = 3) or the instruction set must be finished. Control bytes have to be handled accordingly.

Examples:

START - ADR - ACK - DB1 - ACK - DB2 - ACK - DB3 - ACK - CB1 - ACK - CB2 - ACK - CB3 - ACK - STOP
START - ADR - ACK - CB1 - ADK - CB2 - ACK - STOP

However:

START - ADR - ACK - DB1 - ACK - CB1 - ACK - STOP is not allowed.

Description:

START start condition
STOP stop condition
ACK acknowledge
ADR address byte
DBi divider byte i (i = 1, 2, 3)
CBi control byte i (i = 1, 2, 3)

I²C Bus Timing

The values of the drawn periods in figure 3, are specified in the section 'Electrical Characteristics'. A typical pulse diagram is shown in figure 4. **Please note:** due to the I²C bus specification, the MSB of a byte is transmitted first, the LSB last.

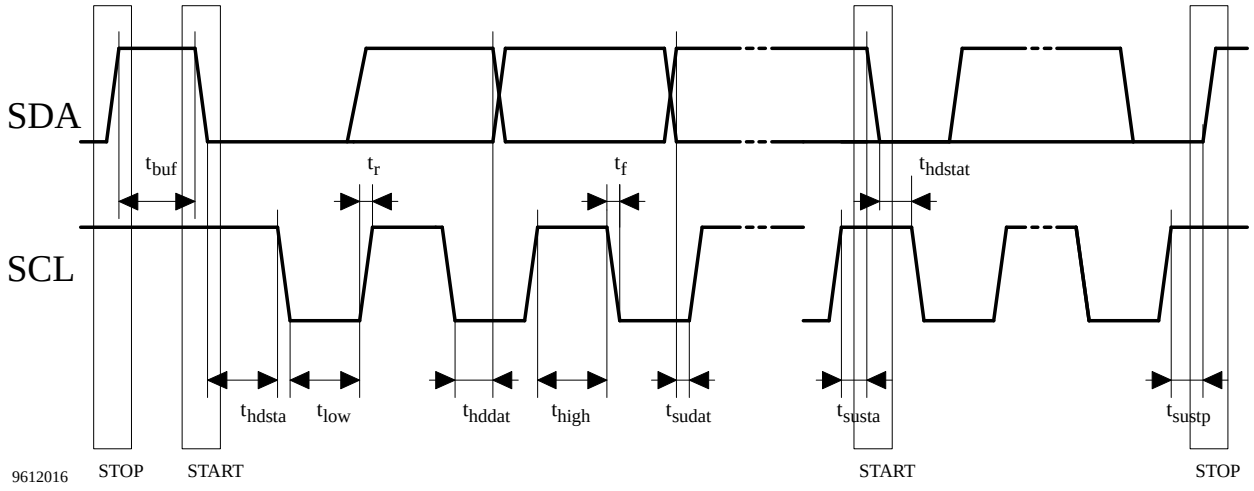


Figure 3.

Typical Pulse Diagram

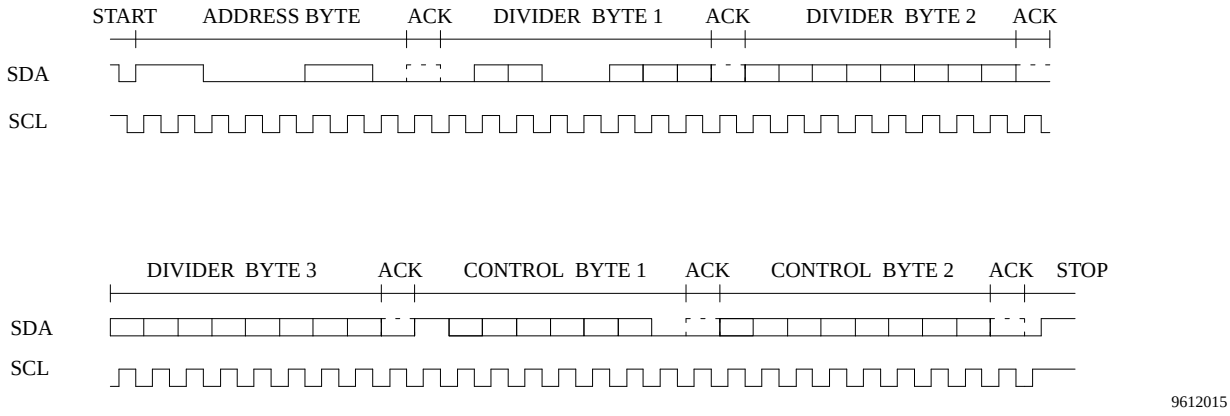


Figure 4.

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Value	Unit
Supply voltage	VS		–0.3 to 5.5	V
RF input voltage (AC)	RF, NRF		1	V_{pp}
Reference input voltage (AC)	REF, NREF		1	V_{pp}
I^2C bus input/ output voltage	SCL SDA		–0.3 to V_s	V
SDA output current	SDA		5	mA
Address select voltage	ADR		–0.3 to V_s	V
Switch output current	SWa	Open collector	4	mA
Switch output voltage	SWa	Open collector	–0.3 to 5.5	V
PLCK output current	PLCK	Open collector	0.5	mA
PLCK output voltage	PLCK	Open collector	–0.3 to 5.5	V
Frequency doubler output voltage	FDO, NFDO	Open collector	V_s–1 to 5.5	V
Ambient temperature range	T_{amb}		–40 to 85	°C
Junction temperature	T_j		125	°C
Storage temperature	T_{stg}		–40 to 125	°C

Thermal Resistance

Parameter	Symbol	Conditions	Value	Unit
Junction ambient	R_{thJA}	SSO20	140	K/W

Electrical Characteristics

Test conditions: V_S = 5 V, T_{amb} = 27°C, unless otherwise specified

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Supply voltage		V_S	4.5	5	5.5	V
Supply current V_S	SW_a = ‘L’, PLCK = ‘L’, TRI = ‘L’, OS = ‘L’, I50 = ‘H’, I100 = ‘H’, OFD = ‘L’, 2IFD = ‘L’	I_S	12.0	15.1	18.1	mA
Scaling factor of programmable divider		SF	2048		32767	
Scaling factor of reference divider	RD1 = ‘L’, RD2 = ‘L’ RD1 = ‘H’, RD2 = ‘L’ RD1 = ‘L’, RD2 = ‘H’ RD1 = ‘H’, RD2 = ‘H’	SF_{ref}		1120 1152 1024 1536		
Tuning step	17.920 MHz/ 18.432 MHz/ 16.384 MHz/ 24.576 MHz ref. frequency	f_{rast}		16		kHz

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
RF input, RF, NRF						
Input frequency range	V_S = 4.5 V, T_{amb} = 20°C		70		500	MHz
Input sensitivity		V_{rfs}		10	20	mV_{rms}
Max. input signal		V_{rfmax}			300	mV_{rms}
Input impedance	Differential	Z_{rf}		200		Ω
VSWR		$VSWR_{rf}$		2		
REF input, REF, NREF						
Input frequency range	V_S = 4.5 V, T_{amb} = 20°C	f_{ref}	5	17.92 18.432	30	MHz
Input sensitivity		V_{refs}		10	50	mV_{rms}
Max. input signal		V_{refmax}			300	mV_{rms}
Input impedance	Single ended	Z_{ref}		2.7 2.5		kΩ pF
Phase detector, PD						
Charge pump	I100 = 'H', I150 = 'H' I100 = 'H', I50 = 'L' I100 = 'L', I50 = 'H' I100 = 'L', I50 = 'L' TRI = 'H'	$\pm I_{PD4}$ $\pm I_{PD3}$ $\pm I_{PD2}$ $\pm I_{PD1}$ $\pm I_{PD, TRI}$	± 160 ± 120 ± 80 ± 40	± 203 ± 151 ± 102 ± 50	± 240 ± 180 ± 120 ± 60 ± 100	µA µA µA µA nA
Phase noise	I100 = 'H', I50 = 'H'	L_{PD}		–155		dBc/Hz
Lock indication, PLCK						
Leakage current	V_{PLCK} = 5.5 V	$I_{PLCK, L}$			10	µA
Saturation voltage	IPLCK = 0.5 mA	$V_{PLCK, s}$ at			0.5	V
Frequency doubler, FDO, NFDO						
Output current	$V_{FDO} = V_S$ $V_{NFDO} = V_S$ 2IFD = 'L'	I_{FDOL}, I_{NFDOL}	0.4	0.5	0.6	mA_{pp}
	$V_{FDO} = V_S$ $V_{NFDO} = V_S$ 2IFD = 'H'	I_{FDOH} I_{NFDOH}	0.8	1.0	1.2	mA_{pp}
Minimum output voltage	V_S = 5 V	V_{FDO} V_{NFDO}	4			V
Switches, SWa						
Leakage current	V_{SWa} = 5.5 V	$I_{SW, L}$			10	µA
Saturation voltage	I_{SWa} = 4 mA	V_{SW}, sat			0.5	V
Address selection, ADR						
AS1 = 0, AS2 = 0			0		0.1 V_S	
AS1 = 0, AS2 = 1				open		
AS1 = 1, AS2 = 0			0.4 V_S		0.6 V_S	
AS1 = 1, AS2 = 1			0.9 V_S		V_S	
I^2C bus, SCL, SDA						
Input voltage, SCL/SDA	'HIGH' 'LOW'	V_H V_L	3		5.5 1.5	V V
Output voltage SDA (open collector)	I_{SDA} = 2 mA SDA = 'L'				0.4	V
SCL clock frequency		f_{SCL}	0.1		100	kHz
Rise time (SCL, SDA)		t_r			1	µs
Fall time (SCL, SDA)		t_f			300	ns

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Time before new transmis-sion can be started		t_{buf}	4.7			µs
SCL 'H' perion		t_{high}	4			µs
SCL 'L'		t_{low}	4.7			µs
Hold time START		t_{hdsta}	4			µs
Set up time START		t_{susta}	4.7			µs
Set up time STOP		t_{sustp}	4.7			µs
fHold time DATA		t_{hddat}	0			µs
Set up time DATA		t_{sudat}	250			ns

Application Circuit

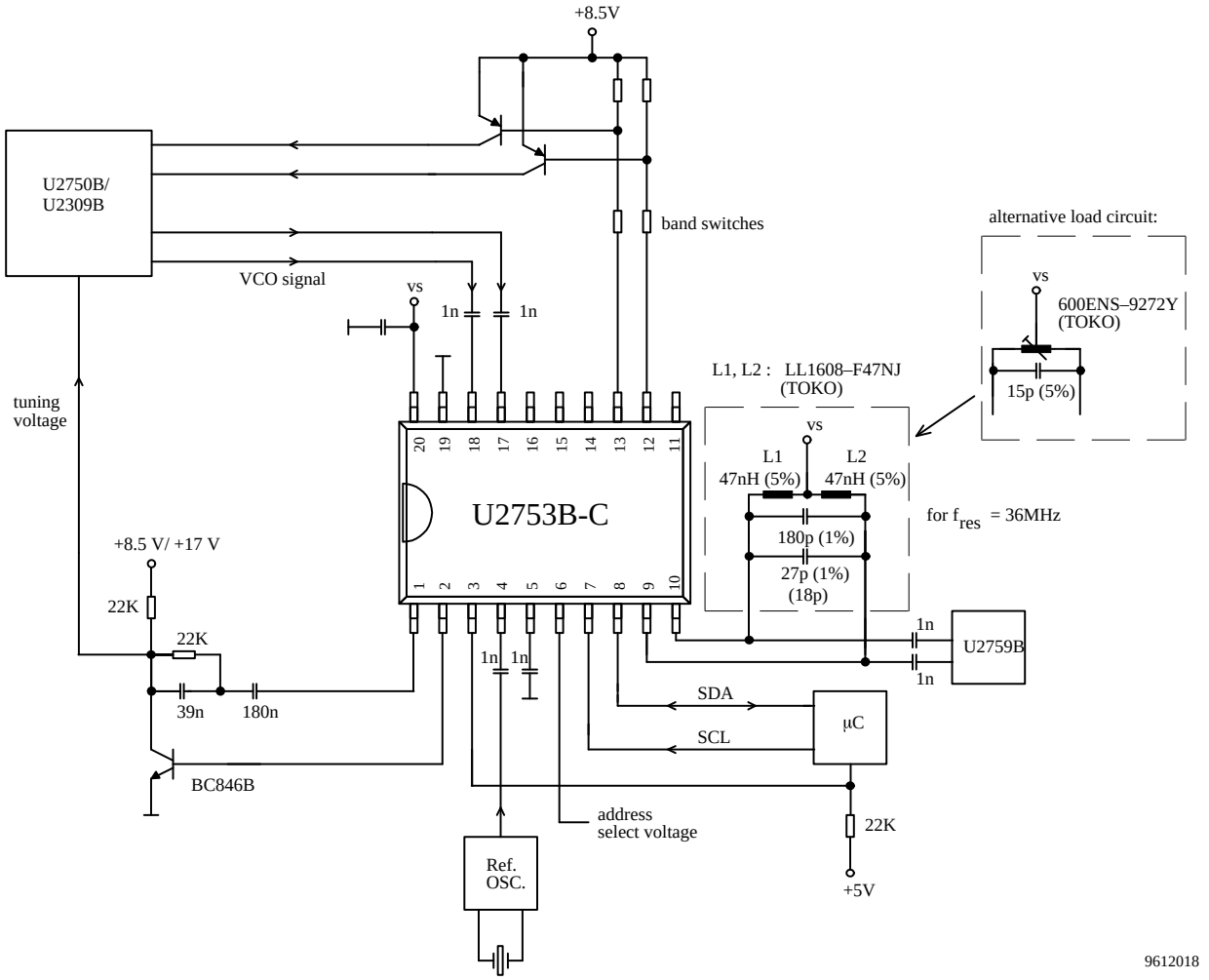
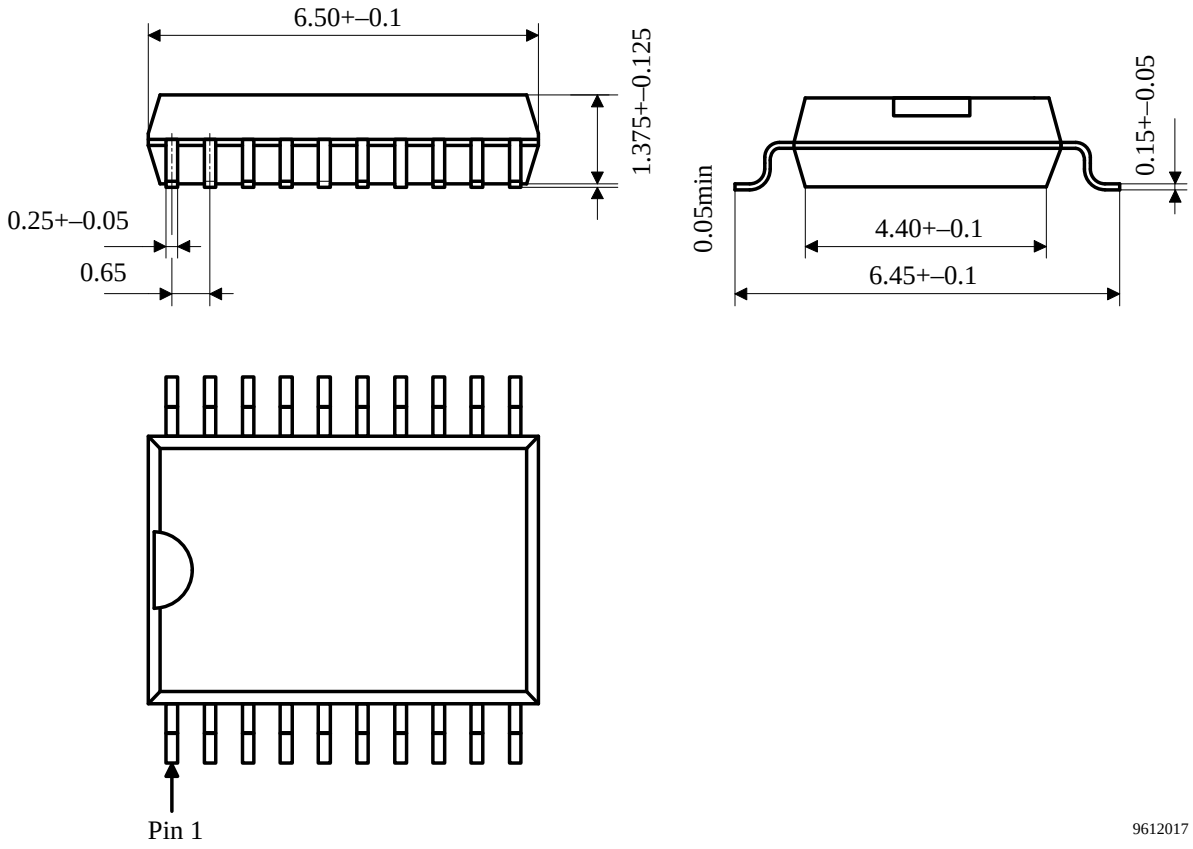


Figure 5.

Package SSO20

Dimensions in mm



Ozone Depleting Substances Policy Statement

It is the policy of **TEMIC TELEFUNKEN microelectronic GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC TELEFUNKEN microelectronic GmbH semiconductor division has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

TEMIC TELEFUNKEN microelectronic GmbH, P.O.B. 3535, D-74025 Heilbronn, Germany
Telephone: 49 (0)7131 67 2831, Fax number: 49 (0)7131 67 2423