# U6809B

# Fail-Safe IC with Relay Driver and Lamp Driver

## Description

The U6809B is designed to support the fail-safe function of a safety-critical system e.g., ABS. It includes a relay driver, two independent short-circuit-protected lamp drivers which are supplied by redundant ground lines, two monitoring circuits of the lamp driver output voltage and output current, a watchdog controlled by an external R/C-network and a reset circuit initiated by an over- and undervoltage condition of the 5-V supply providing a positive and a negative reset signal.

## Features

- Digital self-supervising watchdog with hysteresis
- Three 250-mA output drivers
- One relay driver, two lamp drivers
- Lamp drivers with auxiliary ground
- Lamp drivers short-circuit protected
- Lamp drivers with status feedback
- Enable output
- Over-/undervoltage detection and reset
- All power outputs protected against standard transients
- All power outputs protected against 40-V load dump
- Automatically activated lamp drivers if $V_S$ is disconnected
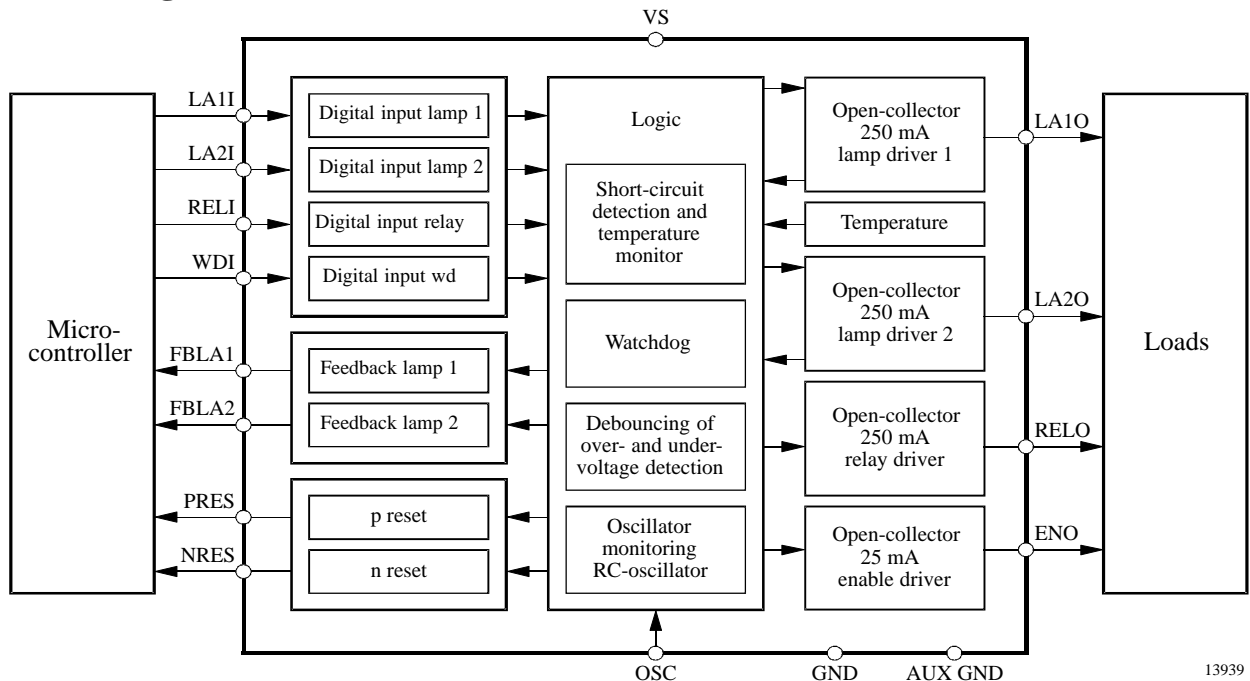- Automatically activated lamp drivers via AUX GND if standard ground is disconnected

## Block Diagram



Figure 1. Block diagram

## Ordering Information

| Extended Type Number | Package | Remarks |
|---|---|---|
| U6809B | SO20 special lead frame | |

# U6809B
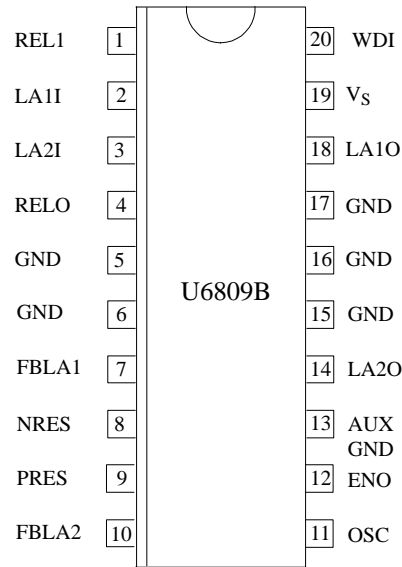
## Pin Description



Table 1  Pining and circuit description

| Pin | Name | Type | Function | Logic |
|---|---|---|---|---|
| 1 | RELI | Digital input | Activation of relay driver | L: driver on<br>H: driver off |
| 2 | LA1I | Digital input | Activation of lamp 1 driver | L: driver off<br>H: driver on |
| 3 | LA2I | Digital input | Activation of lamp 2 driver | L: driver off<br>H: driver on |
| 4 | RELO | Open collector driver output | Fail-safe relay driver | Driver off:——<br>driver on: L |
| 5, 6 | GND | Supply | Standard ground | |
| 7 | FBLA1 | Digital output | Feedback lamp1 | See table 2 and 3 |
| 8 | NRES | Digital output | Negative reset signal | Reset: L<br>no reset:H |
| 9 | PRES | Digital output | Positive reset signal | Reset: H<br>no reset:L |
| 10 | FBLA2 | Digital output | Feedback lamp 2 | See table 2 and 3 |
| 11 | OSC | Analog input | Ext. RC for watchdog timer | |
| 12 | ENO | Open collector output | Watchdog disable output | Watchdog ok: ——<br>watchdog n ok: L |
| 13 | AUX GND | Supply | Auxiliary ground of lamp drivers | |
| 14 | LA2O | Open collector driver output | Warning lamp driver | Driver off: ——<br>driver on: L |
| 15, 16, 17 | GND | Supply | Standard ground | |
| 18 | LA1O | Open collector driver output | Warning lamp driver | Driver off: ——<br>driver on: L |
| 19 | VS | Supply | 5 V supply | |
| 20 | WDI | Digital input | Watchdog trigger signal | Pulse sequence |

## Detailed Block Diagram with External Components
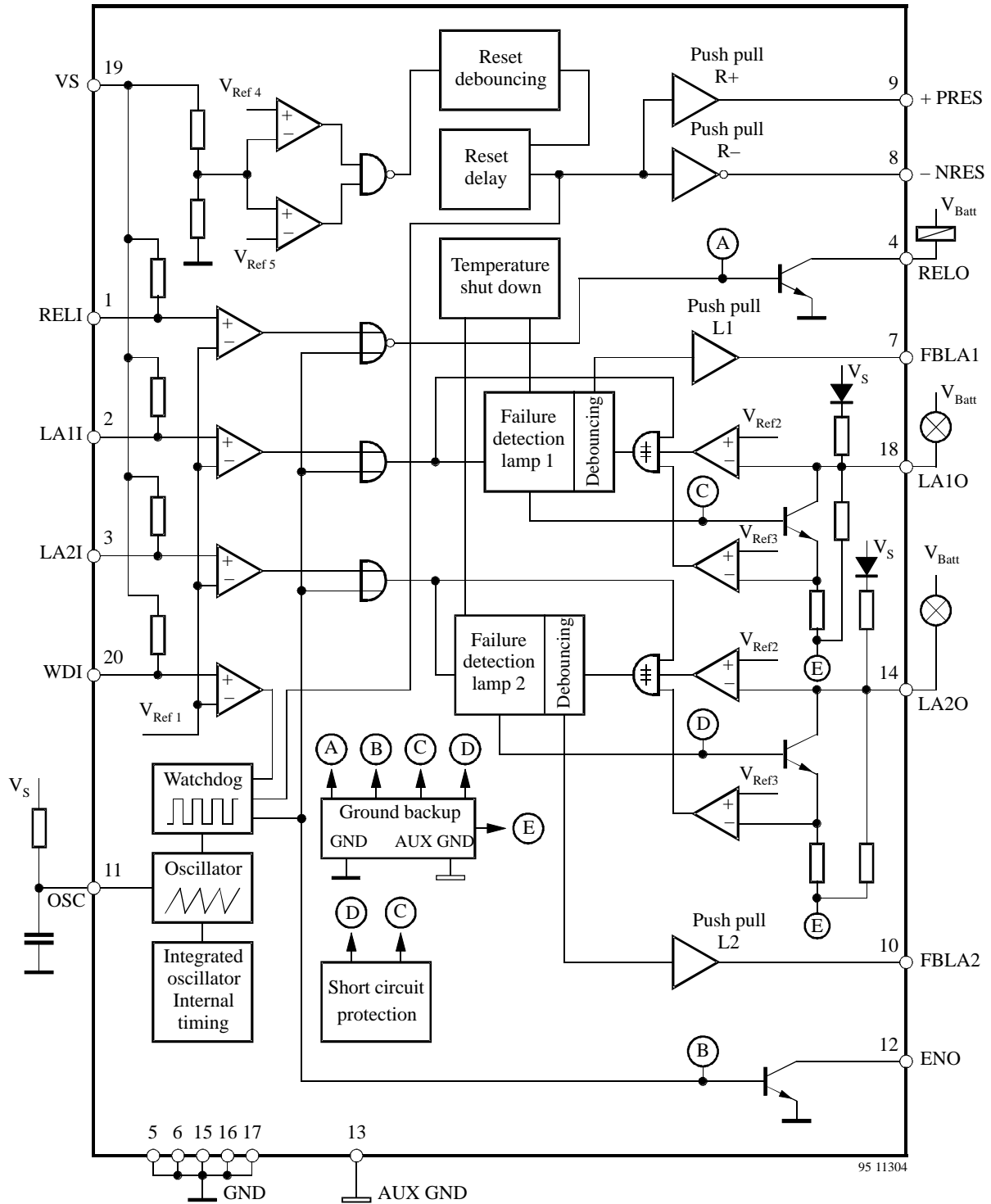


Figure 2.  Detailed block diagram

Table 2  Thruth table for lamp drivers and lamp feedback

| Inputs | | | Outputs | | | Comment |
|---|---|---|---|---|---|---|
| Lamp (I) | Lamp Voltage | Lamp Current | Lamp Driver Current | Lamp Current | Feedback Lamp | |
| 0 | 1 | 0 | off | off | 1 | Output ok or open (internal pull up) or shorted to $V_{Batt}$ |
| 0 | 1 | 1 | on | off | 1 | Output shorted to $V_{Batt}$ and faulty input level |
| 0 | 0 | 1 | on | on | 0 | Internal driver activated caused by internal failure |
| 0 | 0 | 0 | off | on | 0 | Output shorted to GND |
| 1 | 0 | 1 | on | on | 0 | Output ok |
| 1 | 1 | 1 | on | off | 1 | Output shorted to $V_{Batt}$ |
| 1 | 1 | 0 | off | off | 1 | Internal driver deactivated caused by internal failure or thermal shutdown |
| 1 | 0 | 0 | off | on/off | 1 | Output shorted to GND or open |

**Explanation:**

Lamp voltage is logic 1 if output voltage > threshold voltage detection

Lamp voltage is logic 0 if output voltage < threshold voltage detection

Lamp current is logic 1 if output current > threshold current detection

Lamp current is logic 0 if output current < threshold current detection

Table 3  Table of fault detection

| Condition | Feedback Lamp | |
|---|---|---|
| | Lamp Input is 0 (Lamp off) | Lamp Input is 1 (Lamp on) |
| Normal operation | 1 | 0 |
| Lamp output shorted to GND | 0 (= detection) | 1 (= detection) |
| Lamp output shorted to VBat | 1 (= no detection) | 1 (= detection) |
| Lamp output open | 1 (= no detection) | 1 (= detection) |
| Feedback shorted to GND | 0 (= detection) | 0 (= no detection) |
| Feedback shorted to Vs | 1 (= no detection) | 1 (= detection) |
| Lamp input shorted to GND | 1 (= no detection) | 1 (= detection) |
| Lamp input shorted to Vs | 0 (= detection) | 0 (= no detection) |

## Fail-Safe Functions

A fail-safe IC has to maintain its monitoring function even if there is a fault condition at one of the pins (e.g. short circuit). This ensures that a microcontroller system would not be brought into a critical status. A critical status is reached if the system is not able to actuate a warning lamp and switch off the relay. The following table shows fault conditions for different pins during which the IC still works as a fail-safe device.

Table 4  Table of fault conditions

| Pin | Function | Short to Vs | Short to VBat | Short to GND | Open Circuit |
|---|---|---|---|---|---|
| LA2O | Short-circuit proof driver for warning lamp | LA2O partly on | LA2O off | LA2O on | LA2O off |
| LA2I | Digital input to activate warning lamp | LA2O on | LA2O on | LA2O off | LA2O on |
| FBLA2 | Digital feedback of warning lamp | Faulty feedback | Faulty feedback | Faulty feedback | Faulty feedback |
| LA1O | Short-circuit proof driver for warning lamp | LA1O partly on | LA1O off | LA1O on | LA1O off |
| LA1I | Digital input to activate warning lamp | LA1O on | LA1O on | LA1O off | LA1O on |
| FBLA1 | Digital feedback of warning lamp | Faulty feedback | Faulty feedback | Faulty feedback | Faulty feedback |
| RELI | Digital input to activate the fail-safe relay | Relay off | Relay off | Relay on | Relay off |
| WDI | Watchdog trigger input | Watchdog reset | Watchdog reset | Watchdog reset | Watchdog reset |
| OSC | Capacitor and resistor of watch-dog | Watchdog reset | Watchdog reset | Watchdog reset | Watchdog reset |

# Description of the Watchdog

## Abstract

The microcontroller is monitored by a digital window watchdog which accepts an incomming trigger signal of a constant frequency for correct operation. The frequency of the trigger signal can be varied in a broad range as the watchdog's time window is determined by external R/C components.

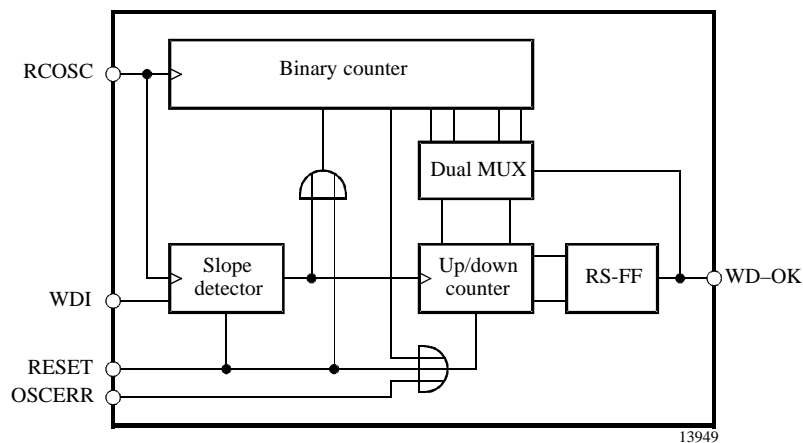The following description refers to the block diagram (Fig. 2)



Figure 3.  Watchdog block diagram

# U6809B

## WDI Input (Pin 20)

The microcontroller has to provide a trigger signal with the frequency $f_{WDI}$ which is fed to the WDI input. A positive edge of $f_{WDI}$ detected by a slope detector resets the binary counter and clocks the up/down counter additionally. The latter one counts only from 0 to 3 or reverse. Each correct trigger increments the up/down counter by 1, each wrong trigger decrements it by 1. As soon as the counter reaches status 3 the RS flip-flop is set; see Fig. 4 (Watchdog state diagram). A missing incoming trigger signal is detected after 250 clocks of the internal watchdog frequency $f_{RC}$ (see WD-OK output) and resets the up-/down counter directly.

## RCOSC Input

With an external R/C circuitry the IC generates a time base (frequency $f_{RC}$) independent from the microcontroller. The watchdog's time window refers to a frequency of

$$f_{RC} = 100 \times f_{WDI}$$

## Reset Input

During power-on and under-/overvoltage detection a reset signal is fed to this pin. It resets the watchdog timer and sets the initial state.

During power on and under/overvoltage detection a reset signal is fed to this pin. It resets the watchdog timer and sets the initial state.

## WD – OK Output

After the up/down counter is incremented to status 3 (see Fig. 4, WD state diagram) the RS flip-flop is set and the WD-OK output becomes logic "1". This information is available for the microcontroller at the open collector output ENO. If on the other hand the up/down counter is decremented to 0 the RS flip flop is reset, the WD OK output and the ENO output are disabled. The WD OK output also controls a dual MUX stage which shifts the time window by one clock after a successful trigger thus forming a hysteresis to provide stable conditions for the evaluation of the trigger signal "good or false". The WD OK signal is also reset in the case the watchdog counter is not reset after 250 clocks (missing trigger signal).
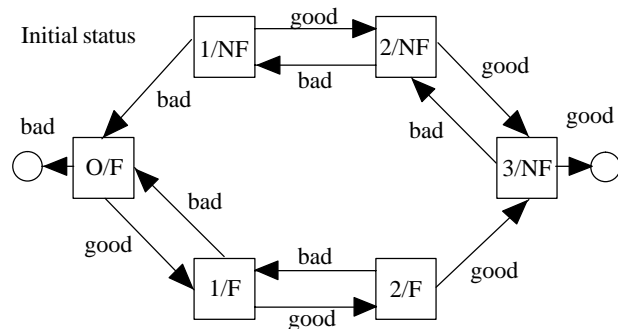
## Watchdog State Diagram



Figure 4. Watchdog state diagram

## Explanation

In each block, the first character represents the state of the counter. The second notation indicates the fault status of the counter. A fault status is indicated by an "F" and a no fault status is indicated by an "NF". When the watchdog is powered up initially, the counter starts out at the 0/F block (initial state). "good" indicates that a pulse has been received whose width resides within the timing window. "bad" indicates that a pulse has been received whose width is either too short or too long.

## Watchdog-Window Calculation

### Example with recommended values

$C_{osc} = 3.3$ nF    (should be preferably 10%, NPO)

$R_{osc} = 39$ kΩ    (may be 5%, $R_{osc} < 100$ kΩ due to leakage current and humidity)

### RC Oscillator

$$t_{WDC} \text{ (s)} = 10^{-3} \times [C_{osc} \text{ (nF)} \times [(0.00078 \times R_{osc} \text{ (k}\Omega\text{))} + 0.0005]]$$

$$f_{WDC} \text{ (Hz)} = 1 / (t_{WDC})$$

### Watchdog WDI

$$f_{WDI} \text{ (Hz)} = 0.01 \times f_{WDC}$$

| | | |
|---|---|---|
| $t_{WDC} = 100$ µs | –> | $f_{WDC} = 10$ kHz |
| $f_{WDI} = 100$ Hz | –> | $t_{WDI} = 10$ ms |

**WDI pulse width for fault detection after 3 pulses:**

Upper watchdog window

Minimum: $169/f_{WDC} = 16.9$ ms $\to f_{WDC} / 169 = 59.1$ Hz
Maximum: $170/f_{WDC} = 17.0$ ms $\to f_{WDC} / 170 = 58.8$ Hz

Lower watchdog window

Minimum: $79/f_{WDC} = 7.9$ ms $\to f_{WDC} / 79 = 126.6$ Hz
Maximum: $80/f_{WDC} = 8.0$ ms $\to f_{WDC} / 80 = 125.0$ Hz

**WDI dropouts for immediate fault detection:**

Minimum: $250/f_{WDC} = 25$ ms
Maximum: $251/f_{WDC} = 25.1$ ms

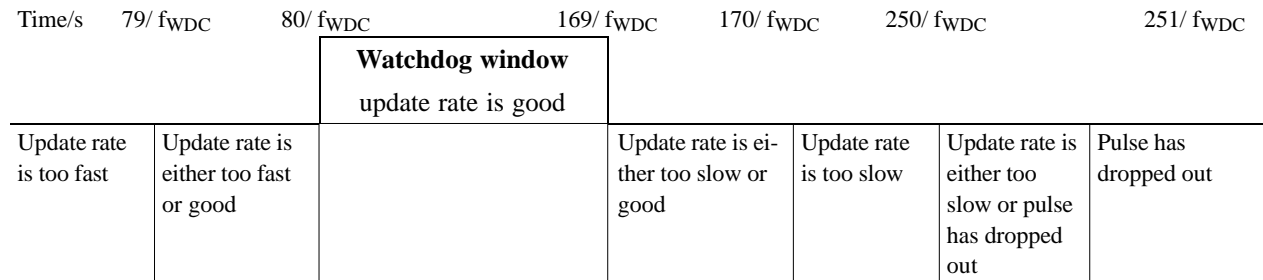| Time/s | $79/f_{WDC}$ | $80/f_{WDC}$ | | $169/f_{WDC}$ | $170/f_{WDC}$ | $250/f_{WDC}$ | $251/f_{WDC}$ |
|---|---|---|---|---|---|---|---|
| | | | **Watchdog window** update rate is good | | | | |
| | Update rate is too fast | Update rate is either too fast or good | | Update rate is either too slow or good | Update rate is too slow | Update rate is either too slow or pulse has dropped out | Pulse has dropped out |

Figure 5. Watchdog timing diagram with tolerances

**Remark to reset delay**

The duration of the over- or undervoltage pulses determines the enable- and reset output. A pulse duration shorter than the debounce time has no effect on the outputs. A pulse longer than the debounce time results in the first reset delay. If a pulse appears during this delay, a 2nd delay time is triggered. Therefore, the total reset delay time can be longer than specified in the data sheet.

## Absolute Maximum Ratings

| Parameters | Symbol | Value | Unit |
|---|---|---|---|
| Supply voltage range | $V_S$ | – 0.2 to 16 | V |
| AUX GND offset voltage to GND | $V_{AUX}$ | +/– 1.5 | V |
| AUX GND offset current to GND | $I_{AUX}$ | – 600 | mA |
| Power dissipation $V_S = 5$ V; $T_{amb} = 125°C$ | $P_{tot}$ | 700 | mW |
| Thermal resistance | $R_{thjc}$ | 25 | K/W |
| Junction temperature | $T_j$ | 150 | °C |
| Ambient temperature range | $T_{amb}$ | –40 to 125 | °C |
| Storage temperature range | $T_{stg}$ | –55 to 155 | °C |

# U6809B

## Electrical Characteristics

$V_S = 5$ V, $T_{amb} = -40$ to $+125°C$; reference pin is GND; $f_{intern} = 100$ kHz $+ 50\% - 45\%$,
$f_{WDC} = 10$ kHz $\pm 10\%$; $f_{WDI} = 100$Hz

| Parameter | Test Conditions / Pins | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Supply voltage** | | | | | | |
| Operation range general | | $V_S$ | 4.5 | | 5.5 | V |
| Operation range reset | | $V_S$ | 1.5 | | 16.0 | V |
| **Supply current** | | | | | | |
| Lamp driver on, relay off | $T_{amb} = -40°C$<br>$T_{amb} = 125°C$ | | | | 40<br>35 | mA<br>mA |
| Lamp driver off, relay on | $T_{amb} = -40°C$<br>$T_{amb} = 125°C$ | | | | 25<br>20 | mA<br>mA |
| Lamp driver off, relay off | $T_{amb} = -40°C$<br>$T_{amb} = 125°C$ | | | | 15<br>10 | mA<br>mA |
| **Auxiliary ground (AUX GND)** | | | | | | |
| AUX GND offset voltage operation range | $T_{amb} = -40°C$<br>$T_{amb} = 90°C$<br>$T_{amb} = 125°C$ | | $-1.2$<br>$-0.65$<br>$-0.5$ | | 1.2<br>1.0<br>0.8 | V<br>V<br>V |
| AUX GND offset voltage to GND | $I_{AUX} = -600$ mA | | $-1.7$ | | 3.0 | V |
| **Digital inputs (LA1I, LA2I, REL1 and WDI)** | | | | | | |
| Detection low | | | $-0.2$ | | $0.2 \times V_S$ | V |
| Detection high | | | $0.7 \times V_S$ | | $V_S + 0.5$ V | V |
| Resistance to $V_S$ | | | 10 | | 40 | k$\Omega$ |
| Input current low | Input voltage = 0 V | | 100 | | 550 | $\mu$A |
| Input current high | Input voltage = $V_S$ | | $-5$ | | 5 | $\mu$A |
| **Digital outputs; lamp driver feedbacks (FBLA1, FBLA2)** | | | | | | |
| Voltage low | $I \leq 1.6$ mA | | 0 | | 0.5 | V |
| Voltage high | $I \leq 10$ A<br>$10$ A $\leq I \leq 1.6$mA | | $0.8 \times V_S$<br>$0.7 \times V_S + 0.1$ | | $V_S$<br>$V_S$ | V<br>V |
| Threshold voltage detection | | | $0.4 \times V_S$ | | $0.5 \times V_S$ | V |
| Threshold current detection | | | 10 | | 50 | mA |
| **Digital outputs (PRES and NRES)** | | | | | | |
| Voltage high | $I \leq 100$A | | $0.7 \times V_S + 0.1$ | | $V_S$ | V |
| Voltage low | $I \leq 1$ mA | | 0 | | 0.3 | V |
| **Digital output (ENO) with open collector** | | | | | | |
| Saturation voltage low | $I \leq 25$ mA | | 0 | | 0.3 | V |
| Clamping voltage | | | 26 | | 30 | V |
| Current limit low | | | 25 | | | mA |
| Leakage current | $V_{ENO} = 5$ V<br>$V_{ENO} = 16$ V<br>$V_{ENO} = 26$ V | | | | 20<br>100<br>200 | $\mu$A<br>$\mu$A<br>$\mu$A |
| **Lamp drivers (LA1O and LA2O) with integrated pull-up resistor** | | | | | | |

## Electrical Characteristics (continued)

$V_S$ = 5 V, $T_{amb}$ = –40 to + 125°C; reference pin is GND; $f_{intern}$ = 100 kHz + 50% – 45%,
$f_{WDC}$ = 10 kHz ± 10%; $f_{WDI}$ = 100Hz

| Parameter | Test Conditions / Pins | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Saturation voltage | I ≤ 125 mA; $V_S$ = 5 V | | | | 0.5 | V |
| | I ≤ 125 mA; $V_S$ = 0 V | | | | 1.5 | V |
| Saturation voltage 250mA requires enhanced heat sink | I ≤ 250 mA; $V_S$ = 5 V | | | | 1.0 | V |
| | I ≤ 250 mA; $V_S$ = 0 V | | | | 2.0 | V |
| | I ≤ 250 mA; no GND | | | | 3.0 | V |
| Maximum load current | $T_{amb}$ = 90°C | | 250 | | | mA |
| | $T_{amb}$ = 125°C | | 180 | | | mA |
| Clamping voltage | | | 26 | | 30 | V |
| Leakage current | $V_{LA1O, LA2O}$ = 16 V | | | | 1 | mA |
| | $V_{LA1O, LA2O}$ = 26 V | | | | 3 | mA |
| Threshold current limitation | | | 0.5 | | 1.0 | A |
| Pull-up resistor | | | 2 | | 17 | kΩ |
| **Relay driver (RELO)** | | | | | | |
| Saturation voltage | I ≤ 250 mA | | | | 0.5 | V |
| Maximum load current | $T_{amb}$ = 90°C | | 250 | | | mA |
| | $T_{amb}$ = 125°C | | 200 | | | mA |
| Clamping voltage | | | 26 | | 30 | V |
| Leakage current | $V_{Bat}$ = 16 V | | | | 20 | μA |
| | $V_{Bat}$ = 26 V | | | | 200 | μA |
| **Reset and $V_S$ control** | | | | | | |
| Lower reset level | | $V_S$ | 4.5 | | 4.8 | V |
| Upper reset level | | $V_S$ | 5.2 | | 5.5 | V |
| Hysteresis | | | 25 | | | mV |
| Reset debounce time | | | 120 | | 500 | μs |
| Reset delay | | | 20 | | 80 | ms |
| **Watchdog timing** | | | | | | |
| Feedback reaction time (FBLA1, FBLA2) | no fault, edge at LA1I, LA2I | $t^{FB}$ | 2.56 | | 12.8 | ms |
| Minimum lamp input toggle time for a securely feedback reaction | no fault, pulse at LA1I, LA2I | $t_{P,FB}$ | 10.24 | | | ms |
| Power-on-reset prolongation time | | $t_{POR}$ | 34 .3 | | 103.1 | ms |
| Detection time for RC-oscillator fault | $V_{RC}$ = const. | $t_{RCerror}$ | 81.9 | | 246 | ms |
| Time interval for over-/ under voltage detection | | $t_{D,OUV}$ | 0.16 | | 0.64 | ms |
| Reaction time of NRES output on over-/under voltage | | $t_{R,OUV}$ | 0.187 | | 0.72 | ms |

## Electrical Characteristics (continued)

$V_S$ = 5 V, $T_{amb}$ = –40 to + 125°C; reference pin is GND; $f_{intern}$ = 100 kHz + 50% – 45%,
$f_{WDC}$ = 10 kHz ± 10%; $f_{WDI}$ = 100Hz

| Parameter | Test Conditions / Pins | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Minimum toggle time for a securely broken ground detection | | $t_{P,BGND}$ | 13.3 | | | μs |
| Maximum reaction time for broken ground detection | | $t_{R,BGND}$ | | | 100 | μs |
| Nominal frequency for WDI | $f_{RC} = 100 \times f_{WDI}$ | $f_{WDI}$ | 10 | | 130 | Hz |
| Nominal frequency for RC | $f_{WDI} = 1/100 \times f_{RC}$ | $f_{RC}$ | 1 | | 13 | kHz |
| Minimum pulse duration for a securely WDI input pulse detection | | $t_{P,WDI}$ | 182 | | | μs |
| Frequency range for a correct WDI signal | | $f_{WDI}$ | 64.7 | | 112.5 | Hz |
| Number of incorrect WDI trigger counts for locking the outputs | | $n_{lock}$ | | 3 | | |
| Number of correct WDI trigger counts for releasing the outputs | | $n_{release}$ | | 3 | | |
| Detection time for a stucked WDI signal | $V_{WDI}$ = const. | $t_{WDIerror}$ | 24.5 | | 25.5 | ms |
| **Watchdog timing relative to $f_{RC}$** | | | | | | |
| Minimum pulse duration for a securely WDI input pulse detection | | | | 2 | | cycles |
| Frequency range for a correct WDI signal | | | 80 | | 170 | cycles |
| Hysteresis range at the WDI ok margins | | | | 1 | | cycle |
| Detection time for a stucked WDI signal | $V_{WDI}$ = const. | | 250 | | 251 | cycles |

## Protection against transient voltages according to ISO TR 7637–3 level 4 (except pulse 5)

| Pulse | Voltage | Source Resistance * | Rise Time | Duration | Amount |
|---|---|---|---|---|---|
| 1 | – 110 V | 10 Ω | 100 V/s | 2 ms | 15.000 |
| 2 | + 110 V | 10 Ω | 100 V/s | 0.05 ms | 15.000 |
| 3a | – 160 V | 50 Ω | 30 V/ns | 0.1 s | 1 h |
| 3b | + 150 V | 50 Ω | 20 V/ns | 0.1 s | 1 h |
| 5 | 40 V | 2 Ω | 10 V/ms | 250 ms | 20 |

\*    Lamp drivers:      1.2 W lamps to be added to the source resistance
    Relay driver:      relay coil with $R_{min}$ = 70 Ω to be added to the source resistance.

## Application Hints

a.) The lamp output pins LA1O and LA2O may need to be protected by external protection diodes against reversed battery (e.g. BAV 202) in order to avoid a reset during negative pulses.

b.) If pilot lamps with a wattage of P > 1.2 W are connected external Zener diodes are mandatory.
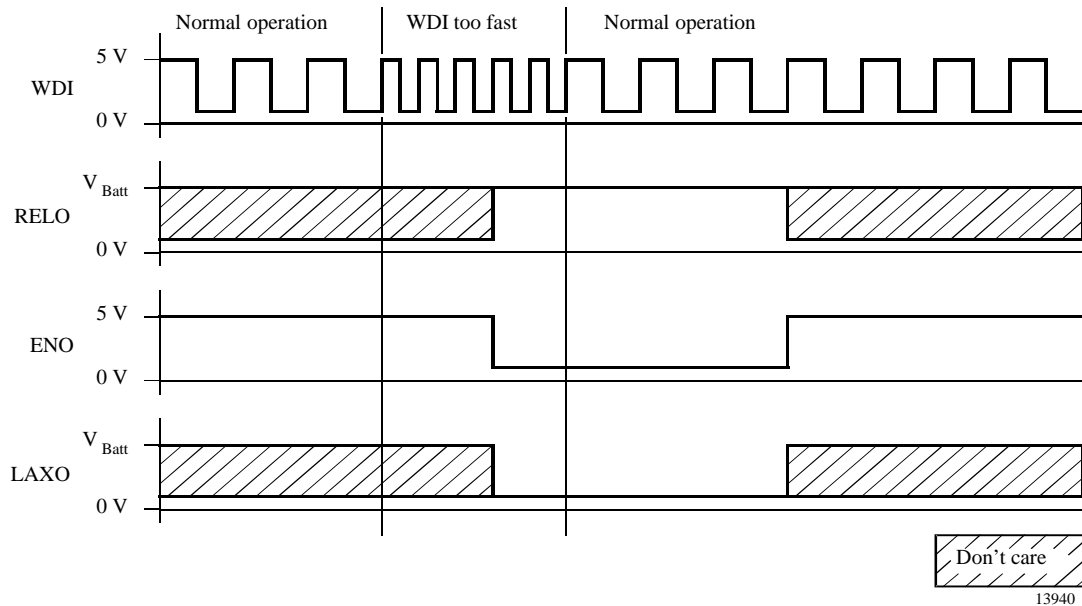
## Timing Diagrams
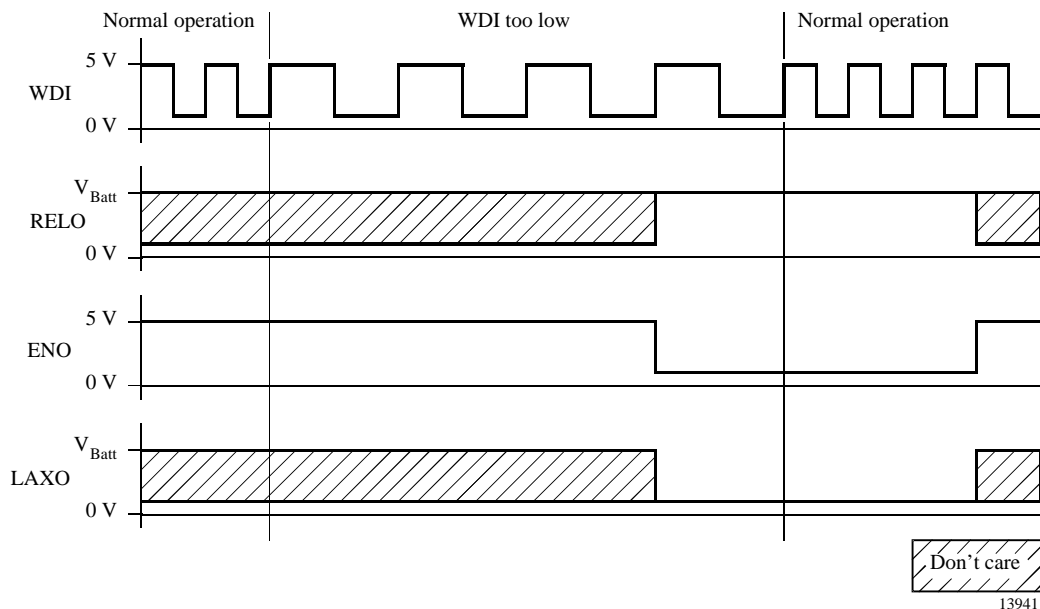


Figure 6. Watchdog in too fast condition



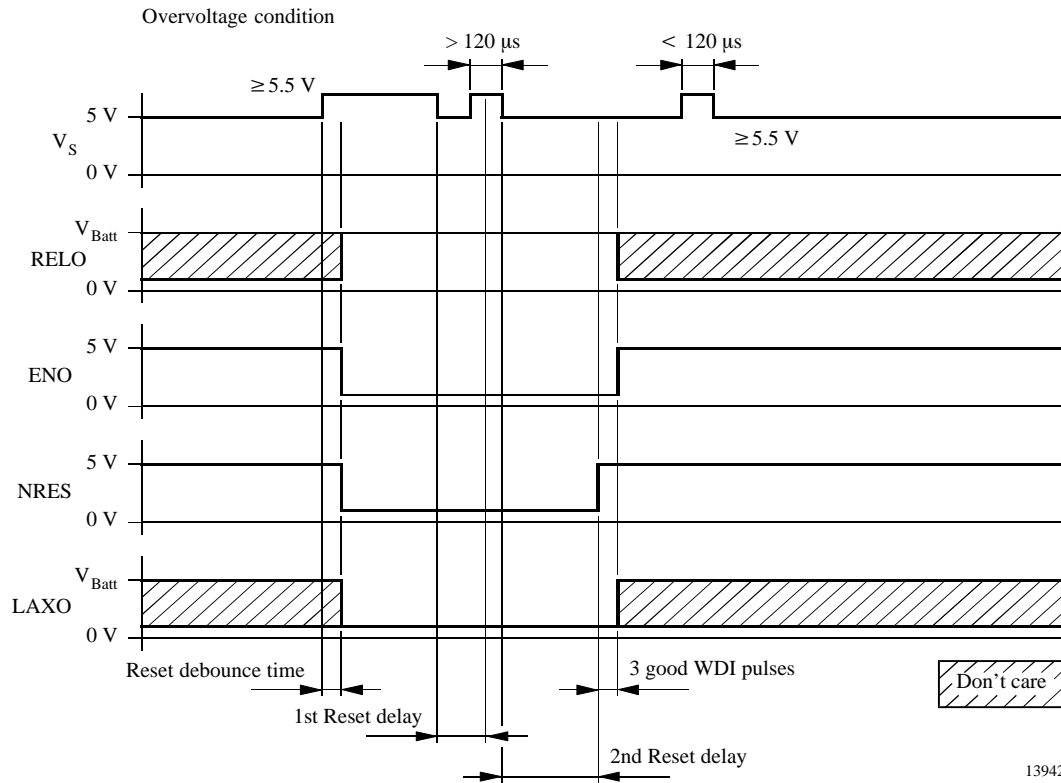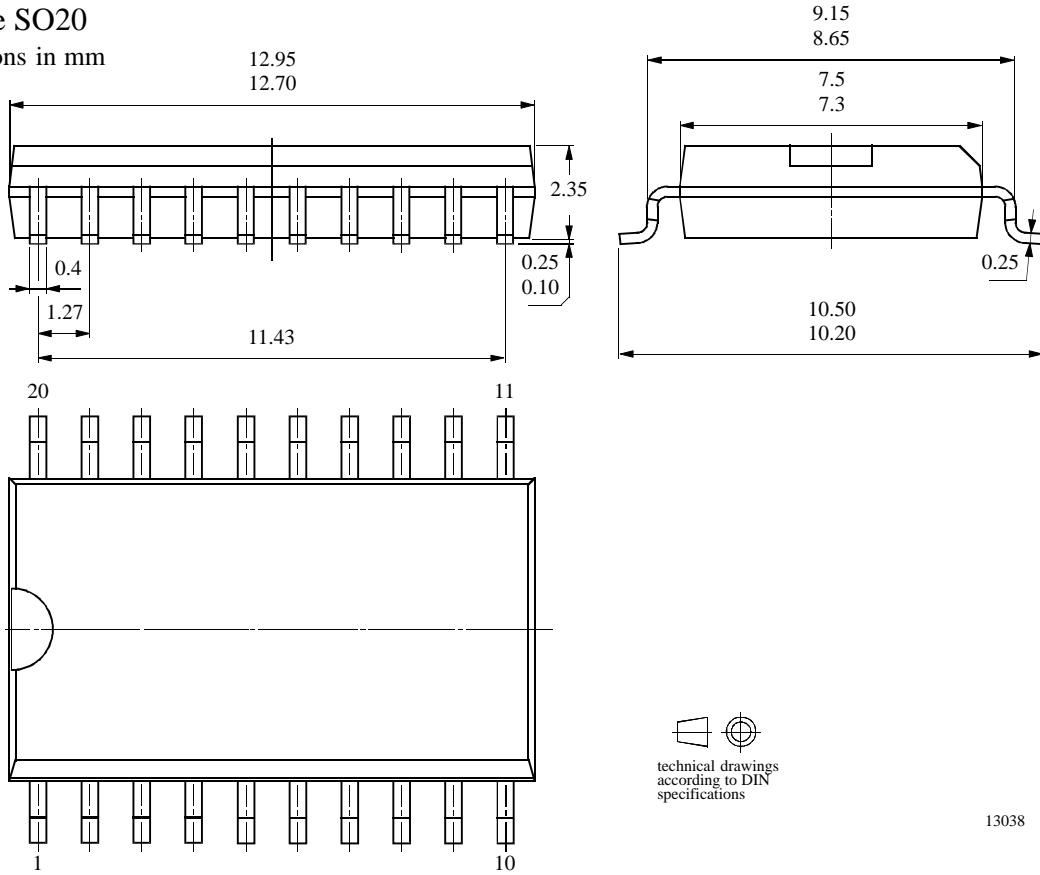Figure 7. Watchdog in too slow condition

Overvoltage condition

Figure 8. Overvoltage condition

Undervoltage condition
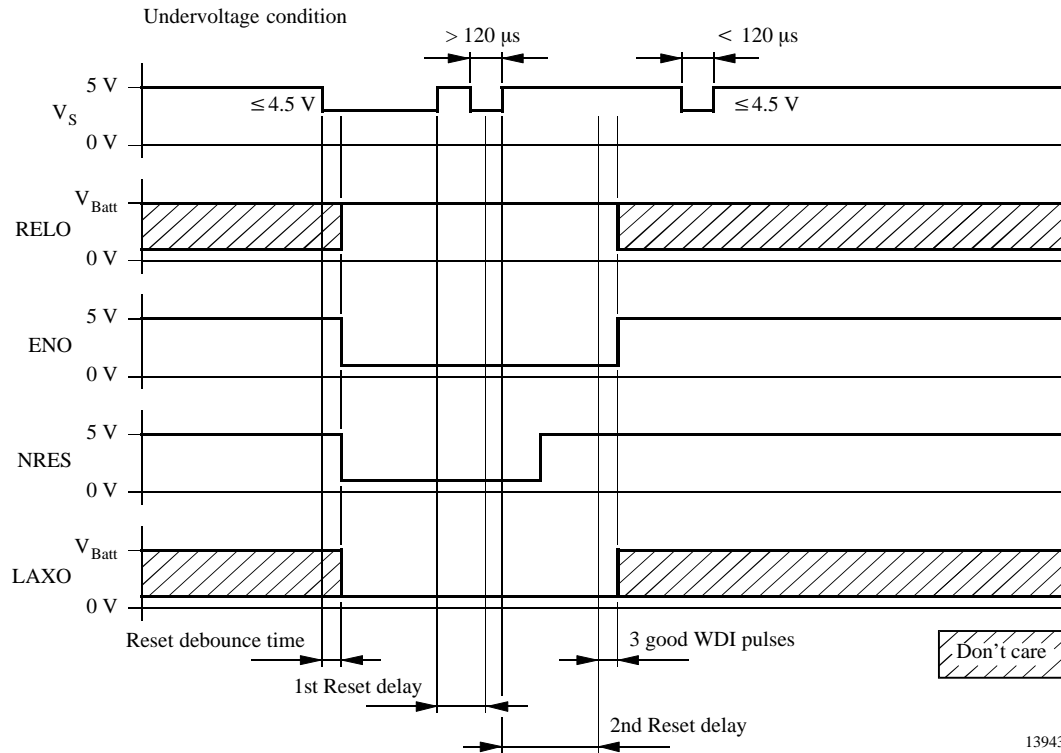
Figure 9. Undervoltage condition

## Package Information

Package SO20

Dimensions in mm

12.95
12.70

2.35

0.4

0.25
0.10

1.27

11.43

9.15
8.65

7.5
7.3

0.25

10.50
10.20

20    11

1    10

technical drawings
according to DIN
specifications

13038

## Ozone Depleting Substances Policy Statement

It is the policy of **Atmel Germany GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

**Atmel Germany GmbH** has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

**Atmel Germany GmbH** can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

**Data sheets can also be retrieved from the Internet:** http://www.atmel–wm.com