NEC

BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1677C

5 V-BIAS, +19.5 dBm OUTPUT, 1.8 GHz WIDE BAND SiMMIC AMPLIFIER

DESCRIPTION

The μPC1677C is a silicon monolithic integrated circuit designed as medium output power amplifier for high frequency system applications. Due to +17 dBm TYP. output at 1 GHz, this IC is recommendable for transmitter stage amplifier of L Band wireless communication systems. This IC is packaged in 8-pin plastic DIP.

This IC is manufactured using NEC's 20 GHz f_T NESAT™IV silicon bipolar process. This process uses silicon nitride passivation film and gold electrodes. These materials can protect chip surface from external pollution and prevent corrosion/migration. Thus, this IC has excellent performance, uniformity and reliability.

FEATURES

- Supply voltage : V_{CC} = 4.5 to 5.5 V
- Saturated output power : $P_{O(sat)}$ = +19.5 dBm TYP. @ f = 500 MHz
- Wideband response : f_u = 1.8 GHz TYP. @ 3dB bandwidth
- Power gain : G_P = 24 dB TYP. @ f = 500 MHz
- Isolation : ISL = 34 dB TYP. @ f = 500 MHz

APPLICATION

- PA driver for high frequency system.

ORDERING INFORMATION

Part Number	Package	Marking	Supplying Form
μPC1677C	8-pin Plastic DIP (300 mil)	C1677C	Plastic Magazine Case

Remark To order evaluation samples, please contact your local NEC sales office. (Part number for sample order: μPC1677C)

Caution Electro-static sensitive devices.

The information in this document is subject to change without notice.

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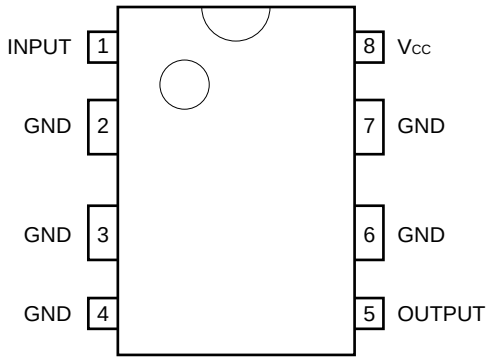
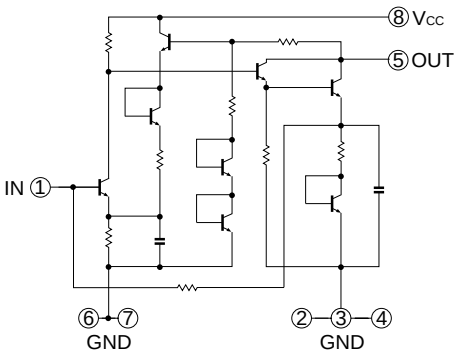
The mark ★ shows major revised points.

PIN CONNECTIONS



Pin No.	Pin Name
1	INPUT
2	GND
3	GND
4	GND
5	OUTPUT
6	GND
7	GND
8	V_{CC}

PIN EXPLANATION

Pin No.	Pin Name	Applied Voltage V	Function and Applications	Internal Equivalent Circuit
1	INPUT	–	Signal input pin. A internal matching circuit, configured with resisters, enables 50 Ω connection over a wide band. A multi-negative feedback circuit is designed to cancel the deviations of h_{FE} and resistance. This pin must be coupled to signal source with capacitor for DC cut.	 2, 3, 4, 6 and 7 are chorted by a lead frame.
2 3 4 6 7	GND	0	Ground pin. This pin should be connected to system ground with minimum inductance. Ground pattern on the board should be formed as possible. All the ground pins must be connected together with wide ground pattern to decrease impedance difference.	
5	OUTPUT	Voltage as same as V_{CC} through external inductor	Signal output pin. The inductor must be attached between V_{CC} and output pins to supply current to the internal output transistors.	
8	V_{CC}	4.5 to 5.5	Power supply pin, which biases the internal input transistors. This pin should be externally equipped with bypass capacitor to minimize its impedance.	

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Rating	Unit
Supply Voltage	V_{CC}	T_A = +25 °C, pin 5 and 8	6	V
Power Dissipation	P_D	Mounted on double copper clad 50 × 50 × 1.6 mm epoxy glass PWB (T_A = +85 °C)	750	mW
Operating Ambient Temperature	T_A		–45 to +85	°C
Storage Temperature	T_{stg}		–55 to +150	°C
Input Power	P_{in}	T_A = +25 °C	+10	dBm

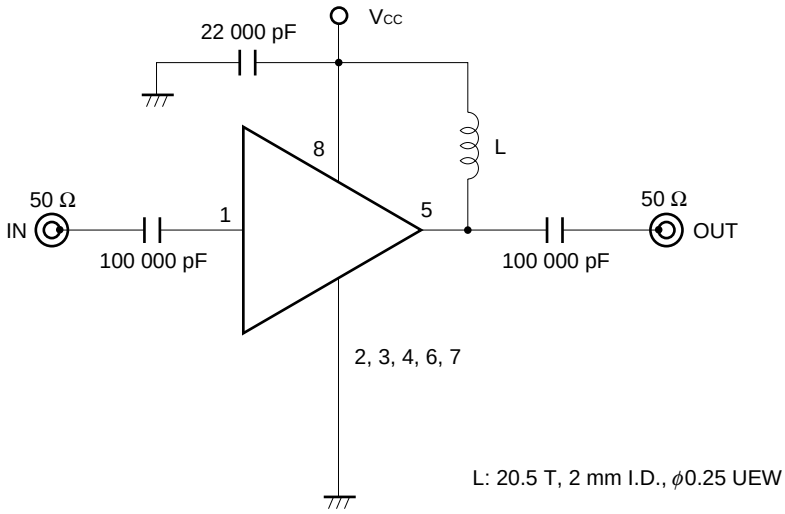
RECOMMENDED OPERATING RANGE

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Remark
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	The same voltage should be applied to pin 5 and 8.
Operating Ambient Temperature	T_A	–45	+25	+85	°C	

ELECTRICAL CHARACTERISTICS (T_A = +25 °C, V_{CC} = V_{out} = 5 V, Z_S = Z_L = 50 Ω)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Circuit Current	I_{CC}	No signal	63	77	93	mA
Power Gain	G_P	f = 500 MHz	22	24	26	dB
Noise Figure	NF	f = 500 MHz	–	6.0	8.0	dB
Upper Limit Operating Frequency	f_u	3 dB down below flat gain at 0.1 GHz	1.5	1.8	–	GHz
Isolation	ISL	f = 500 MHz	29	34	–	dB
Input Return Loss	RL_{in}	f = 500 MHz	10	13	–	dB
Output Return Loss	RL_{out}	f = 500 MHz	1	4	–	dB
Maximum Output Level	$P_{O(sat)}$	f = 500 MHz, P_{in} = +3 dBm	+17.5	+19.5	–	dBm

TEST CIRCUIT



Inductance for V_{CC} and output pin

Due to 50 mA consuming internal output stage transistor, this IC outputs medium power. This 50 mA current should be supplied into output pin (pin No. 5) through inductance. So, please connect inductance (e.g. 300 nH) between V_{CC} (pin 8) and output pin (pin 5).

Inductance is intended to DC and AC effects. As for DC effect, this inductance make internal-output-transistor maximum biased to output maximum +19.5 dBm. As for AC effect, this inductance make output-port-impedance higher to get enough gain.

For above reason, large inductance value make operation wide band. 300 nH inductance is recommendable because of specified circuit.

Capacitors for V_{CC}, input and output pins

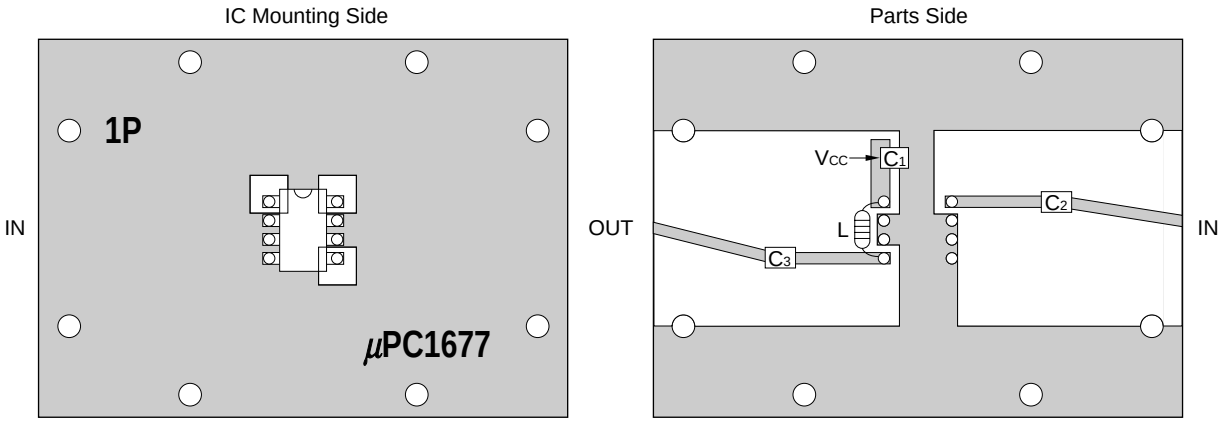
22 000 pF and 100 000 pF capacitors are recommendable as bypass capacitor for V_{CC} pin and coupling capacitors for input/output pins.

Bypass capacitor for V_{CC} pin is intended to minimize V_{CC} pin's ground impedance. Therefore, stable bias can be supplied against V_{CC} fluctuation.

Coupling capacitors for input/output pins are intended to minimize RF serial impedance and cut DC.

To get flat gain from 100 MHz up, 100 000 pF capacitors are assembled on the test circuit. [In the case of under 100 MHz operation, increase the value of coupling capacitor such as 1 μF. Because the coupling capacitors are determined by the equation of $C = 1/(2 \pi fZs)$.]

★ **ILLUSTRATION OF THE TEST CIRCUIT ASSEMBLED ON EVALUATION BOARD**



L: Manually wound coil

COMPONENT LIST

	Value
C_1	22000 pF
C_2, C_3	100000 pF
L	300 nH

Notes

1. 70 × 50 × 1.6 mm double sided copper clad polyimide board.

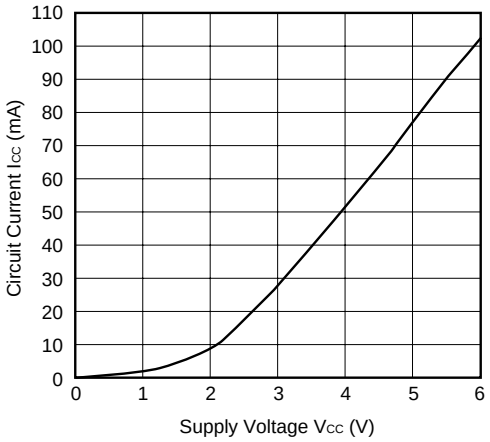
2. Solder plated on pattern

3. ○ ◯ : Through holes

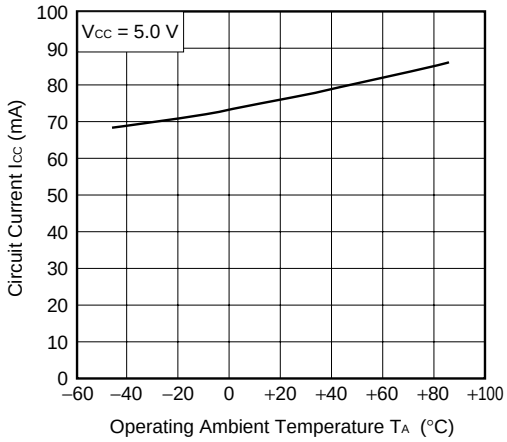
For more information on the use of this IC, refer to the following application note: USAGE AND APPLICATION OF SILICON MEDIUM-POWER HIGH-FREQUENCY AMPLIFIER MMIC (P12152E).

TYPICAL CHARACTERISTICS (T_A = +25 °C unless otherwise specified)

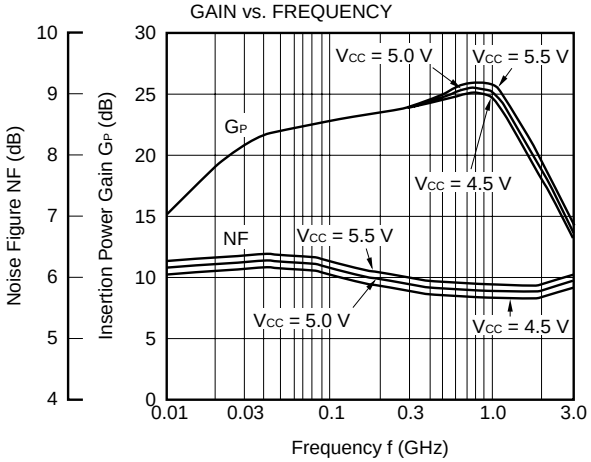
CIRCUIT CURRENT vs. SUPPLY VOLTAGE



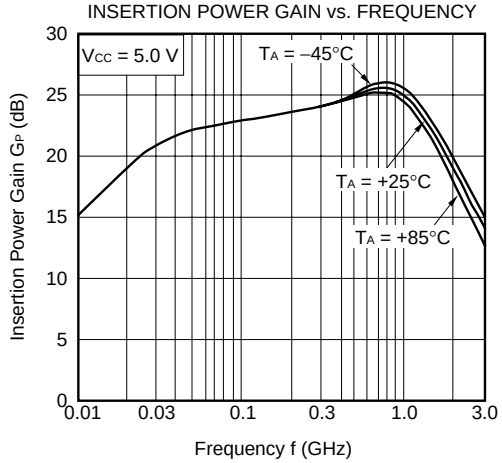
CIRCUIT CURRENT vs. OPERATING AMBIENT TEMPERATURE



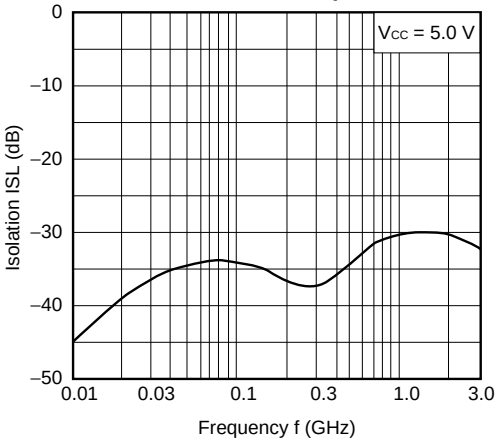
NOISE FIGURE AND INSERTION POWER GAIN vs. FREQUENCY



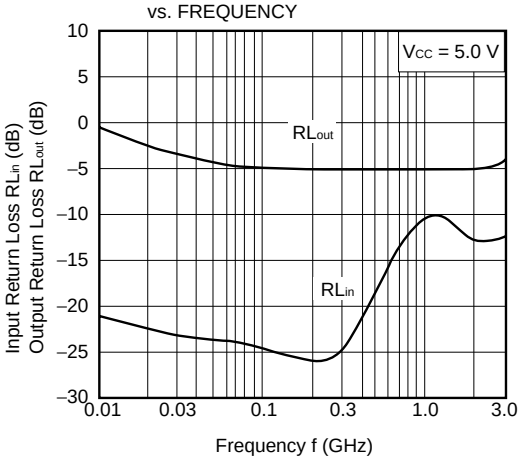
INSERTION POWER GAIN vs. FREQUENCY



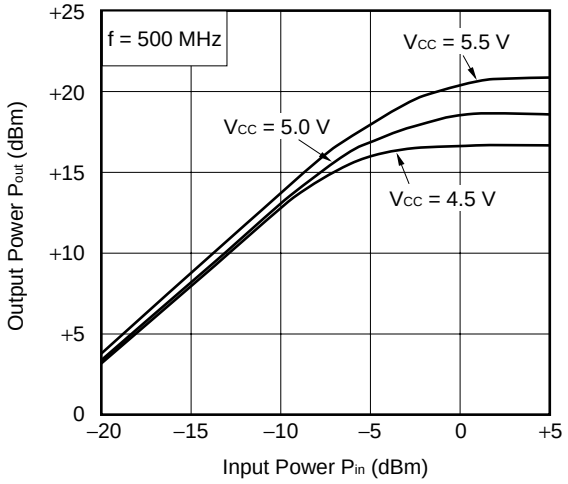
ISOLATION vs. FREQUENCY



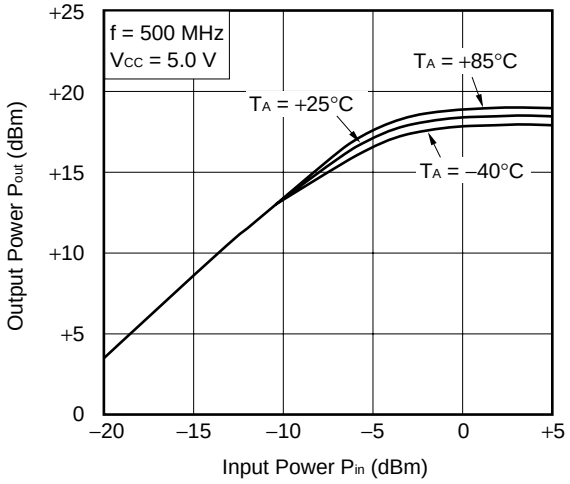
INPUT AND OUTPUT RETURN LOSS vs. FREQUENCY



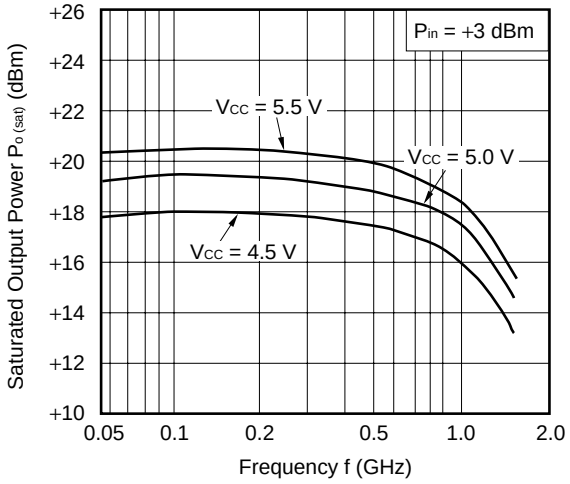
OUTPUT POWER vs. INPUT POWER



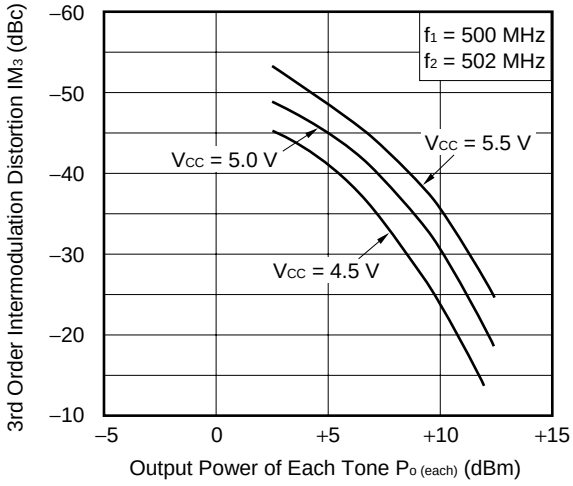
OUTPUT POWER vs. INPUT POWER



SATURATED OUTPUT POWER vs. FREQUENCY

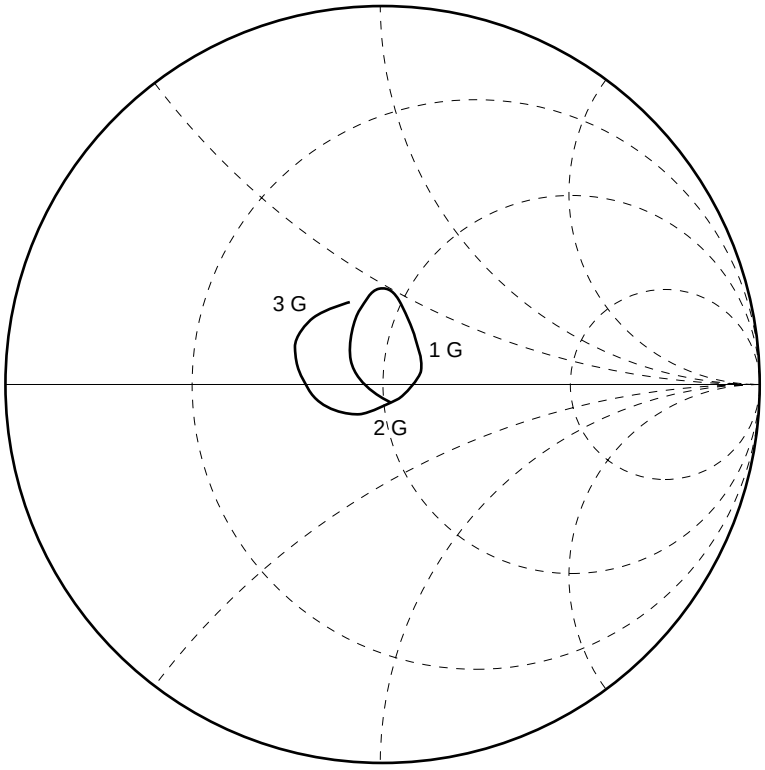


THIRD ORDER INTERMODULATION DISTORTION vs. OUTPUT POWER OF EACH TONE

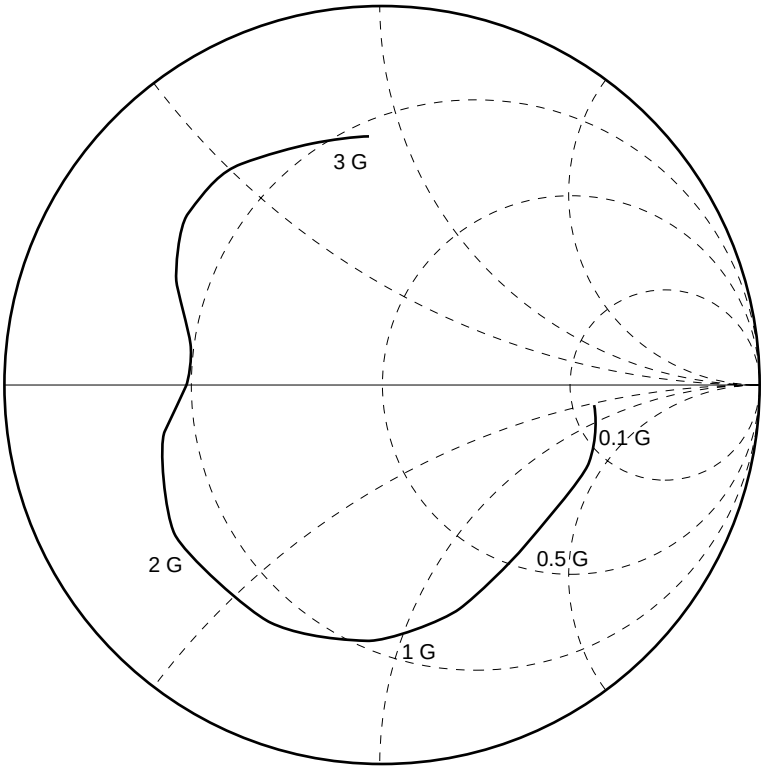


★ **S-PARAMETER (V_{CC} = V_{out} = 5.0 V)**

S_{11}-FREQUENCY



S_{22}-FREQUENCY



★ **TYPICAL S-PARAMETER VALUES (T_A = +25 °C)**

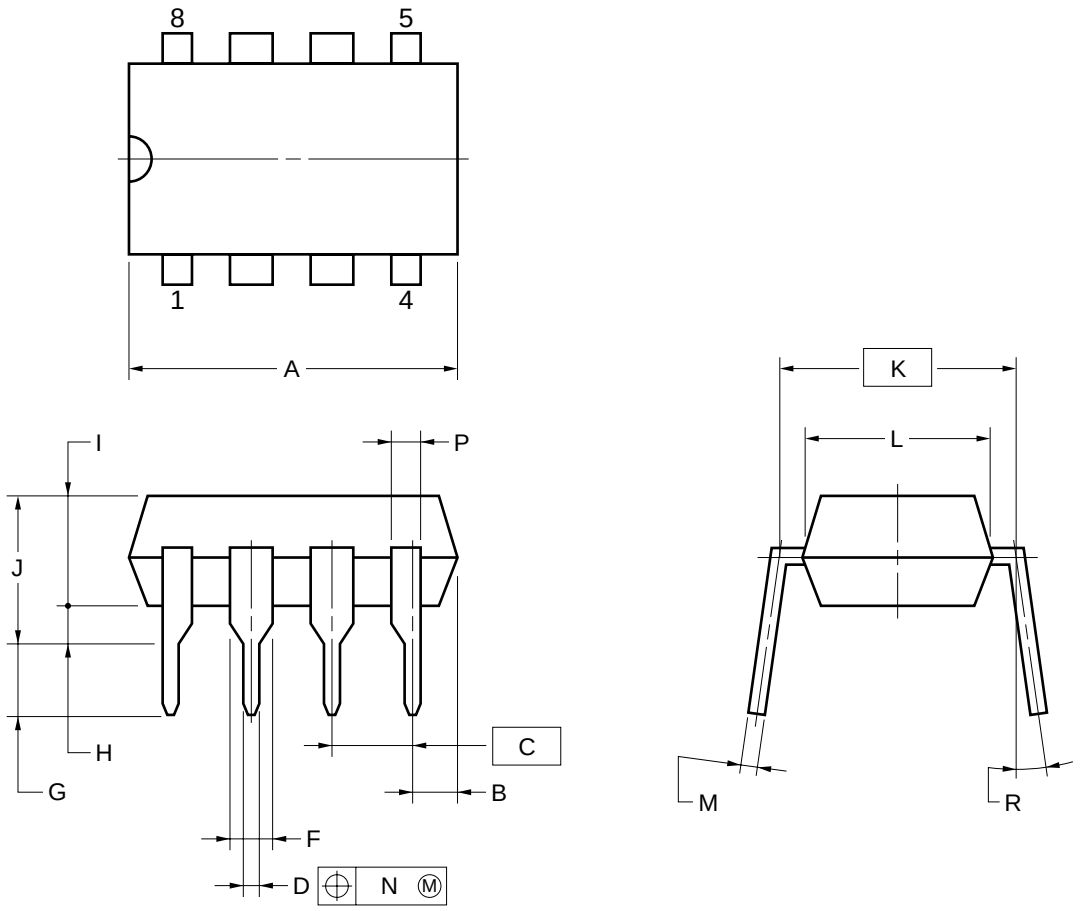
μPC1677C

V_{CC} = V_{out} = 5.0 V, I_{CC} = 77 mA

FREQUENCY	S_{11}		S_{21}		S_{12}		S_{22}		K
MHz	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG	
100.0000	.050	–60.4	13.659	–4.3	.018	–2.5	.554	–3.0	1.51
200.0000	.103	103.3	15.031	–25.0	.017	10.7	.575	–20.1	1.46
300.0000	.252	86.3	15.761	–45.8	.021	26.7	.556	–42.0	1.07
400.0000	.220	78.1	14.739	–50.3	.021	26.1	.535	–49.3	1.20
500.0000	.124	69.7	13.742	–48.4	.020	32.1	.569	–48.0	1.30
600.0000	.123	59.1	13.141	–53.7	.020	31.6	.574	–55.3	1.32
700.0000	.116	54.9	13.565	–60.1	.023	38.4	.606	–66.3	1.08
800.0000	.134	45.0	13.392	–66.0	.025	37.4	.594	–72.7	1.04
900.0000	.109	22.8	13.216	–69.7	.027	40.3	.623	–78.8	0.98
1000.0000	.112	13.7	13.942	–77.0	.027	41.2	.657	–86.0	0.87
1100.0000	.092	–2.7	15.392	–83.6	.032	42.5	.681	–107.9	0.77
1200.0000	.060	–12.7	16.419	–90.3	.035	38.4	.687	–113.9	0.73
1300.0000	.055	–26.0	17.235	–102.9	.036	39.2	.683	–122.8	0.74
1400.0000	.036	–52.8	18.528	–115.1	.038	38.7	.690	–134.9	0.73
1500.0000	.014	–122.3	18.252	–127.5	.041	37.1	.671	–144.5	0.75
1600.0000	.012	153.3	18.308	–143.2	.043	34.6	.631	–156.5	0.78
1700.0000	.037	119.2	17.699	–154.9	.046	31.8	.598	–167.4	0.80
1800.0000	.032	53.1	16.162	–166.3	.046	24.8	.514	–170.0	0.85
1900.0000	.040	58.1	15.643	–177.3	.047	22.1	.497	–176.9	0.86
2000.0000	.034	51.2	14.709	171.5	.048	20.7	.484	178.0	0.88
2100.0000	.030	2.8	13.794	161.6	.048	14.5	.463	176.0	0.91
2200.0000	.037	–83.1	13.120	152.3	.045	8.0	.510	174.1	0.91
2300.0000	.078	–117.6	12.483	139.9	.043	–1.0	.553	168.7	0.91
2400.0000	.127	–146.2	11.808	129.4	.037	–6.9	.605	161.6	0.95
2500.0000	.188	–176.6	10.880	115.8	.029	–10.6	.680	149.0	1.07
2600.0000	.255	154.8	9.246	101.0	.018	2.6	.718	134.0	1.64
2700.0000	.272	130.3	7.497	90.5	.020	35.8	.683	119.5	1.82
2800.0000	.237	115.9	6.031	86.4	.028	31.2	.610	111.3	1.88
2900.0000	.226	110.7	5.138	79.3	.028	29.9	.608	105.2	2.16
3000.0000	.235	108.2	4.424	76.5	.028	27.8	.613	100.4	2.45
3100.0000	.268	114.4	3.812	69.4	.022	18.6	.671	96.9	3.16

PACKAGE DIMENSIONS

8 PIN PLASTIC DIP (300 mil)



NOTES

1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	10.16 MAX.	0.400 MAX.
B	1.27 MAX.	0.050 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	0.50 ± 0.10	$0.020^{+0.004}_{-0.005}$
F	1.4 MIN.	0.055 MIN.
G	3.2±0.3	0.126±0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.4	0.252
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.25	0.01
P	0.9 MIN.	0.035 MIN.
R	0~15°	0~15°

P8C-100-300B,C-1

NOTES ON CORRECT USE

(1) Observe precautions for handling because of electro-static sensitive devices.
(2) Form a ground pattern as wide as possible to minimize ground impedance (to prevent undesired oscillation). All the ground pins must be connected together with wide ground pattern to decrease impedance difference.
(3) The bypass capacitor should be attached to V_{CC} line.
(4) The inductor must be attached between V_{CC} and output pins. The inductance value should be determined in accordance with desired frequency.
(5) The DC cut capacitor must be attached to input pin.

RECOMMENDED SOLDERING CONDITIONS

This product should be soldered under the following recommended conditions. For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

μPC1677C

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Wave Soldering	Soldering bath temperature: 260°C or below Time: 10 seconds or less Count: 1, Exposure limit[Note]: None	WS60-00-1

Note After opening the dry pack, keep it in a place below 25°C and 65% RH for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

For details of recommended soldering conditions for surface mounting, refer to information document SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL (C10535E).

ATTENTION
OBSERVE PRECAUTIONS
FOR HANDLING
ELECTROSTATIC
SENSITIVE
DEVICES

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M4 96.5