DATA SHEET

NEC

BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC2731GS

L-BAND SILICON DOWN-CONVERTER IC WITH AGC AMPLIFIER

DESCRIPTION

The μPC2731GS is a silicon monolithic integrated circuit designed for DBS tuner and mobile communications. This IC consists of double balanced mixer, local oscillator, IF amplifier, regulator and AGC amplifier. This means that L-band down-converter and AGC amplifier are integrated in 1 chip. This 1 chip IC is packaged in 20-pin SOP suitable for high-density surface mounting. Thus, this product contributes to produce physically-small DBS tuner and mobile communication equipments.

The μPC2731GS is manufactured using NEC's 20 GHz f_T NESAT™ III silicon bipolar process. This process uses silicon nitride passivation film and gold electrodes. These materials can protect chip surface from external pollution and prevent corrosion and migration. Thus, this IC has excellent performance, uniformity and reliability.

FEATURES

- L-Band Operation f_{RF} = 0.9 G to 2.0 GHz
- L-Band down-converter and AGC amplifier are integrated in 1 chip
- 50 Ω impedance output
- Supply voltage 5.0 V TYP.
- Circuit current $I_{CCTOTAL}$ = 69 mA (Down-converter: 42 mA, AGC Amplifier: 27 mA)
- Packaged in 20-pin SOP suitable for high-density surface mounting

★ APPLICATION

- L-Band receiver (0.9 to 2.0 GHz)

★ ORDERING INFORMATION

Part Number	Package	Supplying Form
μPC2731GS-E1	20-pin plastic SOP (7.62 mm (300))	Embossed tape 24 mm wide. Pin 1 indicates pull-out direction of tape. Qty 2.5 kp/reel.

Remark To order evaluation samples, please contact your local NEC sales office (Part number for sample order: μPC2731GS).

Caution Electro-static sensitive devices

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

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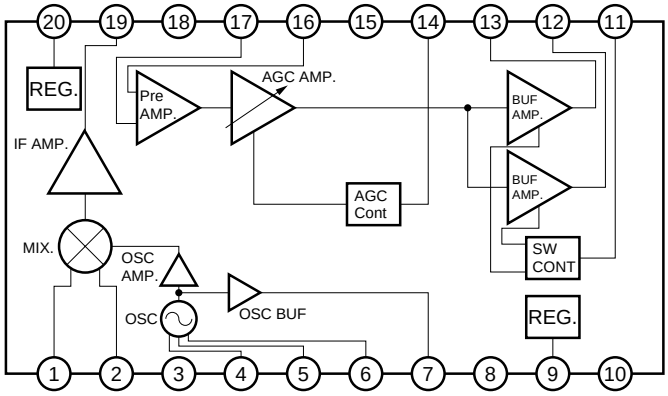
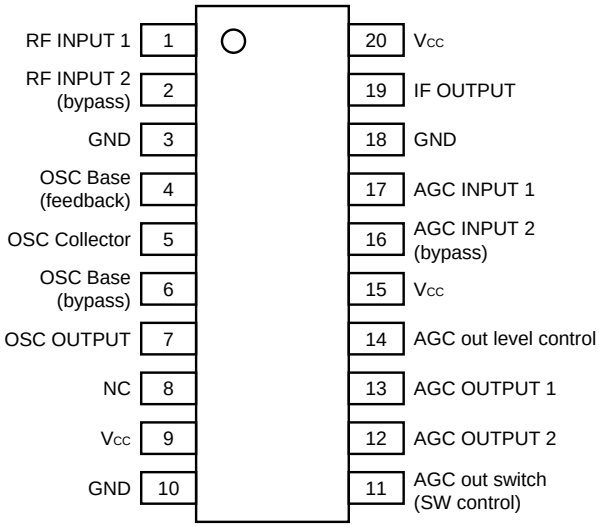
The mark ★ shows major revised points.

INTERNAL BLOCK DIAGRAM



PIN CONNECTIONS

(Top View)

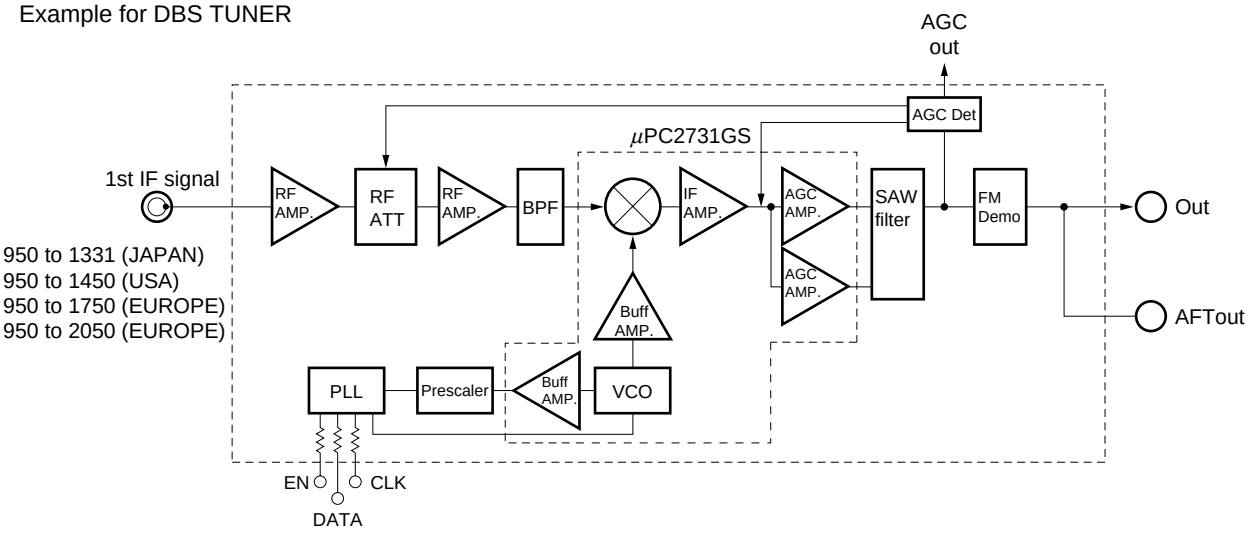


PRODUCT LINE-UP (T_A = +25°C, V_{CC} = 5.0 V)

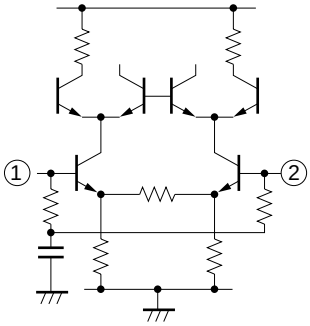
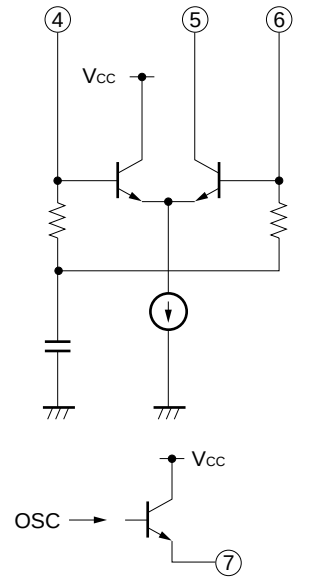
Main Feature	Part Number	f_{RF} (GHz)	CG (dB)	NF (dB)	D_{AGC} (dB)	$G_{AGC\ MAX.}$ (dB)	Package
50 Ω impedance output	μPC2721GR/GV	0.9 to 2.0	21	11	–	–	8-pin SOP/ SSOP
High impedance output	μPC2722GR/GV	0.9 to 2.0	18	11	–	–	8-pin SOP/ SSOP
• Equipped with AGC amplifier • 50 Ω impedance output	μPC2731GS	0.9 to 2.0	14	14	60	25	20-pin SOP

TYPICAL SYSTEM APPLICATION

Example for DBS TUNER

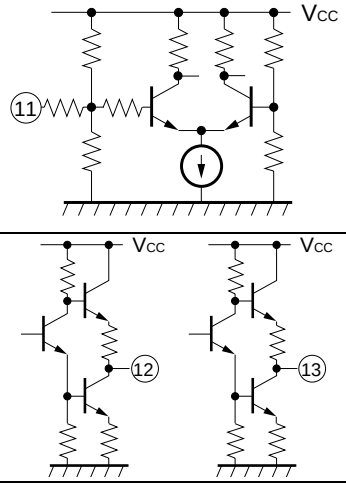
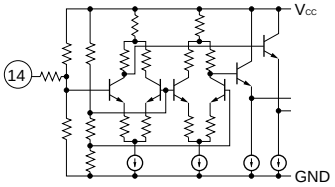
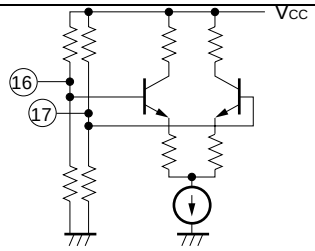
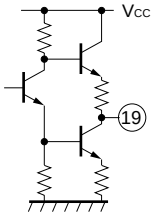


PIN EXPLANATIONS

Pin No.	Pin Name	Pin Voltage (V)	Function and Applications	Internal Equivalent Circuit
1	RF INPUT 1	2.5	① and ② pins are inputs for mixer designed as double balanced type. Either pin can be assigned for input and another for ground.	
2	RF INPUT 2 (bypass)	2.5		
3	GND	0[Note]	Must be connected to the system ground with minimum inductance. Ground pattern on the board should be formed as wide as possible. (Track length should be kept as short as possible.)	———
4	OSC Base (feedback)	2.9	Internal oscillator consist in balance amplifier. ④ and ⑤ pins should be externally equipped with tank resonater circuit in order to oscillate with feedback loop.	
5	OSC Collector	5.0	⑥ pin should be grounded through coupling capacitor (example: 0.5 pF).	
6	OSC Base (bypass)	2.9	⑤ pin is defined as open collector. This pin should be coupled through resistor or chock coil in order to adjust Q and be supplied voltage to. In case of undesired oscillation, adjust its Q lower to stabilize the operation.	
7	OSC OUTPUT	3.7	Oscillator output pin. Must be connected PLL synthesizer IC's input pin.	
8	NC	–	Non connection pin.	———
9	V_{CC}	5.0 ± 0.5[Note]	Supply voltage pin for AGC amplifier. Must be conneced bypass capacitor (example: 1 000 pF) to minimize ground impedance.	———
10	GND	0[Note]	Must be connected to the system ground with minimum inductance. Ground pattern on the board should be formed as wide as possible. (Track length should be kept as short as possible).	———

Note Externally supply voltage

<table>
<tr><th>Pin No.</th><th>Pin Name</th><th>Pin Voltage (V)</th><th>Function and Applications</th><th>Internal Equivalent Circuit</th></tr>
<tr><td>11</td><td>AGC out switch (SW control)</td><td>V_{SW}[Note]
H: 5 V
L: 0 V</td><td>⑫ and ⑬ pins are outputs of AGC amplifier. These pins can be selected by V_{SW} voltage to ⑪ pin.

<table><tr><td colspan="2"></td><td>AGC out pin</td></tr><tr><td colspan="2"></td><td>out</td><td>Pin No.</td></tr><tr><td rowspan="2">V_{SW} ⑪</td><td>H: 5 V</td><td>out 1</td><td>⑬</td></tr><tr><td>L: Open or GND</td><td>out 2</td><td>⑫</td></tr></table>
Both ⑫ and ⑬ output with 50 Ω impedance constant.</td><td rowspan="2">  </td></tr>
<tr><td>12</td><td>AGC OUTPUT 2</td><td>2.2</td></tr>
<tr><td>13</td><td>AGC OUTPUT 1</td><td>2.2</td></tr>
<tr><td>14</td><td>AGC out level control</td><td>(open: 2.0)
0 to 5.0[Note]</td><td>Auto gain control pin.
This pin's bias govern the AGC out level.</td><td>  </td></tr>
<tr><td>15</td><td>V_{CC}</td><td>5.0 ± 0.5[Note]</td><td>Supply voltage pin for AGC amplifier.
Must be conneced bypass capacitor (example: 1 000 pF) to minimize ground impedance.</td><td></td></tr>
<tr><td>16</td><td>AGC INPUT 2 (bypass)</td><td>2.0</td><td>Bypass pin of AGC amplifier input. Must be grounded through capacitor.</td><td rowspan="2">  </td></tr>
<tr><td>17</td><td>AGC INPUT 1</td><td>2.0</td><td>Input of AGC amplifier.
Must be coupled with capacitor to cut DC. (example: 1 000 pF)</td></tr>
<tr><td>18</td><td>GND</td><td>0[Note]</td><td>Ground pin of AGC amplifier.
Must be connected to the system ground with minimum inductance. Ground pattern should be formed as wide as possible. (Track length be kept as short as possible.)</td><td></td></tr>
<tr><td>19</td><td>IF OUTPUT</td><td>2.0</td><td>Output from IF amplifier of down-converter. This amplifier is designed as single-end push-pull amplifier. This pin is assigned for the emitter follower output whit 50 Ω impedance.</td><td>  </td></tr>
<tr><td>20</td><td>V_{CC}</td><td>5.0 ± 0.5[Note]</td><td>Supply voltage pin for down-converter.
Operates on 5.0 ± 0.5 V.
Must be connected bypass capacitor (example: 1 000 pF) to minimize ground impedance.</td><td></td></tr>
</table>

Note Externally supply voltage

★ ABSOLUTE MAXIMUM RATINGS

Parameters	Symbol	Conditions	Ratings	Unit
Supply Voltage	V_{CC}	T_A = + 25°C, pin 9, 15 and 20	6.0	V
AGC Control Voltage	V_{AGC}	T_A = + 25°C, pin 14	5.5	V
SW Control Voltage	V_{SW}	T_A = + 25°C, pin 11	5.5	V
Power Dissipation	P_D	T_A = + 85°C **Note**	650	mW
Operating Ambient Temperature	T_A		–20 to +85	°C
Storage Temperature	T_{stg}		–55 to +150	°C

Note Mounted on 50 × 50 × 1.6-mm epoxy glass PWB, with copper patterning on both sides.

RECOMMENDED OPERATING RANGE

Parameters	Symbol	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
AGC Control Voltage	V_{AGC}	0	–	5.0	V
SW Control Voltage	V_{SW}	0	–	5.0	V
Operating Ambient Temperature	T_A	–20	+25	+85	°C

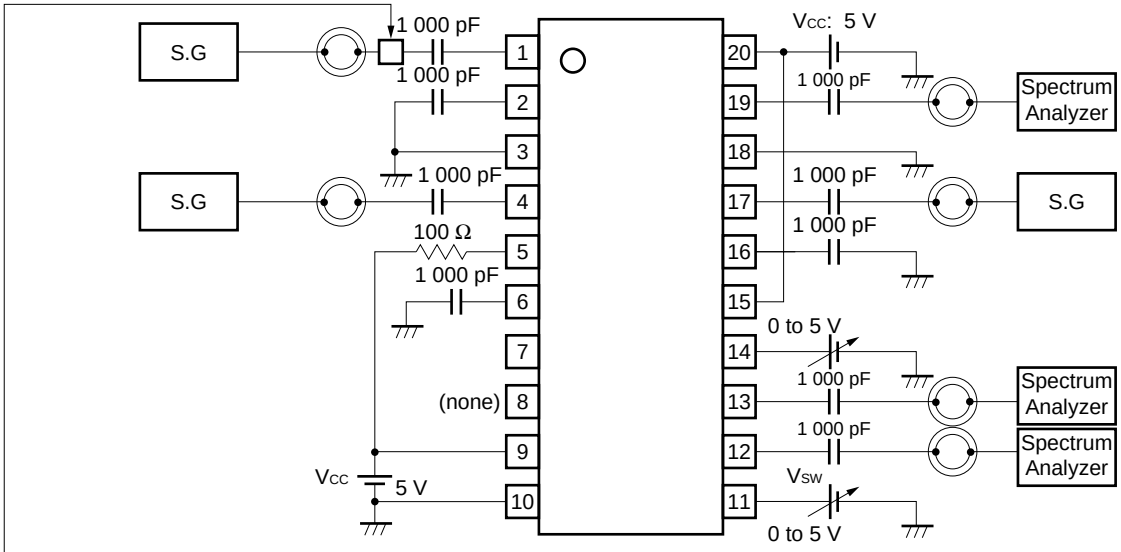
ELECTRICAL CHARACTERISTICS (T_A = + 25°C, V_{CC} = 5.0 V, Z_L = Z_S = 50 Ω)

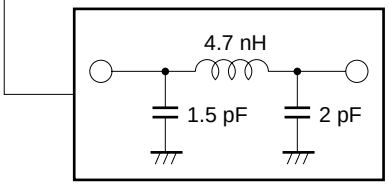
Parameters		Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Circuit Current	Down-converter	Icc	No Input Signal	28.7	42.0	54.0	mA
	AGC Amplifier			15.3	27	38	
	IC Total			44	69	92	
Down-converter Block: unless otherwise specified, f_{IF} = 403 MHz							
Lower RF Input Frequency		f_{RFl}	P_{in} = – 30 dBm	–	–	0.9	GHz
Upper RF Input Frequency		f_{RFu}	P_{in} = – 30 dBm	2.0	–	–	GHz
Conversion Gain 1		CG1	f_{RF} = 900 MHz	11.5	14.5	17.5	dB
Conversion Gain 2		CG2	f_{RF} = 2 GHz	10.5	13.5	16.5	dB
IF Maximum Output Power		$P_{O(SAT)}$	f_{RF} = 2 GHz	0	+7	+10	dBm
Noise Figure 1		NF1	f_{RF} = 900 MHz	–	12	15	dB
Noise Figure 2		NF2	f_{RF} = 2 GHz	–	17	20	dB
AGC Amplifier Block: unless otherwise specified, f_{IF} = 403 MHz							
Lower AGC Input Frequency		f_{IFl}	3 dB down CG from f_{IF} = 403 MHz	–	–	140	MHz
Upper AGC Input Frequency		f_{IFu}	3 dB down CG from f_{IF} = 403 MHz	550	–	–	MHz
Conversion Gain 1		$G_{PMAX.}$	P_{in} = –60 dBm	–	25	–	dB
Conversion Gain 2		$G_{PMIN.}$	P_{in} = –10 dBm	–	–40	–	dB
Gain Control Range		GC	V_{AGC} = 0 to 5.0 V, P_{in} = –30 dBm	45	65	–	dB

STANDARD CHARACTERISTIC FOR REFERENCE (T_A = +25°C, V_{CC} = 5.0 V, Z_L = Z_S = 50 Ω)

Parameters	Symbol	Conditions	Reference Values			Unit
			MIN.	TYP.	MAX.	
Down-converter Block: unless otherwise specified, f_{IF} = 403 MHz						
3rd Order Intermodulation Distortion	IM_3	f_{RF} = 2.0 GHz, 2.04 GHz P_{in} = –20 dBm	–	–39	–	dBc
Local Oscillator Frequency	f_{LO}	Internal local oscillating	1.3	–	2.4	GHz
Noise Figure 2'	NF2'	Internal local oscillating f_{RF} = 2 GHz	–	14	–	dB
AGC Amplifier Block: unless otherwise specified, f_{IF} = 403 MHz						
Input Dynamic Range	D_{range}	Range kept Po = –30 ± 1 dB (V_{AGC} variable)	–	60	–	dB
3rd Order Intermodulation Distortion	IM_3	f_{IFin} = 400 MHz, 420 MHz V_{AGC} = 0 V, Po = –20 dBm	–	–50	–	dBc
SW Control Voltage	V_{SW}	AGC_{OUT1}	4	5	6	V
		AGC_{OUT2}	0	0	1	V

TEST CIRCUIT

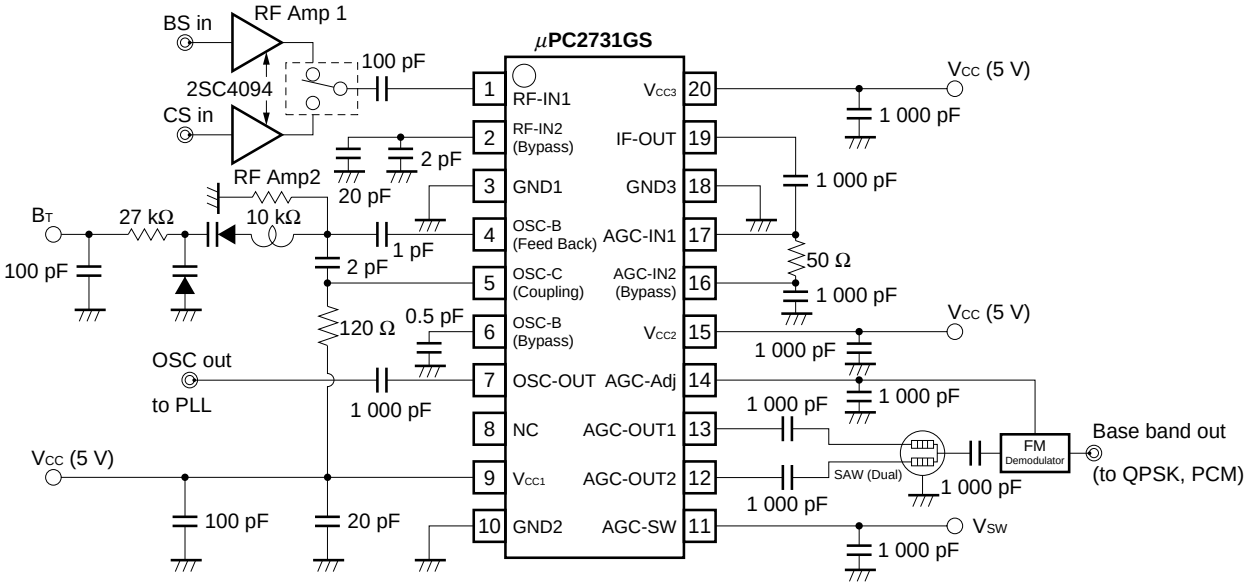




Matching circuit

		AGC out pin	
		Output	Pin No.
V_{SW} 11 pin	H: 5 V	output 1	13
	L: Open or 0 V	output 2	12

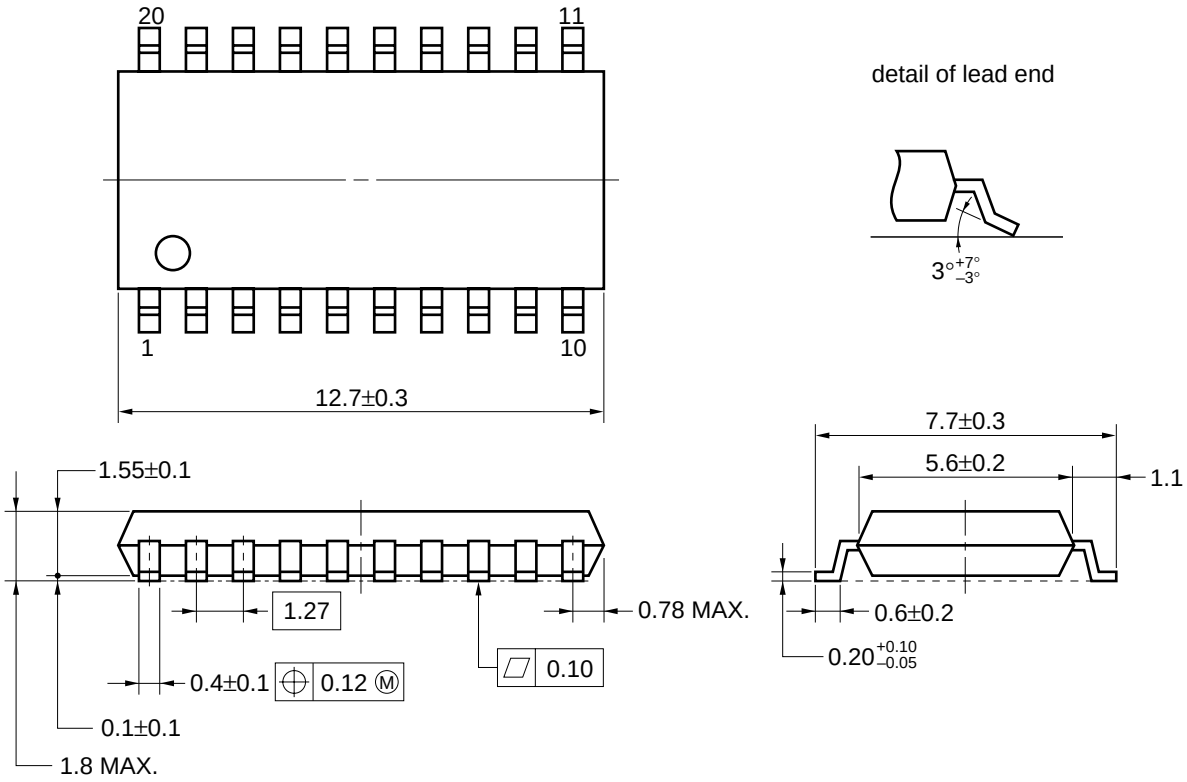
APPLICATION CIRCUIT EXAMPLE



The application circuits and their parameters are for reference only and are not intended for use in actual design-ins.

★ **PACKAGE DIMENSIONS**

20 PIN PLASTIC SOP (7.62 mm (300)) (UNIT: mm)



NOTE Each lead centerline is located within 0.12 mm of its true position (T.P.) at maximum material condition.

NOTE ON CORRECT USE

(1) Observe precautions for handling because of electrostatic sensitive devices.
(2) Form a ground pattern as wide as possible to minimize ground impedance (to prevent undesired oscillation).
(3) Keep the track length of the ground pins as short as possible.
(4) Connect a bypass capacitor (example: 1 000 pF) to the V_{CC} pin.

RECOMMENDED SOLDERING CONDITIONS

This product should be soldered under the following recommended conditions. For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared Reflow	Package peak temperature: 235°C or below Time: 30 seconds or less (at 210°C) Count: 3, Exposure limit: None[Note]	IR35-00-3
VPS	Package peak temperature: 215°C or below Time: 40 seconds or less (at 200°C) Count: 3, Exposure limit: None[Note]	VP15-00-3
Wave Soldering	Soldering bath temperature: 260°C or below Time: 10 seconds or less Count: 1, Exposure limit: None[Note]	WS60-00-1
Partial Heating	Pin temperature: 300°C Time: 3 seconds or less (per side of device) Exposure limit: None[Note]	–

Note After opening the dry pack, keep it in a place below 25°C and 65% RH for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

For details of recommended soldering conditions for surface mounting, refer to information document SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL (C10535E).

[MEMO]

ATTENTION

OBSERVE PRECAUTIONS
FOR HANDLING
ELECTROSTATIC
SENSITIVE
DEVICES

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  - Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots
  - Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
  - Specific: Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

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