

# MOS INTEGRATED CIRCUIT

# $\mu$ PD16435, 16435A

## DOT MATRIX LCD CONTROLLER/DRIVER

### DESCRIPTION

The  $\mu$ PD16435 and 16435A are controllers/drivers for a  $119 \times 73$ -dot LCD, and perform LCD full-dot and character composite display by means of control by a microprocessor that has a 4 or 8-bit data bus. A charge pump type DC/DC converter is also incorporated, enabling 3 or 5 V single power supply drive.

The  $\mu$ PD16435 uses an external reference clock. The  $\mu$ PD16435A has the on-chip oscillation circuit (external crystal resonator).

### FEATURES

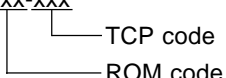
- Can interface to 4 or 8-bit CPU.
- Incorporates 119 segment outputs and 73 common outputs.  
(Display duty selectable from 1/35, 1/37, 1/71, 1/73)
- $5 \times 7$  character font 208 character data configuration character generation ROM and 16 character data configuration character generation RAM, allowing composite full-dot and character display
- Incorporates extended display functions such as magnification, lateral scrolling, blink, reverse, etc.
- Operating voltage: 2.7 V to 5.5 V
- On-chip DC/DC converter: Selectable between  $\times 4$  set-up circuit and  $\times 2$  step-up circuit
- On-chip temperature correction circuit
- Master/slave operation capability
- On-chip power-on reset circuit
- On-chip oscillation circuit ( $\mu$ PD16435A)
- 232-pin TCP (Tape Carried Package)

### ORDERING INFORMATION

Part Number	Package
$\mu$ PD16435N-001-xxx	TCP (TAB), Standard ROM code
$\mu$ PD16435N-001-001	Standard quad TCP (Conforms to EIAJ), Standard ROM code
$\mu$ PD16435N-001-002	Standard dual TCP (Output OLB: 0.25 mm pitch), Standard ROM code
$\mu$ PD16435AN-001-xxx	TCP (TAB), Standard ROM code
$\mu$ PD16435AN-001-001	Standard quad TCP (Conforms to EIAJ), Standard ROM code
$\mu$ PD16435AN-001-052	Standard dual TCP (Output OLB: 0.25 mm pitch), Standard ROM code

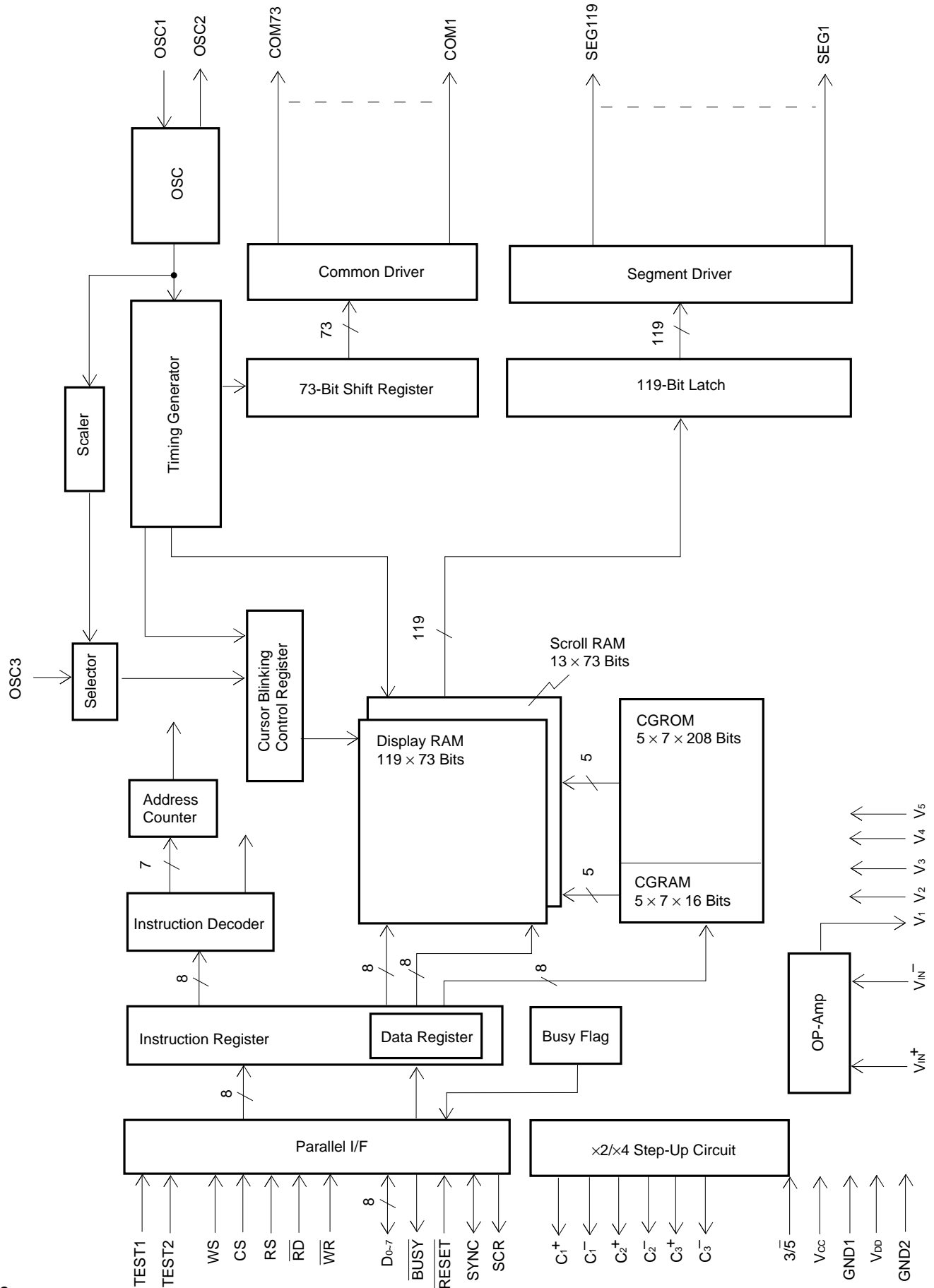
### Explanation of Part Number

$\mu$ PD16435 (A) N-xxx-xxx

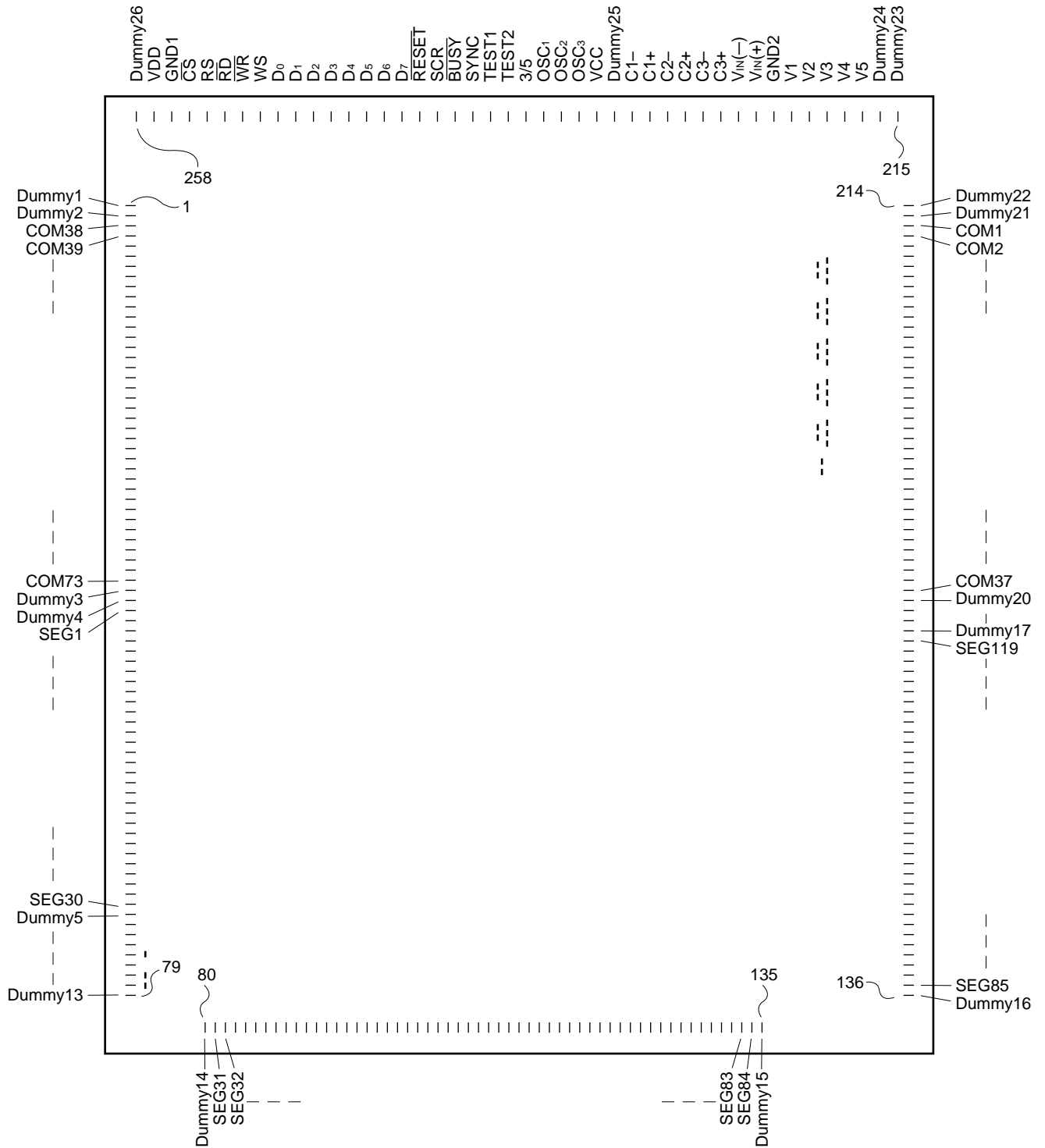


The TCP model is a custom model. For details, consult NEC sales representative.

BLOCK DIAGRAM



PIN CONFIGURATION (CHIP)



**PIN DESCRIPTIONS**

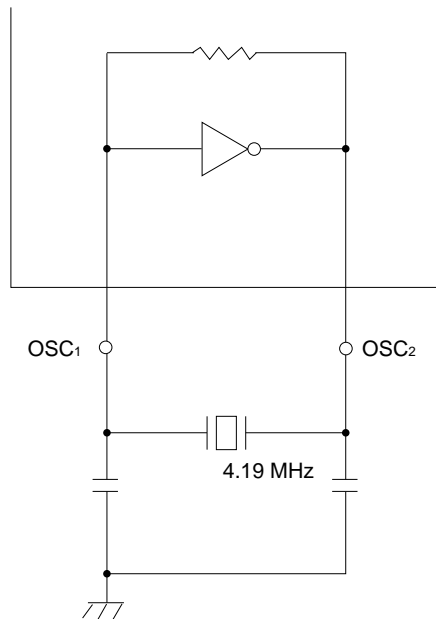
Pin Name	Pin No.	Input/Output	Output Type	Description
$\overline{CS}$	255	Input	—	Chip select signal
RS	254	Input	—	Register selection signal (specifies address register when “0”, control register when “1”).
$\overline{RD}$	253	Input (Schmitt)	—	Read enable signal. Reads write address when scrolling. Active edge is falling edge.
$\overline{WR}$	252	Input (Schmitt)	—	Write enable signal. Active edge is falling edge.
WS	251	Input	—	Word length selection signal (4-bit input when “1”, 8-bit input when “0”).
D <sub>0</sub> to D <sub>7</sub>	250 to 243	Input/output	CMOS 3-state	Transmit/receive data (3-state bidirectional) Upper → D4 to D7 Lower → D0 to D3 (These pins should be set as unused in case of 4-bit data). In test mode, these pins are output pins. In a 4-bit transfer, storage is performed in the upper (MSB) in order from the data transferred first.
$\overline{BUSY}$	240	Output	Nch open-drain	“0” indicates busy state.
$\overline{RESET}$	242	Input	—	“0” → Initialization of all internal registers and commands is performed. Output is fixed at V <sub>1</sub> .
SCR	241	Output	CMOS	Signal is output to CPU on completion of one-character scroll.
SYNC	239	Input/output	Nch open-drain	Synchronization signal input/output pins for master/slave operation.
OSC <sub>1</sub> OSC <sub>2</sub>	235 234	—	—	μPD16435: Input the 4.19 MHz reference clock to the OSC <sub>1</sub> pin externally. Leave the OSC <sub>2</sub> pin open. (Always outputs high level.) μPD16435A: This is the pin to which the 4.19 MHz crystal resonator is connected. Input the external clock to OSC <sub>1</sub> first.
OSC <sub>3</sub>	233	Input (Schmitt)	—	2 Hz external clock input pin. Scaled by 2 internally to generate 1 Hz, used as blink synchronization signal.
COM1 to COM73	212 to 176 3 to 38	Output	Analog switch	Common output signals
SEG1 to SEG119	41 to 70 81 to 134 137 to 171	Output	Analog switch	Segment output signals
TEST1 TEST2	238 237	Output	—	“1” → Test mode “0” or open → Normal operating mode

Pin Name	Pin No.	Input/Output	Output Type	Description
V1	221	Output	—	LCD drive power supply pin Internal OP-amp output
V2 to V5	220 to 217	Input	—	LCD drive power supply pins Can be adjusted by addition of external resistor.
V <sub>IN(-)</sub> V <sub>IN(+)</sub>	224 223	Input	—	Liquid crystal drive power supply OP-amp input pins
V <sub>CC</sub> , GND1	232, 256	—	—	Logic power supply, GND
V <sub>DD</sub> , GND2	257, 222	—	—	Liquid crystal drive (step-up) power supply, GND
3/5	236	Input	—	Drive voltage selection pin "1" → V <sub>DD</sub> = 3 V (×4 step-up circuit selected) "0" → V <sub>DD</sub> = 5 V (×2 step-up circuit selected)
C1±, C2±, C3±	230 to 225	—	—	A 1 $\mu$ F tantalum or ceramic capacitor should be connected externally.

**REFERENCE CLOCK**

Product Name	Reference Clock
$\mu$ PD16435	External input
$\mu$ PD16435A	On-chip oscillation circuit (External crystal resonator)

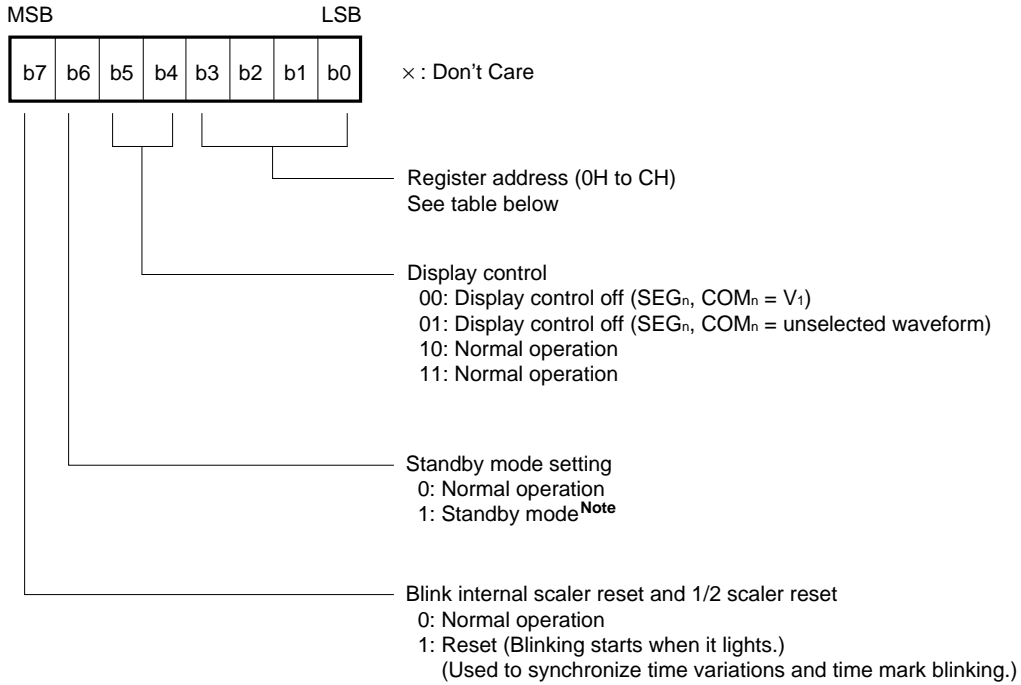
**OSC CIRCUIT ( $\mu$ PD16435A)**



**REGISTER FUNCTIONS**

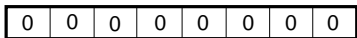
**(1) Address Register**

Sets the address of each register, and also sets display control, standby mode, and scaler resetting.



**Note** Standby mode = { DC/DC converter stopped  
OSC<sub>1</sub> input invalid (μPD16435)  
OSC stopped (μPD16435A)  
SEG<sub>n</sub>, COM<sub>n</sub> = V<sub>1</sub>  
Data write/read prohibited

After powering on

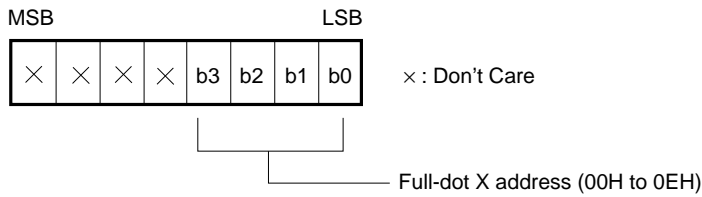


**Register address list**

Address				Register Name
b3	b2	b1	b0	
0	0	0	0	Full-dot X address register
0	0	0	1	Full-dot Y address register
0	0	1	0	Full-dot data register
0	0	1	1	Character X address register
0	1	0	0	Character Y address register
0	1	0	1	Character data register
0	1	1	0	CGRAM address register
0	1	1	1	CGRAM data register
1	0	0	0	Extension register
1	0	0	1	Extension register X address register
1	0	1	0	Extension register Y address register
1	0	1	1	Scroll register
1	1	0	0	Control register

**(2) Full-Dot X Address Register (Register Address = 0000B)**

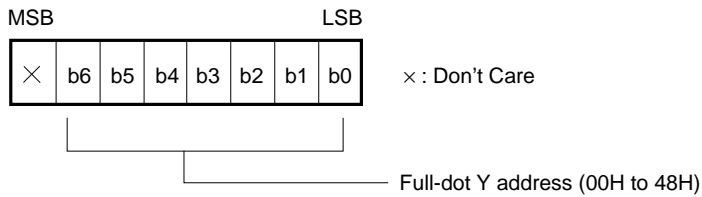
Performs full-dot display, display screen X (segment) direction address setting. As scrolling is not possible with a full-dot display, addresses are not allocated to the scroll RAM area.



After powering on: Undefined

**(3) Full-Dot Y Address Register (Register Address = 0001B)**

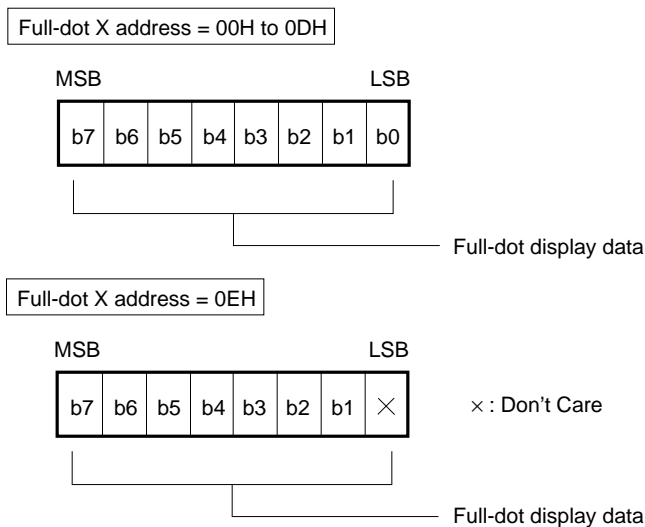
Performs full-dot display, display screen Y (common) direction address setting.



After powering on: Undefined

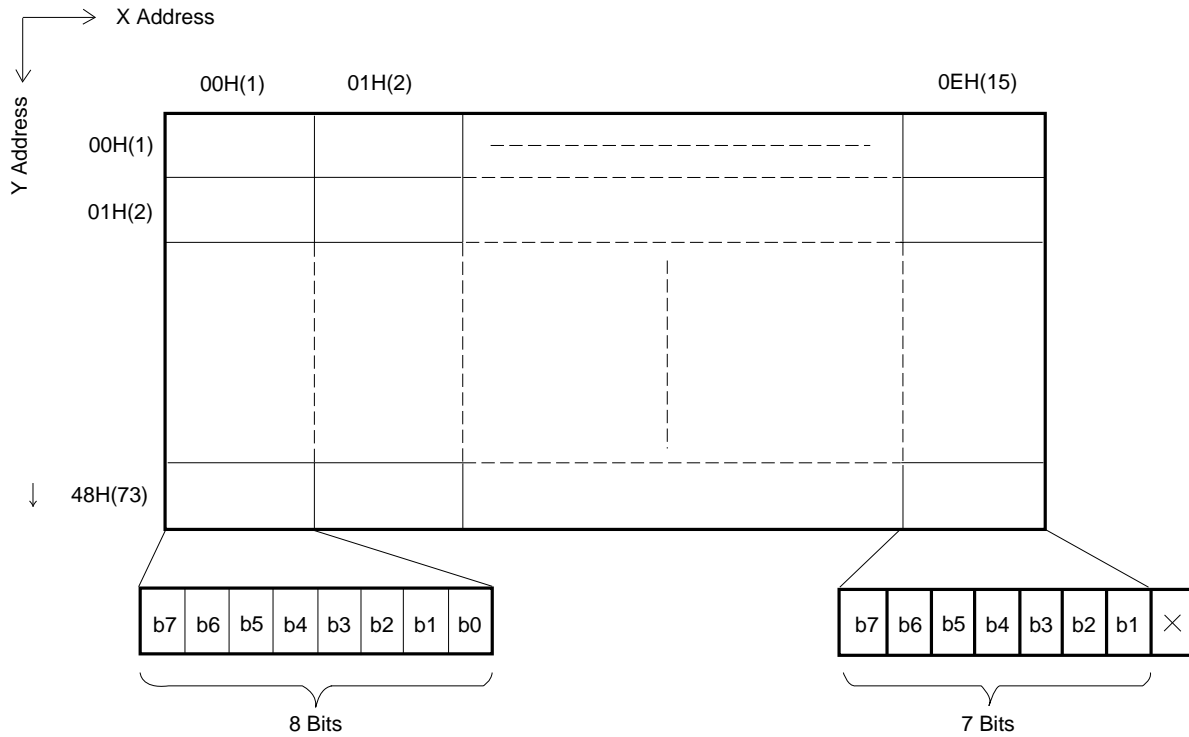
**(4) Full-Dot Data Register (Register Address = 0010B)**

Inputs full-dot display data. Display data is stored in the display memory with the MSB on the left, and display data "1" corresponds to illumination.



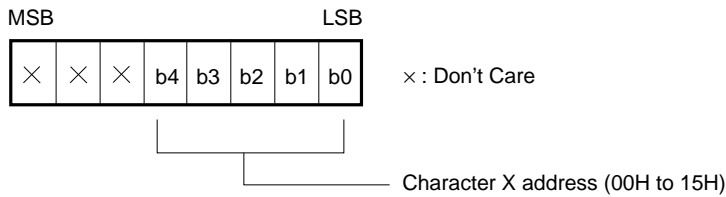
After powering on: Undefined

Full-Dot X Address and Y Address Allocation



(5) Character X Address Register (Register Address = 0011B)

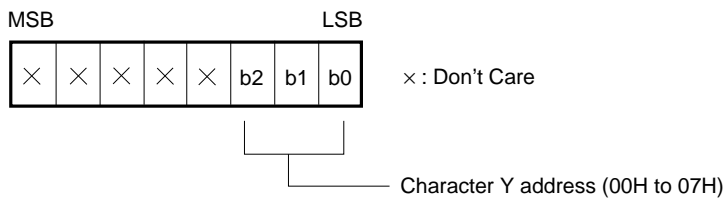
Performs character display display, screen X (segment) direction address setting. X addresses include the scroll RAM area.



After powering on: Undefined

(6) Character Y Address Register (Register Address = 0100B)

Performs character display display, screen Y (common) direction address setting.

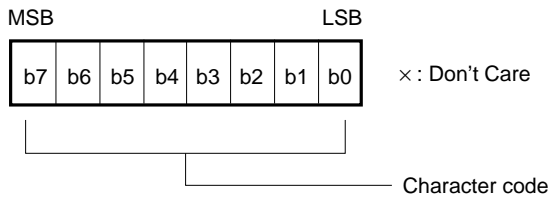


After powering on: Undefined



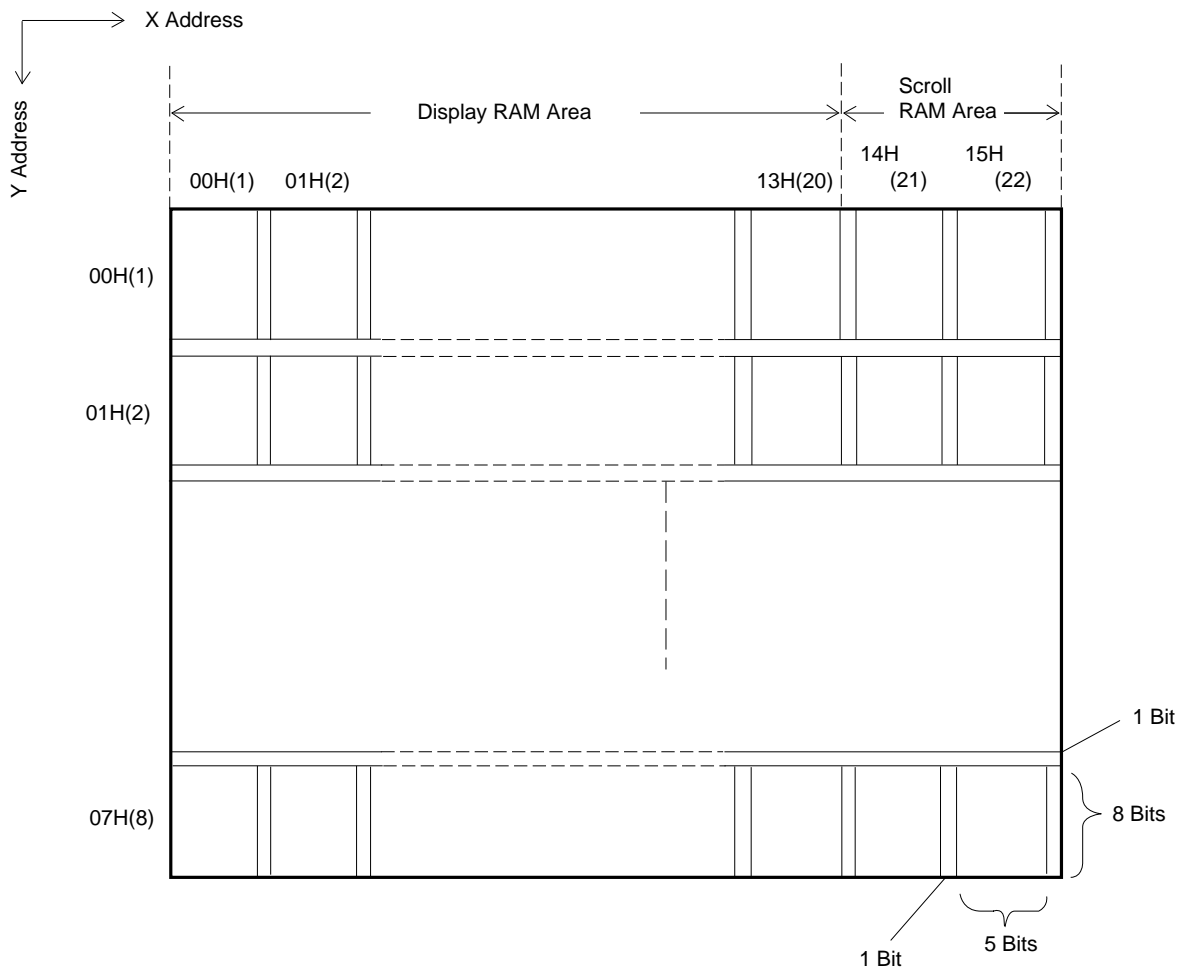
**(7) Character Data Register (Register Address = 0101B)**

The character indicated in the character code table is displayed at the position indicated by the character X and Y address registers.



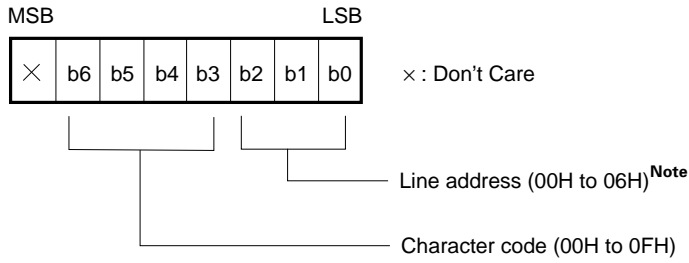
After powering on: Undefined

**Character X Address and Y Address Allocation**



**(8) CGRAM Address Register (Register Address = 0110B)**

Performs address setting when display data is written to CGRAM. Bits b6 to b3 of the CGRAM address indicate the character code, and bits b2 to b0 indicate the character line.



**Note** If auto increment is set with the control register, 06H is followed by 07H. Dummy data should be sent when the address is 07H.

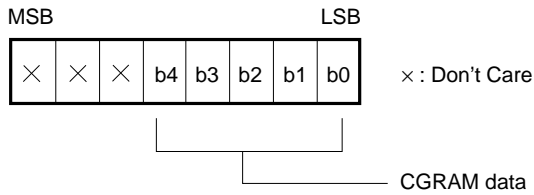
Example: (CGRAM address with auto increment)

--- → 15H → 16H → 17H → 18H → ---

After powering on: Underfined

**(9) CGRAM Data Register (Register Address = 0111B)**

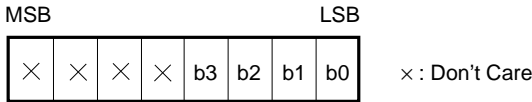
CGRAM display data. The lower 5 bits of the write data are valid.



After powering on: Undefined

**(10) Extension Register (Register Address = 1000B)**

Performs magnification, reverse, cursor, and time mark setting.



**In case of magnification setting**

- 00: Standard
- 01: ×2 horizontal
- 10: ×2 vertical
- 11: ×4 magnification (×2 horizontal & vertical)

Magnification display is performed at any line position; characters of different sizes cannot be displayed on the same line. Line specification magnification display is possible by setting an extension Y address after this command, and multiple-line magnification display is possible by setting consecutive extension Y address.

**In case of reverse setting**

- 00: Reverse cancellation (line specification)
- 01: Reverse (line specification)
- 10: Reverse cancellation (full screen)
- 11: Reverse (full screen)

Line specification reverse display is possible by setting an extension Y address after this command, and multiple-line reverse display is possible by setting consecutive extension Y addresses. Regarding the reverse display Y address direction, a total of 9 dots (7 character part dots + 1 cursor part dot + 1 top space dot) are reversed. In the case of ×2 vertical magnification or ×4 magnification, a total of 18 dots (14 character part dots + 2 cursor part dots + 2 top space dots) are reversed.

**In case of cursor setting**

- 00: Cursor non-display
- 01: Cursor display (blinking stopped)
- 10: Cursor display (blink operation)
- 11: Don't Care

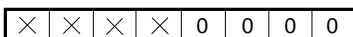
Blinking display can be performed at any address by specifying an extension X and Y address after this command. The specification is for one address only. The address specification should be performed in the order: X address → Y address.

**In case of character blink setting**

X0: Blinking stopped  
X1: Blink operation  
Blinking can be performed at any address by specifying an extension X and Y address after this command. The specification is for one address only. The address specification should be performed in the order: X address → Y address.

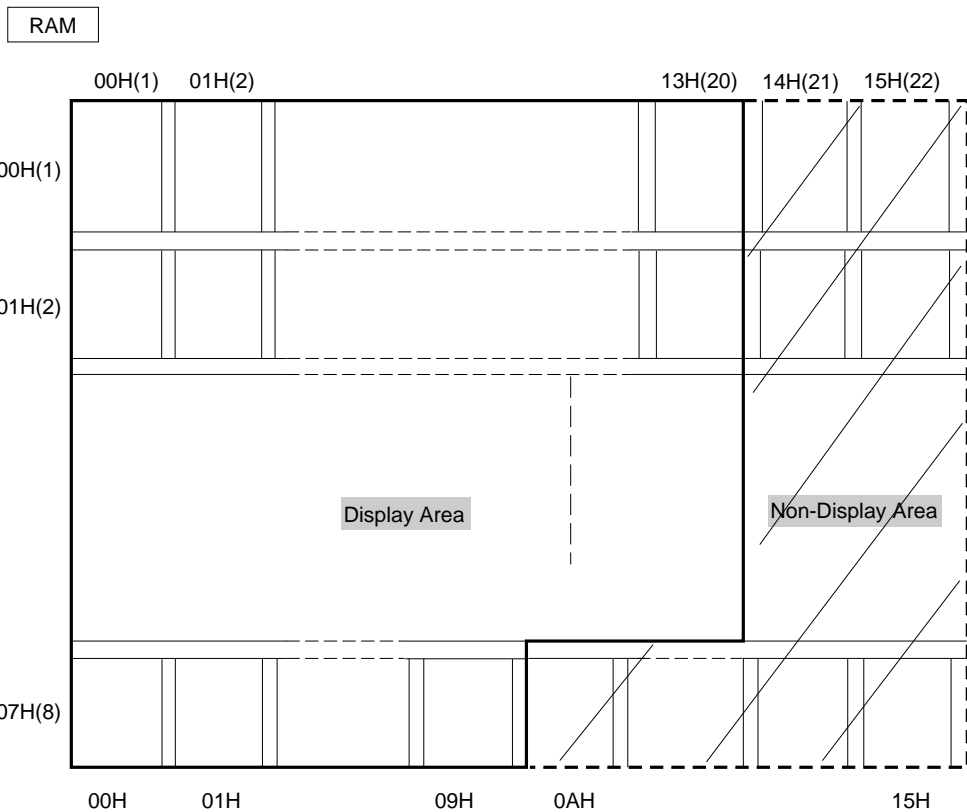
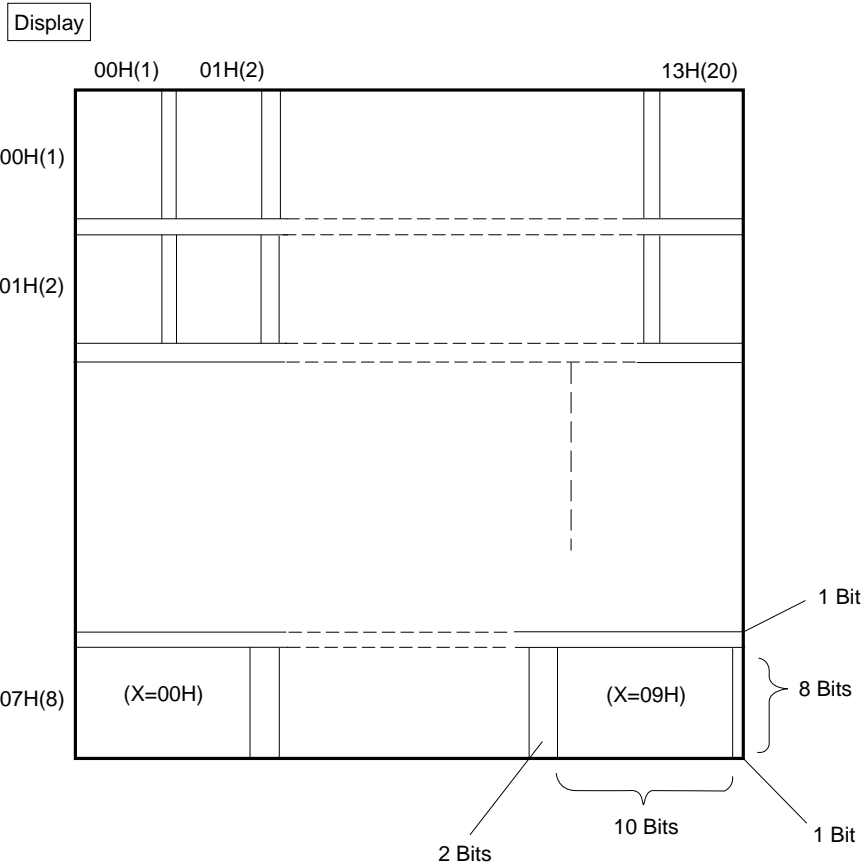
- Extension function setting
- 00: Magnification setting
  - 01: Reverse setting
  - 10: Cursor setting
  - 11: Character blink setting

After powering on



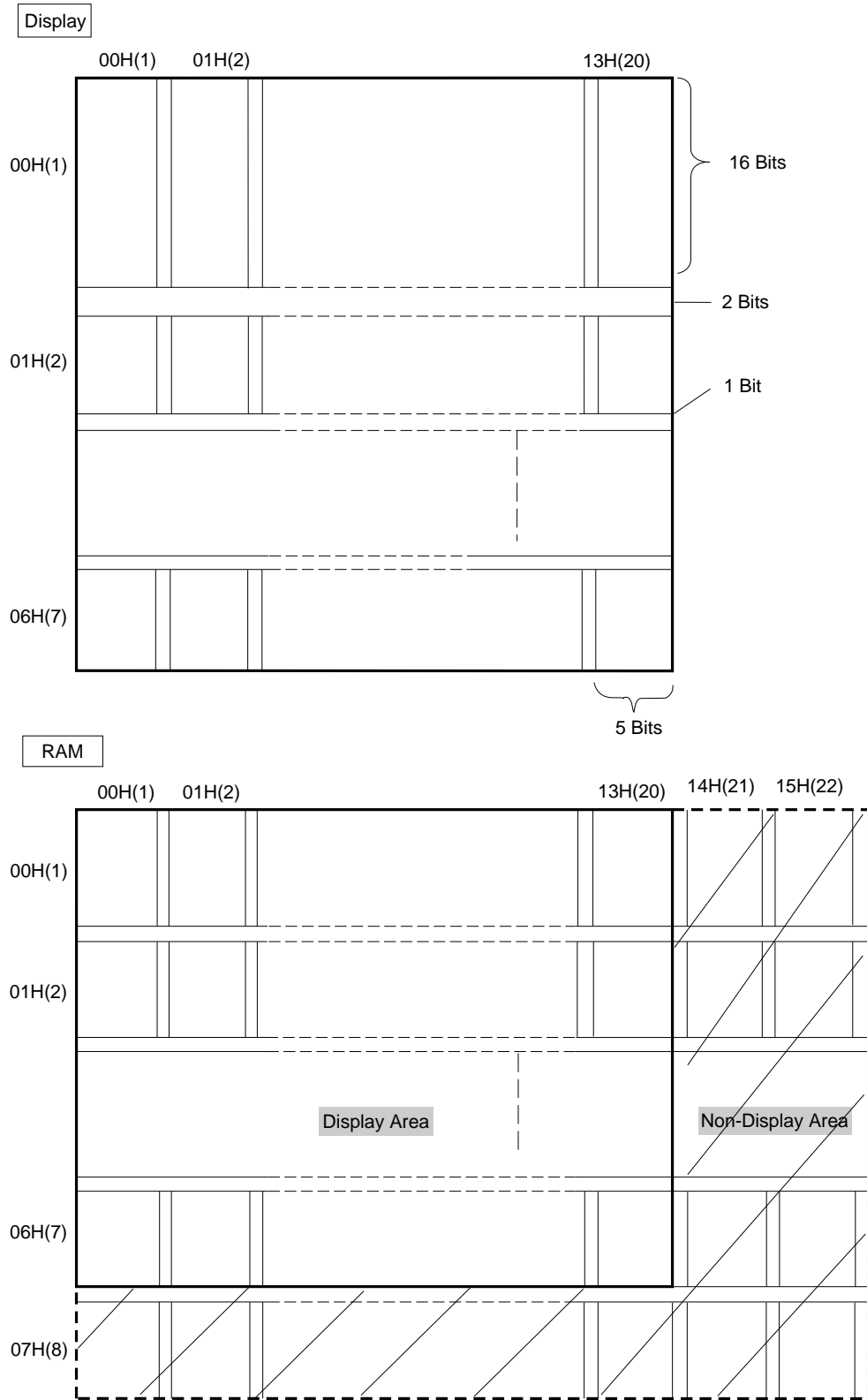
Display and RAM Allocation in Case of Magnification Setting

(1) Example of ×2 horizontal magnification (line 07H specified)



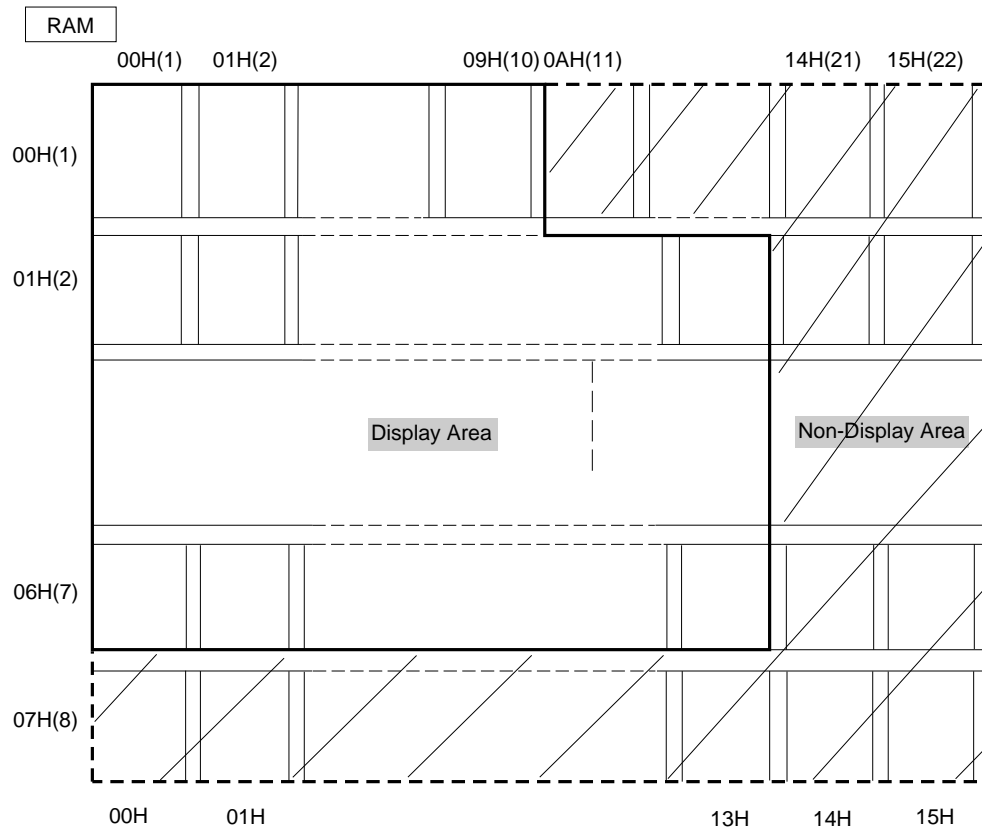
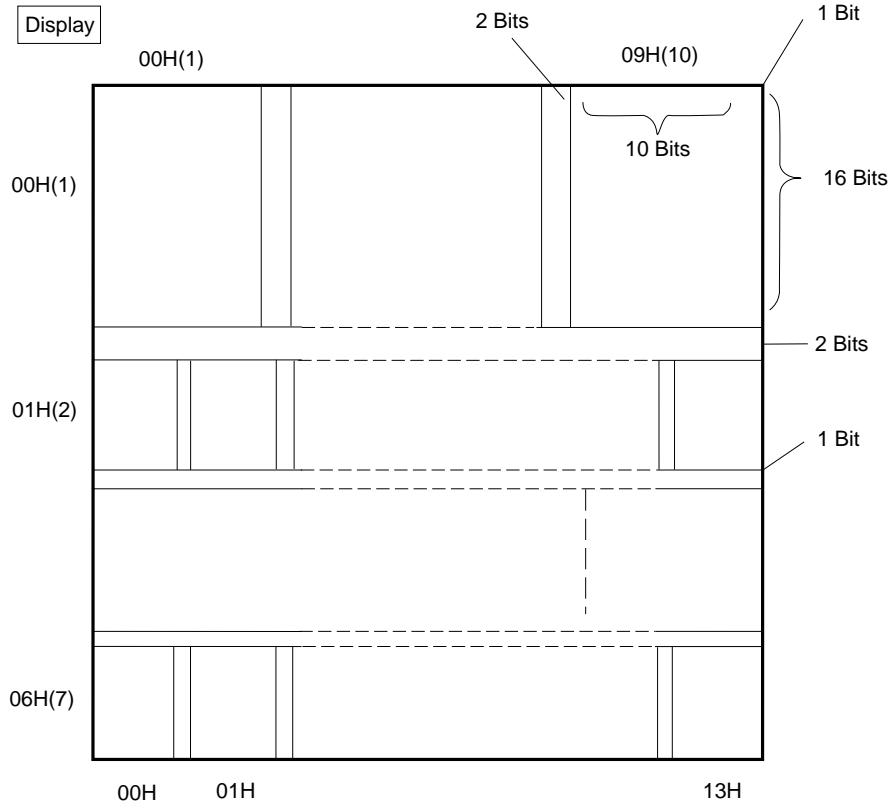
**Note** Lines 0AH to 15H for which ×2 horizontal magnification is specified can be used as scroll RAM.

(2) Example of ×2 vertical magnification (line 00H specified)



**Note** If ×2 vertical magnification is specified for line 07H, the lower half will be outside the display area. Also, if ×2 vertical magnification is specified for line 06H, the bottom dot will be a space.

(3) Example of ×4 magnification (line 00H specified)

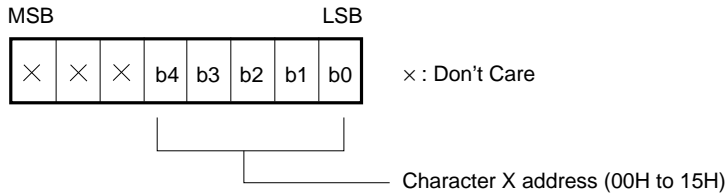


**Note** Lines 0AH to 15H for which ×4 magnification is specified can be used as scroll RAM.

If ×4 magnification is specified for line 07H, the lower half will be outside the display area, and if ×4 magnification is specified for line 06H, the bottom dot will be a space.

**(11) Extension X Address Register (Register Address = 1001B)**

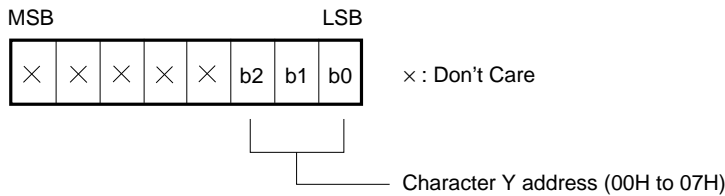
Performs extension display, display screen X (segment) direction address setting. X addresses include the scroll RAM area. This register must be executed before the extension Y address register.



After powering on: Undefined

**(12) Extension Y Address Register (Register Address = 1010B)**

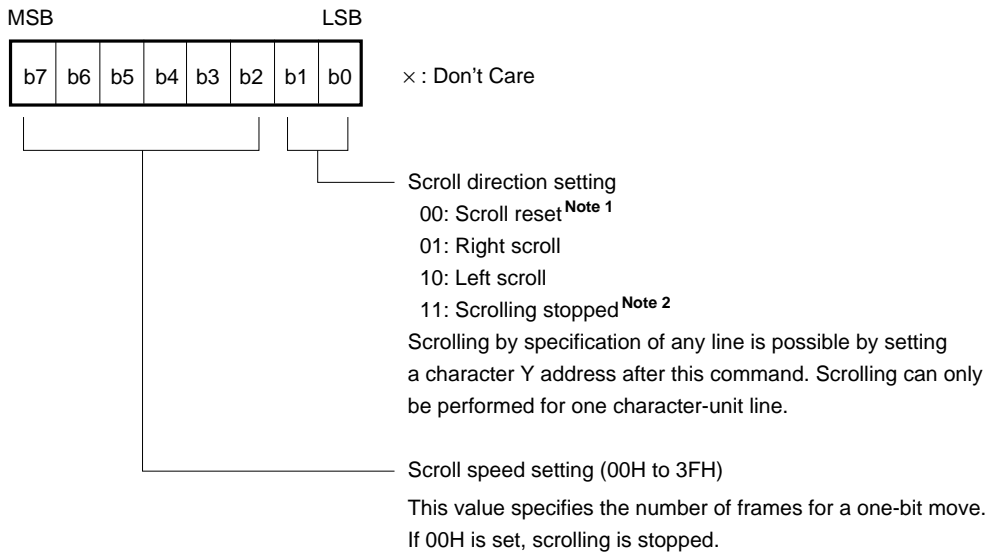
Performs extension display, display screen Y (common) direction address setting. This register must be executed after the X address.



After powering on: Undefined

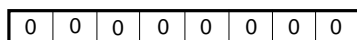
**(13) Scroll Register (Register Address = 1011B)**

Performs scroll setting.



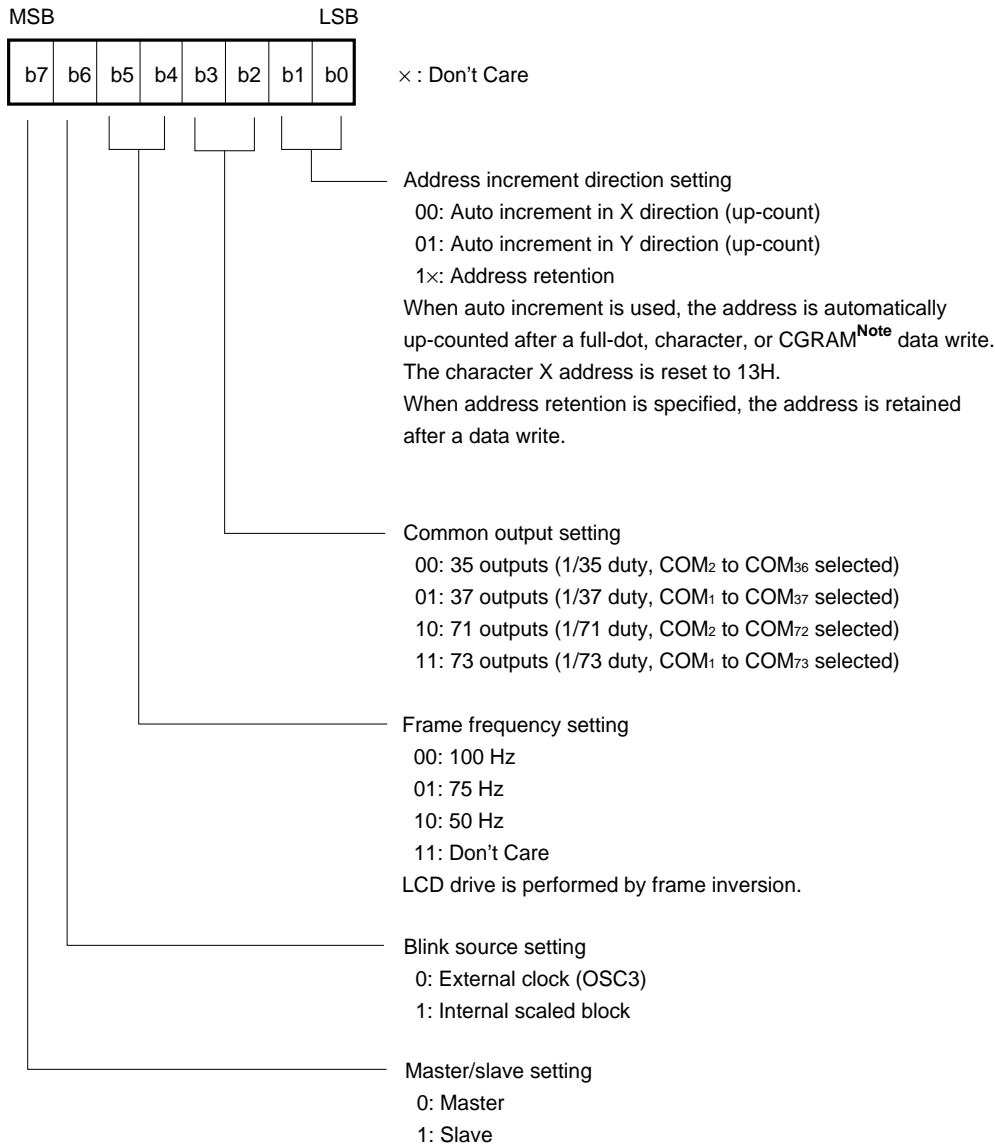
- Notes 1.** When scroll reset is executed, the screen leftmost character X address returns to 00H, and scrolling is stopped.
- 2.** After scrolling has been stopped, character Y address setting is necessary when scrolling is restarted. It is not possible to set a different address from the character Y address before scrolling was stopped.

After powering on



**(14) Control Register (Register Address = 1100B)**

Performs address increment direction, common output, frame frequency, blinking, and master/slave setting.



**Note** CGRAM is incremented in the Y direction even if 00H is set.

After powering on

0	0	0	0	0	0	0	0	0	0
---	---	---	---	---	---	---	---	---	---



Standard ROM Code (001)

Higher Bit Lower 4 Bits Bit 4 Bits	0000	0001	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
xxxx0000	CC RAM (1)													
xxxx0001	(2)													
xxxx0010	(3)													
xxxx0011	(4)													
xxxx0100	(5)													
xxxx0101	(6)													
xxxx0110	(7)													
xxxx0111	(8)													
xxxx1000	(9)													
xxxx1001	(10)													
xxxx1010	(11)													
xxxx1011	(12)													
xxxx1100	(13)													
xxxx1101	(14)													
xxxx1110	(15)													
xxxx1111	(16)													

**ABSOLUTE MAXIMUM RATINGS** ( $T_A = 25\text{ }^\circ\text{C}$ ,  $\text{GND1} = \text{GND2} = 0\text{ V}$ )

Parameter	Symbol	Rating	Unit
Supply voltage 1 ( $3/\bar{5} = \text{L}$ )	$V_{CC1}$	-0.3 to +7.0	V
Supply voltage 2 ( $3/\bar{5} = \text{H}$ )	$V_{CC2}$	-0.3 to +4.0	V
Logic input voltage	$V_{IN}$	-0.3 to $V_{CC}+0.3$	V
Logic output voltage	$V_{OUT1}$	-0.3 to $V_{CC}+0.3$	V
LCD drive power supply voltage	$V_{DD}$	$V_{CC}-0.3$ to +16.0	V
LCD drive power supply input voltage	$V_2$ to $V_5$	-0.3 to $V_{DD}+0.3$	V
LCD drive power supply output voltage	$V_1$	-0.3 to $V_{DD}+0.3$	V
Amplifier input voltage	$V_{IN (+)}$ , $V_{IN (-)}$	-0.3 to $V_{DD}+0.3$	V
Driver output voltage (Segment, common)	$V_{OUT2}$	-0.3 to $V_{DD}+0.3$	V
Storage temperature range	$T_{stg.}$	-55 to +150	$^\circ\text{C}$

**RECOMMENDED OPERATING RANGES**

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage 1 ( $3/\bar{5} = \text{L}$ )	$V_{CC1}$	4.5	5.0	5.5	V
Supply voltage 2 ( $3/\bar{5} = \text{H}$ )	$V_{CC2}$	2.7	3.0	3.6	V
LCD drive supply voltage	$V_{DD}$	$V_{CC}$	8.0	14.5	V
Logic input voltage	$V_{IN}$	0		$V_{CC}$	V
LCD drive power supply input voltage	$V_2$ to $V_5$	0		$V_{DD}$	V
LCD drive power supply output voltage	$V_1$	0		$V_{DD}$	V
External capacitance	$C_0$ to $C_3$	1		4.7	$\mu\text{F}$
Operating temperature range	$T_A$	-40		+85	$^\circ\text{C}$

**ELECTRICAL SPECIFICATIONS** (Unless specified otherwise,  $T_A = -40$  to  $+85$  °C,  $C_0$  to  $C_3 = 1$  μF,  $V_{CC} = 5$  V  $\pm 10\%$  :  $\overline{3/5} = L$  or  $V_{CC} = 2.7$  V to  $3.6$  V :  $3/5 = H$ )

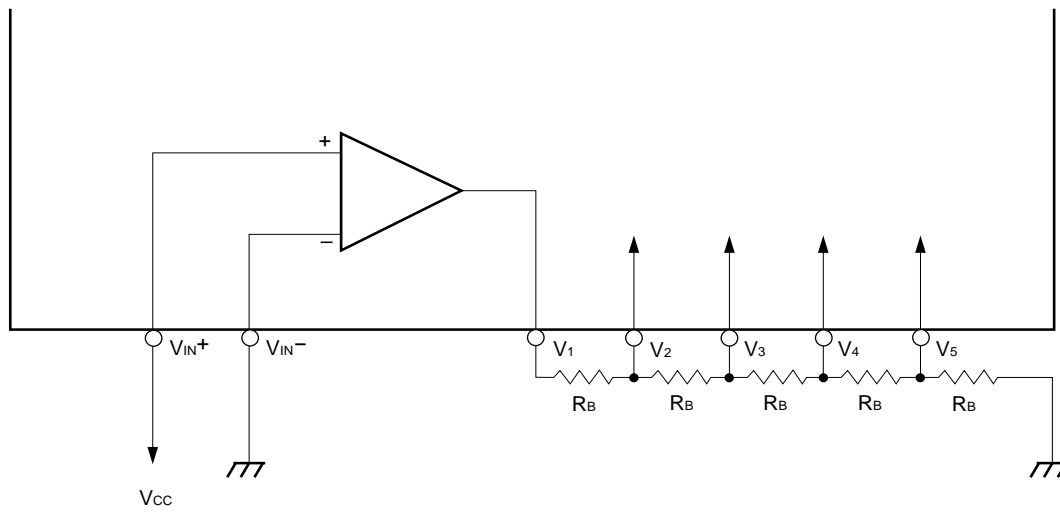
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Input voltage high	$V_{IH1}$	Except Schmitt inputs	$0.7V_{CC}$			V
Input voltage low	$V_{IL1}$	Except Schmitt inputs			$0.3V_{CC}$	V
Input voltage high	$V_{IH2}$	Schmitt inputs	$0.8V_{CC}$			V
Input voltage low	$V_{IL2}$	Schmitt inputs			$0.2V_{CC}$	V
Hysteresis voltage	$V_H$	Schmitt inputs	$0.05V_{CC}$		$0.2V_{CC}$	V
Input current high	$I_{IH1}$	$\overline{CS}$ , RS, $\overline{RD}$ , $\overline{WR}$ , WS, $\overline{RESET}$ , $3/5$ , OSC <sub>3</sub> , $V_{IN(+)}$ , $V_{IN(-)}$ , $V_{IN} = V_{CC}$			1	μA
Input current low	$I_{IH1}$	$\overline{CS}$ , RS, $\overline{RD}$ , $\overline{WR}$ , WS, $\overline{RESET}$ , $3/5$ , OSC <sub>3</sub> , $V_{IN(+)}$ , $V_{IN(-)}$ , $V_{IN} = 0$ V			-1	μA
Input current high	$I_{IH2}$	TEST1, TEST2, $V_{IN} = V_{CC}$			6	mA
Input current low	$I_{IL2}$	TEST1, TEST2, $V_{IN} = 0$ V			-100	μA
Output voltage high	$V_{OH1}$	$D_n$ , SCR, $3/5 = L$ $I_{OH} = -1$ mA	$0.9V_{CC}$			V
Output voltage low	$V_{OL1}$	$D_n$ , BUSY, SCR, SYNC, $3/5 = L$ $I_{OL} = 4$ mA			$0.1V_{CC}$	V
Output voltage high	$V_{OH2}$	$D_n$ , SCK, $3/5 = H$ $I_{OH} = -0.6$ mA	$0.9V_{CC}$			V
Output voltage low	$V_{OL2}$	$D_n$ , BUSY, SCR, SYNC, $3/5 = H$ $I_{OL} = 2.4$ mA			$0.1V_{CC}$	V
Output voltage high	$V_{OH3}$	$V_1$ pin $I_{OH} = -1$ mA $V_{IN(+)} = V_{DD}$ , $V_{IN(-)} = 0$ V	$0.9V_{CC}$			V
Output voltage low	$V_{OL3}$	$V_1$ pin $I_{OL} = -10$ μA $V_{IN(+)} = 0$ V, $V_{IN(-)} = V_{DD}$			$0.1V_{DD}$	V
Leak current high	$I_{LOH}$	$D_n$ , SYNC, BUSY $V_{IN/OUT} = V_{CC}$			10	μA
Leak current low	$I_{LOL}$	$D_n$ , SYNC, BUSY $V_{IN/OUT} = 0$ V			-10	μA
Common output on-resistance	$R_{COM}$	COM <sub>1</sub> to COM <sub>73</sub> $ I_o  = 100$ μA			5	kΩ
Segment output on-resistance	$R_{SEG}$	SEG <sub>1</sub> to SEG <sub>119</sub> $ I_o  = 100$ μA			10	kΩ
Driver unit supply voltage (step-up voltage)	$V_{DD1}$	$R_B = 10$ kΩ $3/5 = L$	$1.9V_{CC}$		$2.0V_{CC}$	V
Driver unit supply voltage (step-up voltage)	$V_{DD2}$	$R_B = 10$ kΩ $3/5 = H$	$3.6V_{CC}$		$4.0V_{CC}$	V

**ELECTRICAL SPECIFICATIONS** (Unless specified otherwise, T<sub>A</sub> = -40 to +85 °C, C0 to C3 = 1 μF, V<sub>CC</sub> = 5 V ±10% : 3/5 = L or V<sub>CC</sub> = 2.7 V to 3.6 V : 3/5 = H)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Logic consumption current (μPD16435)	I <sub>CC1</sub>	V <sub>CC</sub> = 3.0 V, no load, 3/5=H f <sub>OSC</sub> = 4.19 MHz		0.35	1	mA
	I <sub>CC2</sub>	V <sub>CC</sub> = 5.0 V, no load, 3/5=L f <sub>OSC</sub> = 4.19 MHz		0.35	1	mA
	I <sub>CC3</sub>	V <sub>CC</sub> = 3.0 V, 3/5=H R <sub>B</sub> = 10 kΩ <sup>Note</sup> f <sub>OSC</sub> = 4.19 MHz		1.3	2.5	mA
	I <sub>CC4</sub>	V <sub>CC</sub> = 5.0 V, 3/5=L R <sub>B</sub> = 10 kΩ <sup>Note</sup> f <sub>OSC</sub> = 4.19 MHz		0.75	1.5	mA
Logic consumption current (μPD16435A)	I <sub>CC1</sub>	V <sub>CC</sub> = 3.0 V, no load, 3/5=H f <sub>OSC</sub> = 4.19 MHz		0.6	1.5	mA
	I <sub>CC2</sub>	V <sub>CC</sub> = 5.0 V, no load, 3/5=L f <sub>OSC</sub> = 4.19 MHz		0.65	1.5	mA
	I <sub>CC3</sub>	V <sub>CC</sub> = 3.0 V, 3/5=H R <sub>B</sub> = 10 kΩ <sup>Note</sup> f <sub>OSC</sub> = 4.19 MHz		1.5	3	mA
	I <sub>CC4</sub>	V <sub>CC</sub> = 5.0 V, 3/5=L R <sub>B</sub> = 10 kΩ <sup>Note</sup> f <sub>OSC</sub> = 4.19 MHz		1.05	2	mA

**Note** TYP. values are reference values for T<sub>A</sub> = 25 °C.

NOTE MEASUREMENT CIRCUIT



**SWITCHING SPECIFICATIONS** (Unless specified otherwise,  $T_A = -40$  to  $+85$  °C,  $C_0$  to  $C_3 = 1$  μF,  $V_{CC} = 5$  V  $\pm 10\%$ ,  $R_L = 5$  kΩ,  $C_L = 150$  pF)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{RD}$ data delay time	$t_{RDD}$	$\overline{RD} \downarrow \rightarrow D_n$			150	ns
$\overline{RD}$ data hold time	$t_{RDH}$	$\overline{RD} \uparrow \rightarrow D_n$	10			ns
BUSY low-level time	$t_{BL}$	When full-dot data is written	3		9	CLK <sup>Note</sup>
BUSY low-level time	$t_{BL}$	When character data is written	48		54	CLK <sup>Note</sup>
SCR high-level time	$t_{SCR}$		100		550	μs

**Note** CLK = 4/fosc

**REQUIRED TIMING CONDITIONS** (Unless specified otherwise,  $T_A = -40$  to  $+85$  °C,  $C_0$  to  $C_3 = 1$  μF,  $V_{CC} = 5$  V ±10%,  $R_L = 5$  kΩ,  $C_L = 150$  pF)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Clock frequency	$f_{osc}$	μPD16435 only	3.77	4.19	4.61	MHz
High-level clock pulse width	$t_{WHC}$	μPD16435 only	100			ns
Low-level clock pulse width	$t_{WLC}$	μPD16435 only	100			ns
$\overline{RD}$ high-level width	$t_{RDH}$		200			ns
$\overline{RD}$ low-level width	$t_{RD L}$		200			ns
$\overline{WR}$ high-level width	$t_{WRH}$		200			ns
$\overline{WR}$ low-level width	$t_{WRL}$		200			ns
$\overline{WR} - \overline{RD}$ time	$t_{WRRD}$	$\overline{WR}\uparrow \rightarrow \overline{RD}\downarrow$	200			ns
$\overline{RD} - \overline{WR}$ time	$t_{RDWR}$	$\overline{RD}\uparrow \rightarrow \overline{WR}\downarrow$	200			ns
$\overline{CS}$ , $\overline{RS}$ setup time	$t_{CRS}$	$\overline{CS}\downarrow, \overline{RS} \rightarrow \overline{WR}\downarrow, \overline{RD}\downarrow$	0			ns
$\overline{CS}$ , $\overline{RS}$ hold time	$t_{CRH}$	$\overline{WR}\uparrow, \overline{RD}\uparrow \rightarrow \overline{CS}\uparrow, \overline{RS}$	300			ns
Input data setup time	$t_{DS}$	$D_n \rightarrow \overline{WR}\uparrow$	0			ns
Input data hold time	$t_{DH}$	$\overline{WR}\uparrow \rightarrow D_n$	200			ns

**SWITCHING SPECIFICATIONS** (Unless specified otherwise,  $T_A = -40$  to  $+85$  °C,  $C_0$  to  $C_3 = 1$  μF,  $V_{CC} = 2.7$  to  $3.6$  V,  $R_L = 5$  kΩ,  $C_L = 150$  pF)

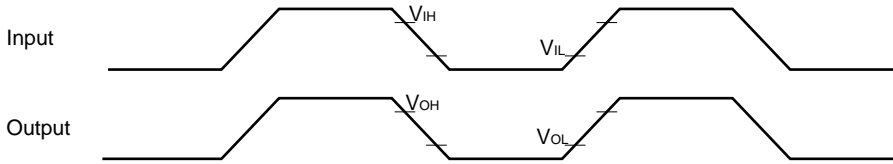
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{RD}$ data delay time	$t_{RDD}$	$\overline{RD}\downarrow \rightarrow D_n$			500	ns
$\overline{RD}$ data hold time	$t_{RDH}$	$\overline{RD}\uparrow \rightarrow D_n$	15			ns
$\overline{BUSY}$ low-level time	$t_{BL}$	When full-dot data is written	3		9	CLK <sup>Note</sup>
$\overline{BUSY}$ low-level time	$t_{BL}$	When character data is written	48		54	CLK <sup>Note</sup>
SCR high-level time	$t_{SCR}$		100		550	μs

**Note** CLK = 4/ $f_{osc}$

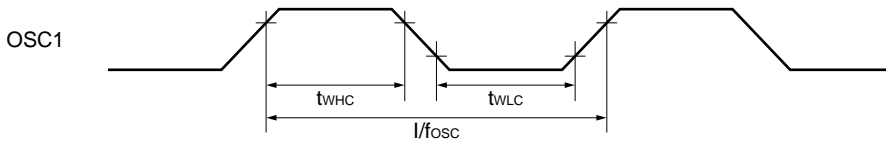
**REQUIRED TIMING CONDITIONS** (Unless specified otherwise,  $T_A = -40$  to  $+85$  °C,  $C_0$  to  $C_3 = 1$  μF,  $V_{CC} = 2.7$  to  $3.6$  V,  $R_L = 5$  kΩ,  $C_L = 150$  pF)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Clock frequency	$f_{OSC}$	μPD16435 only	3.77	4.19	4.61	MHz
High-level clock pulse width	$t_{WHC}$	μPD16435 only	100			ns
Low-level clock pulse width	$t_{WLC}$	μPD16435 only	100			ns
$\overline{RD}$ high-level width	$t_{RDH}$		400			ns
$\overline{RD}$ low-level width	$t_{RD L}$		400			ns
$\overline{WR}$ high-level width	$t_{WRH}$		400			ns
$\overline{WR}$ low-level width	$t_{WRL}$		400			ns
$\overline{WR} - \overline{RD}$ time	$t_{WRRD}$	$\overline{WR}\uparrow \rightarrow \overline{RD}\downarrow$	400			ns
$\overline{RD} - \overline{WR}$ time	$t_{RDWR}$	$\overline{RD}\uparrow \rightarrow \overline{WR}\downarrow$	400			ns
CS, RS setup time	$t_{CRS}$	$\overline{CS}\downarrow, RS \rightarrow \overline{WR}\downarrow, \overline{RD}\downarrow$	0			ns
CS, RS hold time	$t_{CRH}$	$\overline{WR}\uparrow, \overline{RD}\uparrow \rightarrow \overline{CS}\uparrow, RS$	600			ns
Input data setup time	$t_{DS}$	$D_n \rightarrow \overline{WR}\uparrow$	0			ns
Input data hold time	$t_{DH}$	$\overline{WR}\uparrow \rightarrow D_n$	400			ns

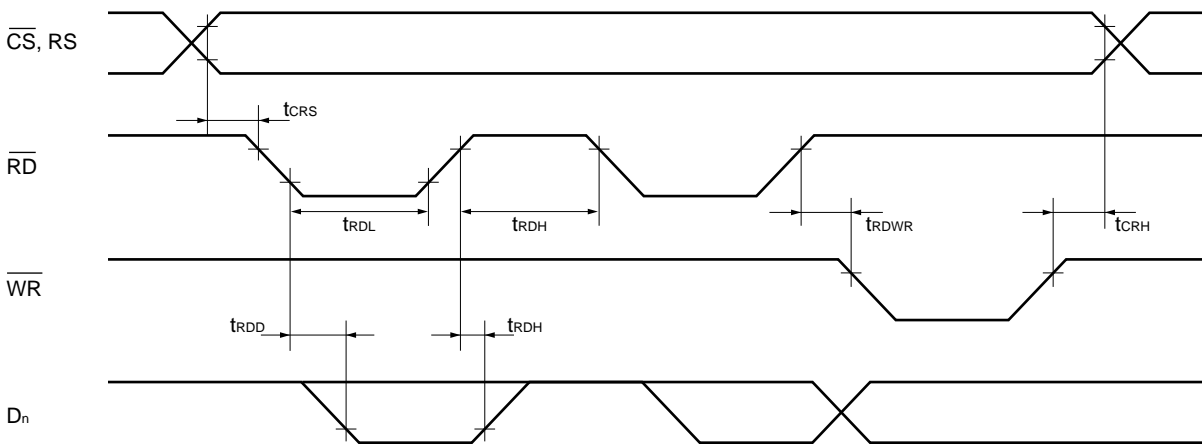
**AC TIMING TEST VOLTAGE**



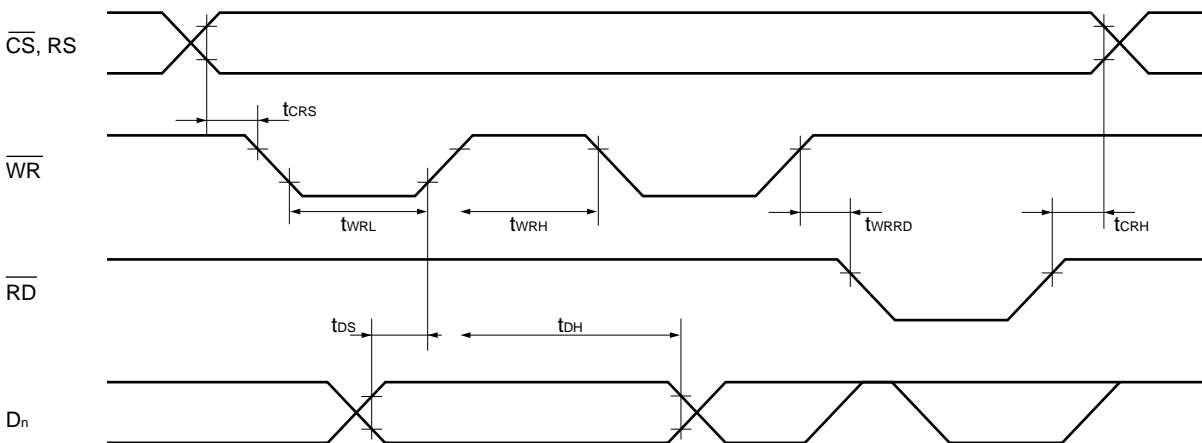
**AC CHARACTERISTICS WAVEFORM OSC**



**READ TIMING**

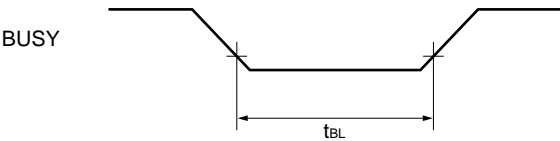


**WRITE TIMING**

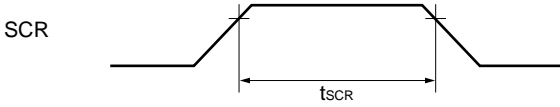




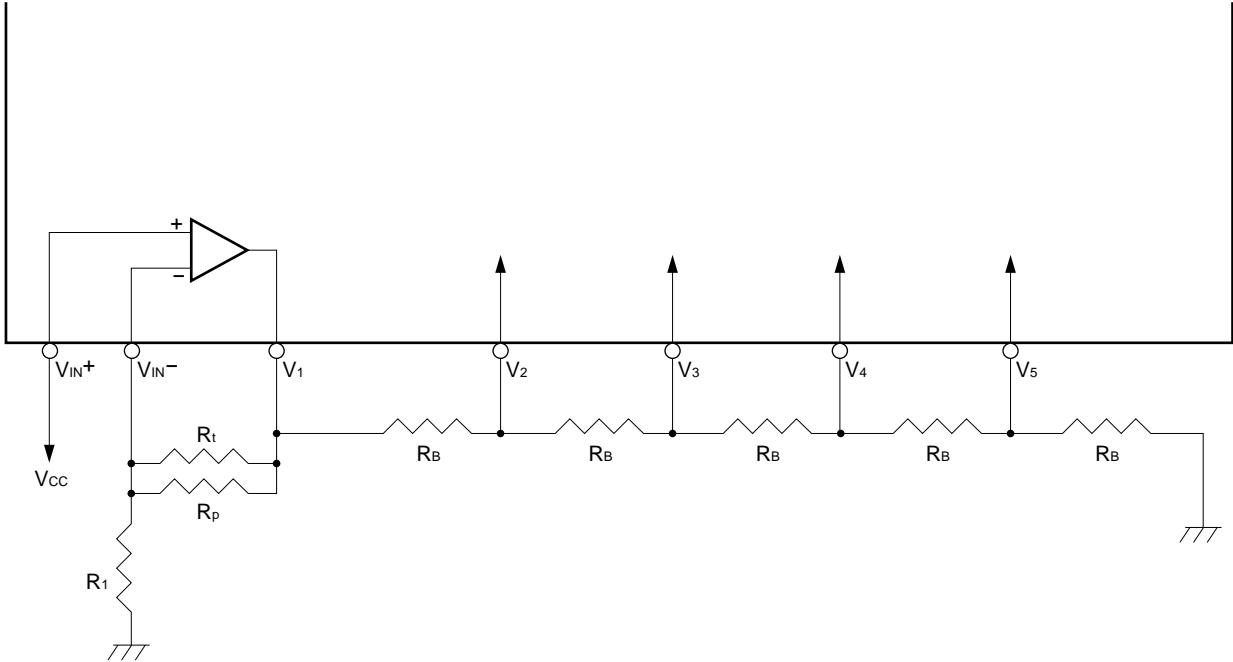
**BUSY**



**SCR**

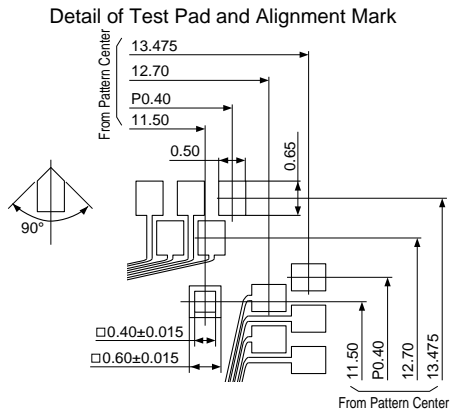
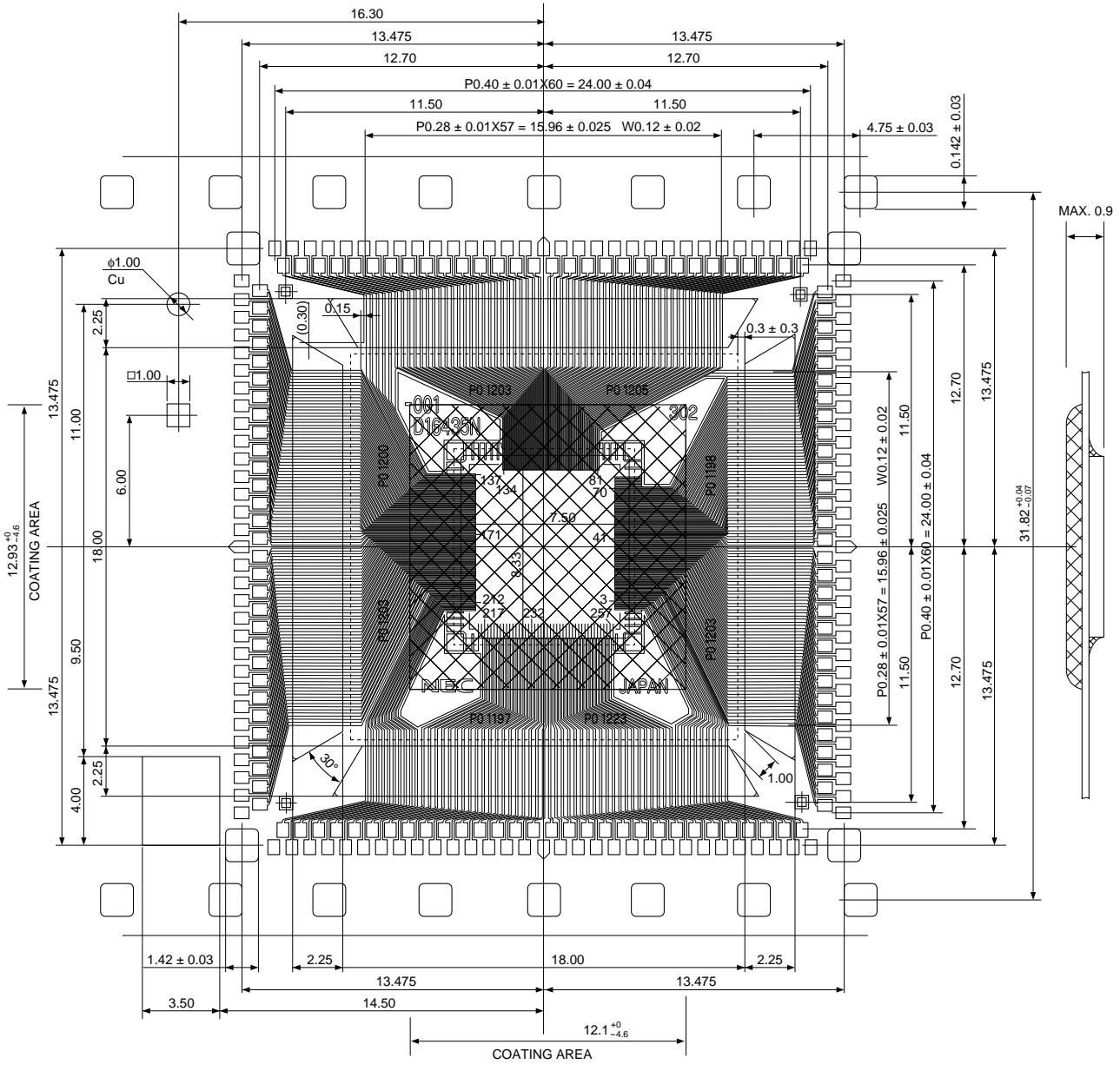


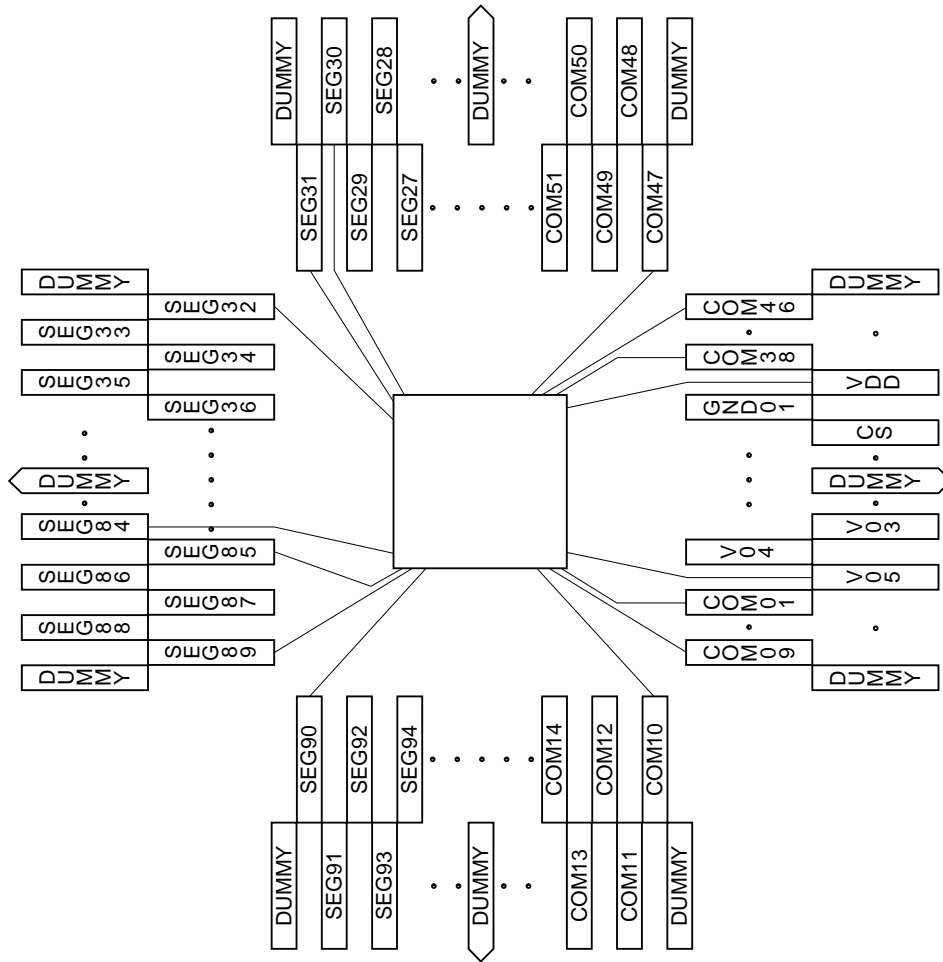
EXAMPLE TEMPERATURE CORRECTION CIRCUIT CONNECTION



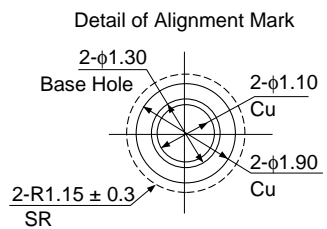
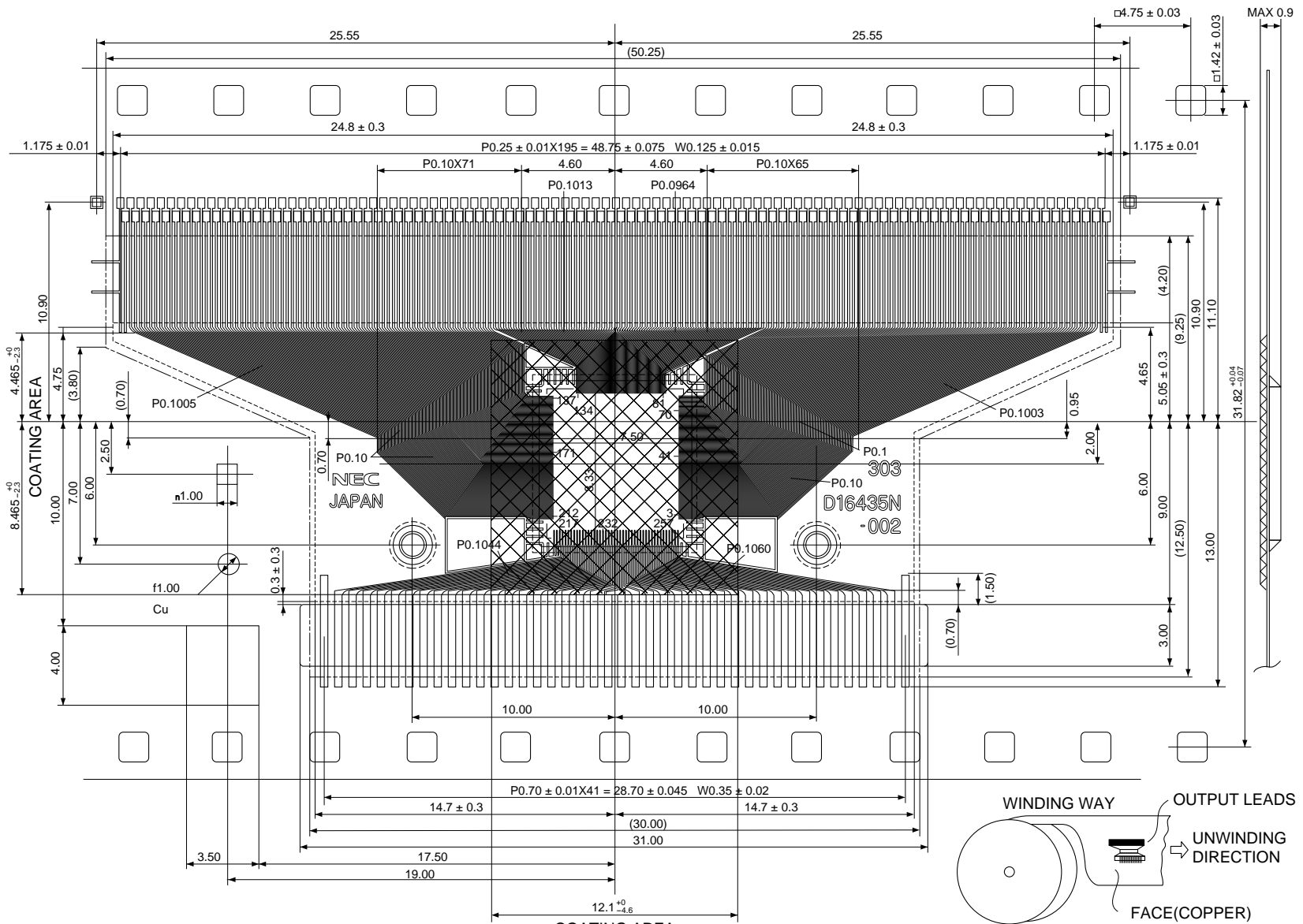
$R_t$ : Thermistor

STANDARD TCP PACKAGE DRAWINGS (μPD16435N-001-001, μPD16435AN-001-001)





STANDARD TCP PACKAGE DRAWINGS (μPD16435N-001-002)



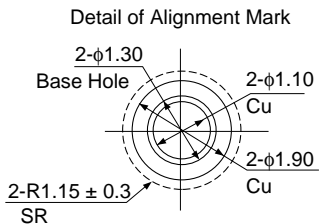
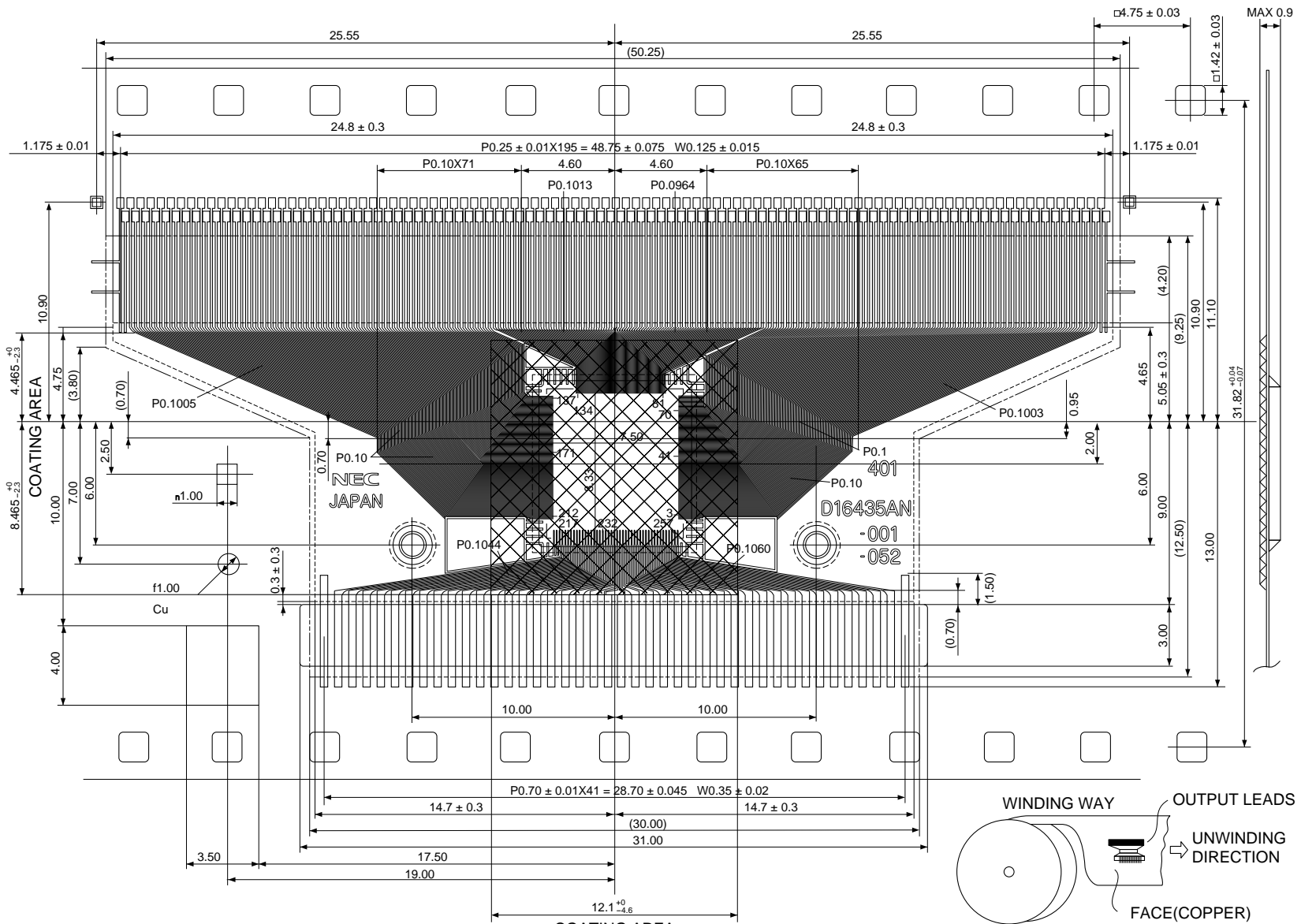
MATERIAL

BASE FILM	: UPLEX-S	t=75 mm
ADHESIVE	: EPOXY	t=12 mm
COPPER FOIL	: ELECTROLYSIS Cu	t=18 mm
PLATING	: Sn	t=MIN 0.25 mm
SOLDER RESIST	: EPOXY	t=25 mm

This Figure is shown by Copper side over Polyimide  
 All tolerances unless otherwise specified 0.05 mm.  
 Coner radius is 0.3 mm Max.  
 II Sprocket holes (52.25 mm) for 1 Pattern



STANDARD TCP PACKAGE DRAWINGS (μPD16435AN-001-052)



MATERIAL

BASE FILM	: UPILEX-S	t=75 mm
ADHESIVE	: EPOXY	t=12 mm
COPPER FOIL	: ELECTROLYSIS Cu	t=18 mm
PLATING	: Sn	t=MIN 0.25 mm
SOLDER RESIST	: EPOXY	t=25 mm

This Figure is shown by Copper side over Polyimide  
All tolerances unless otherwise specified 0.05 mm.  
Coner radius is 0.3 mm Max.  
II Sprocket holes (52.25 mm) for 1 Pattern





**REFERENCE DOCUMENTS**

NEC Semiconductor Device Reliability/Quality Control System (IEI-1212)  
Semiconductor Device Mounting Technology Manual (C10535E)

[MEMO]

[MEMO]

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