NEC

MOS INTEGRATED CIRCUIT

μPD16641

SOURCE DRIVER FOR 240-OUTPUT TFT-LCD (64 GRAY SCALES)

DESCRIPTION

The μPD16641 is a source driver for TFT-LCD 64 gray scale displays. Its logic circuit operates at 3.3 V and the driver circuit operates at 3.3 or 5.0 V (selectable). The input data is digital data at 6 bits × 3 dots, and 260,000 colors can be displayed in 64-value outputs γ-corrected by the internal D/A converter and 11 external power supplies.

Because the clock frequency is 33 MHz_{MIN}, the μPD16641 can be used in TFT-LCD panels conforming to the VGA standards.

FEATURES

- Precharge-less output buffer
- 64-value output by 11 external power supplies and internal D/A converter
- Level of γ-corrected power supply can be inverted
- Output voltage range: 2.8 $V_{P\text{-}PMAX.}$ (at supply voltage V_{DD2} of driver circuit = 3.0 V)
  4.3 $V_{P\text{-}PMAX.}$ (at supply voltage V_{DD2} of driver circuit = 4.5 V)
- CMOS level input
- 6 bit (gray scale data) × 3 dot input
- High-speed data transfer: $f_{max.}$ = 33 $MHz_{MIN.}$ (internal data transfer rate at supply voltage V_{DD1} of logic circuit = 3.0 V)
- 240 outputs
- Supply voltage of driver circuit selectable (V_{sel} = H: 3.3 V, V_{sel} = L: 5.0 V)
- Slim TCP

ORDERING INFORMATION

Part No.	Package
μPD16641N-×××	TCP (TAB package)

The TCP is custom-made. For details, consult NEC

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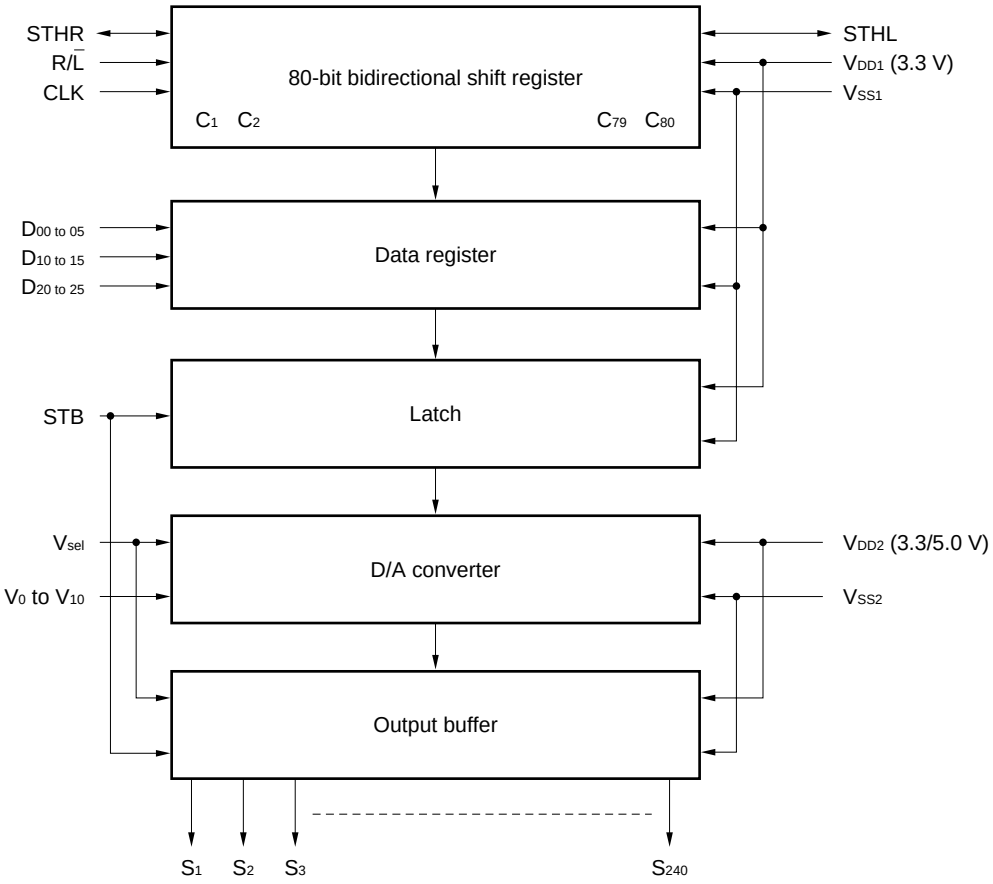
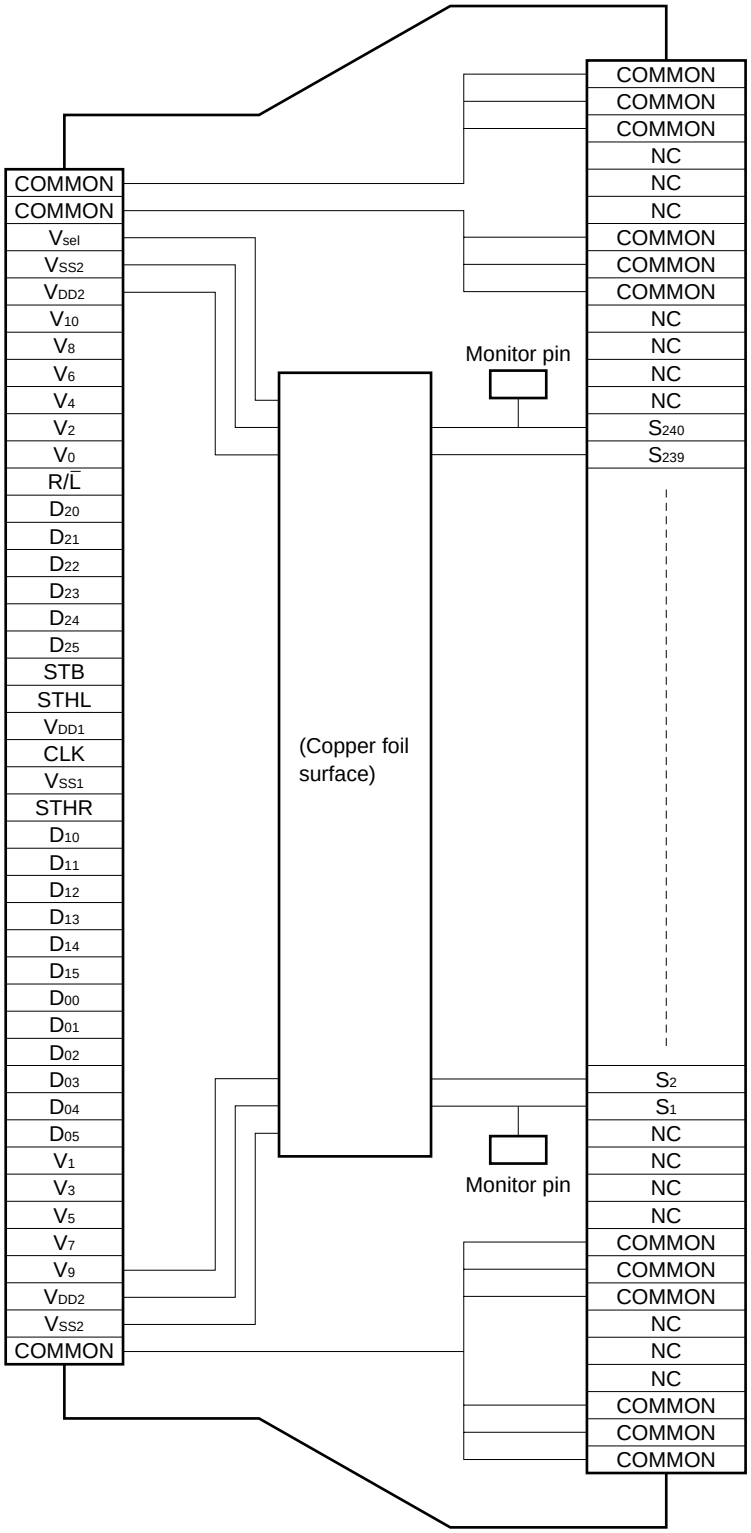
1. BLOCK DIAGRAM



2. PIN CONFIGURATION (standard TCP: μPD16641N-xxx)



V_{sel} pin is internally pulled up.

Therefore, the number of input pins can be reduced by opening or short-circuiting these pins to V_{SS2} by means of TCP wiring.

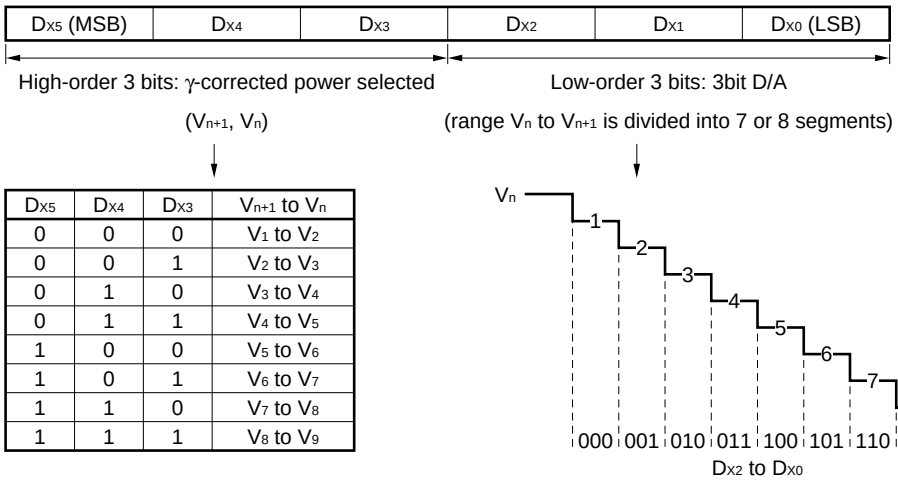
3. PIN DESCRIPTION

Pin Symbol	Pin Name	Description
S_1 to S_{240}	Driver output	Output 64 gray scale analog voltages converted from digital signals.
D_{00} to D_{05}	Display data input	Inputs 18-bit-wide display gray scale data (6 bits) × 3 dots (RGB). D_{X0}: LSB, D_{X5}: MSB
D_{10} to D_{15}		
D_{20} to D_{25}		
R/$\overline{L}$	Shift direction select input	This pin inputs/outputs start pulses when two or more μPD16641s are connected in cascade. Shift direction of shift register is as follows: R/$\overline{L}$ = H : STHR input, $S_1 \rightarrow S_{240}$, STHL output R/$\overline{L}$ = L : STHL input, $S_{240} \rightarrow S_1$, STHR output
STHR	Right shift start pulse I/O	R/$\overline{L}$ = H : Inputs start pulse. R/$\overline{L}$ = L : Outputs start pulse.
STHL	Left shift start pulse I/O	R/$\overline{L}$ = H : Outputs start pulse. R/$\overline{L}$ = L : Inputs start pulse.
V_{sel}	Driver voltage selection	Selects driver voltage. This pin is internally pulled up to V_{DD2}. V_{sel} = V_{DD2} or OPEN: V_{DD2} = 3.3 V ± 0.3 V, V_{sel} = L: V_{DD2} = 5.0 V ± 0.5 V
CLK	Shift clock input	Inputs shift clock to shift register. Display data is loaded to data register at rising edge of this pin. Start pulse output goes high at rising edge of 80th clock after start pulse has been input, and serves as start pulse to driver in next stage. 80th clock of driver in first stage serves as start pulse of driver in next stage.
STB	Latch input	Contents of data register are latched at rising edge, transferred to D/A converter, and output as analog voltage corresponding to display data. Contents of initial shift register are cleared after STB has been input. One pulse of this signal is input when μPD16641 is started, and then device operates normally. For STB input timing, refer to **Relations between STB, Start Pulse, and Blanking Period in Switching Characteristic Waveform**.
V_0 to V_{10}	γ-corrected power supply	Inputs γ-corrected power from external source. $V_{SS2} \le V_{10} \le V_9 \le V_8 \le V_7 \le V_6 \le V_5 \le V_4 \le V_3 \le V_2 \le V_1 \le V_0 \le V_{DD2}$ $V_{SS2} \le V_0 \le V_1 \le V_2 \le V_3 \le V_4 \le V_5 \le V_6 \le V_7 \le V_8 \le V_9 \le V_{10} \le V_{DD2}$ Maintain gray scale power supply during gray scale voltage output.
V_{DD1}	Logic circuit power supply	3.3 V ± 0.3 V
V_{DD2}	Driver circuit power supply	V_{sel} = V_{DD2} or OPEN : V_{DD2} = 3.3 V ± 0.3 V V_{sel} = L : V_{DD2} = 5.0 V ± 0.5 V
V_{SS1}	Logic ground	Ground
V_{SS2}	Driver ground	Ground

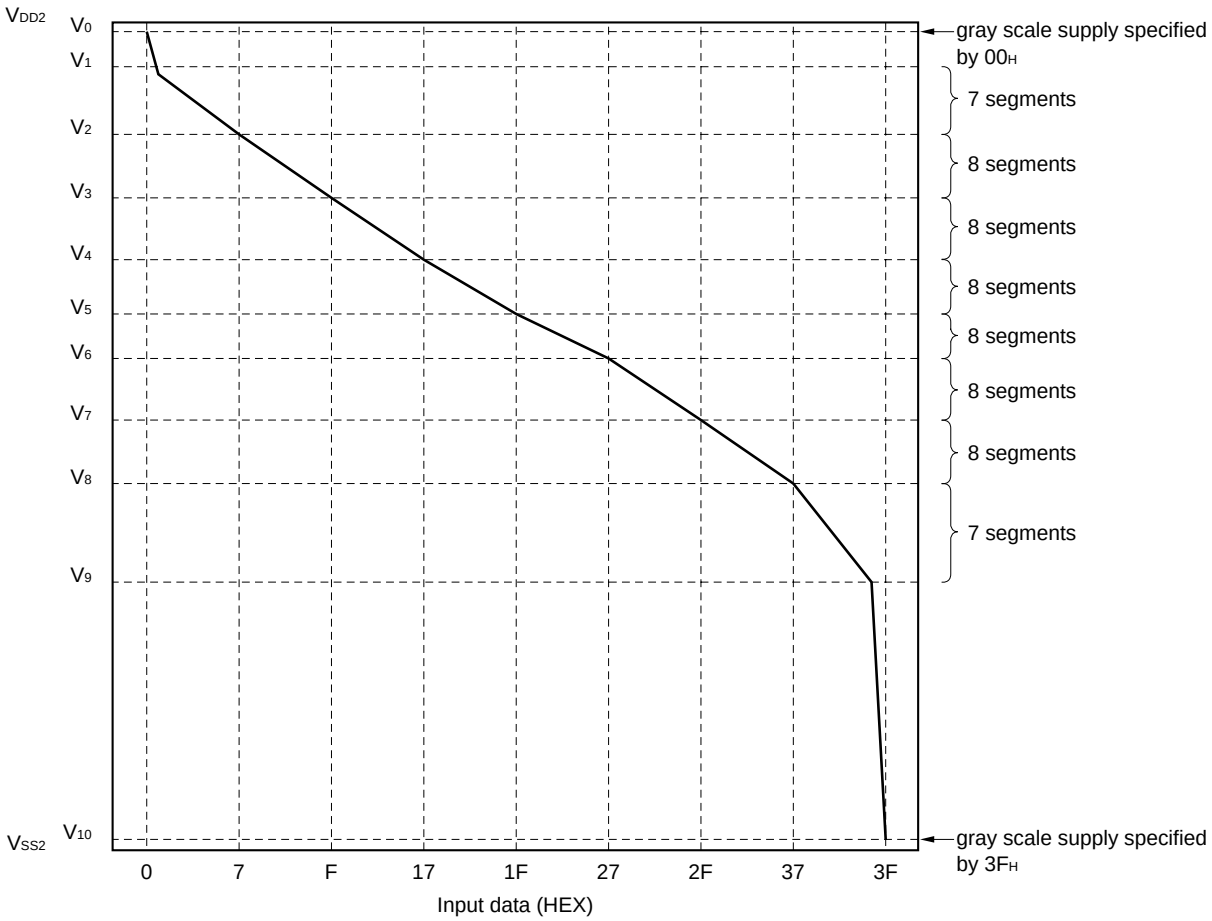
Caution Be sure to turn on power in the order V_{DD1}, logic input, V_{DD2}, and gray scale power (V_0 to V_{10}), and turn off power in the reverse order, to prevent the μPD16641 from being damaged by latchup. Be sure to observe this power sequence even during a transition period.

4. RELATION BETWEEN INPUT DATA AND OUTPUT VOLTAGE VALUE

The 11 major points on the γ characteristic curve of the LCD panel are arbitrarily set by external power supplies V_0 through V_{10}. If the display data is 00_H or $3F_H$, gray scale voltage V_0 or V_{10} is output. If the display data is in the range 01_H to $3E_H$, the high-order 3 bits select an external powers pair V_{n+1}, V_n. The low-order 3 bits evenly divide the range of V_{n+1} to V_n into eight segments by means of D/A conversion (however, the ranges from V_9 to V_8 and from V_2 to V_1 are divided into seven segments) to output a 64 gray scale voltage.



D_{X5}	D_{X4}	D_{X3}	V_{n+1} to V_n
0	0	0	V_1 to V_2
0	0	1	V_2 to V_3
0	1	0	V_3 to V_4
0	1	1	V_4 to V_5
1	0	0	V_5 to V_6
1	0	1	V_6 to V_7
1	1	0	V_7 to V_8
1	1	1	V_8 to V_9

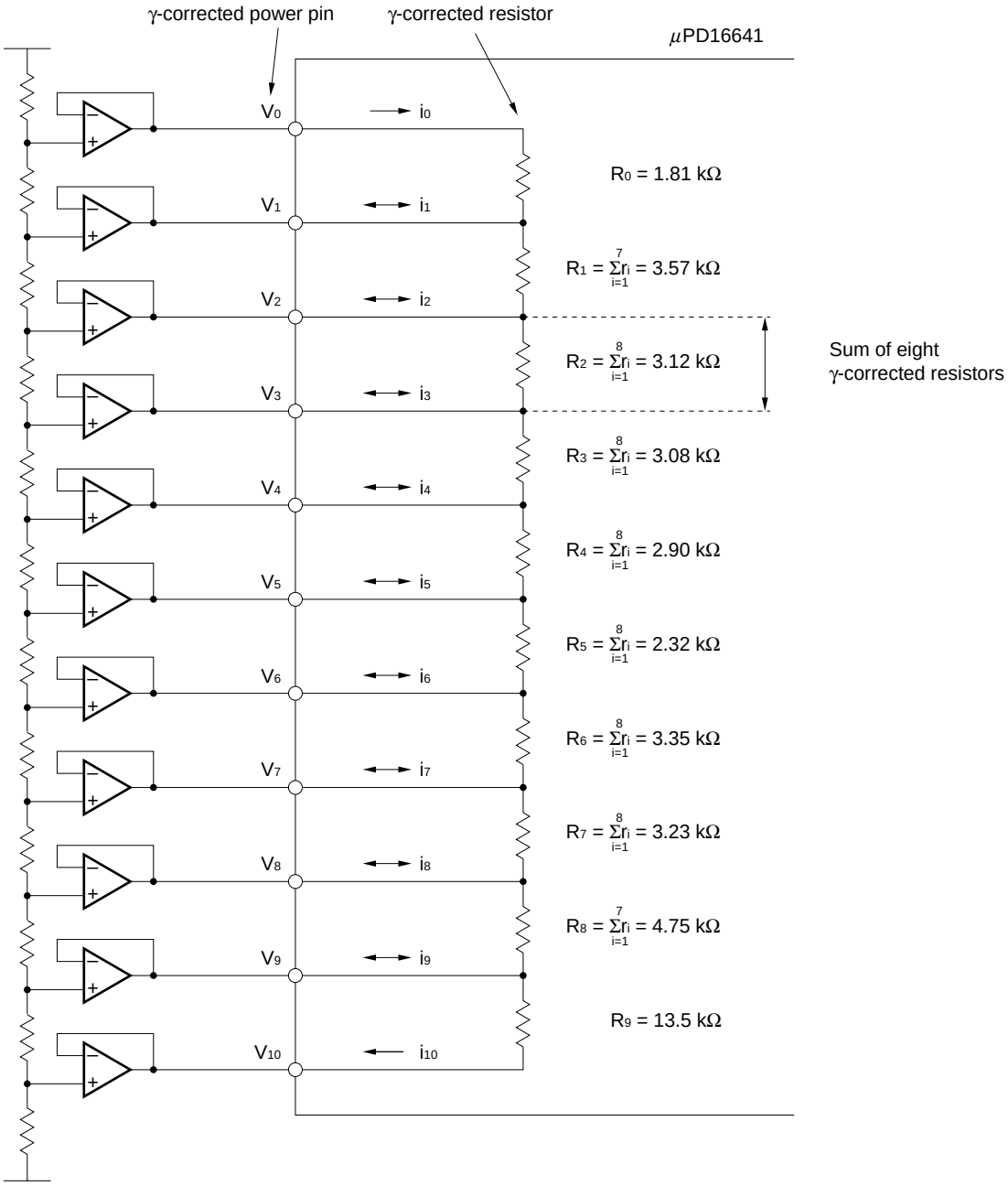


Relation between Input Data and Output Voltage

Input Data	D_{X5}	D_{X4}	D_{X3}	D_{X2}	D_{X1}	D_{X0}	Output Voltage
00_H	0	0	0	0	0	0	V_0
01_H	0	0	0	0	0	1	$V_2 + (V_1 - V_2) \times 6/7$
02_H	0	0	0	0	1	0	$V_2 + (V_1 - V_2) \times 5/7$
03_H	0	0	0	0	1	1	$V_2 + (V_1 - V_2) \times 4/7$
04_H	0	0	0	1	0	0	$V_2 + (V_1 - V_2) \times 3/7$
05_H	0	0	0	1	0	1	$V_2 + (V_1 - V_2) \times 2/7$
06_H	0	0	0	1	1	0	$V_2 + (V_1 - V_2) \times 1/7$
07_H	0	0	0	1	1	1	V_2
08_H	0	0	1	0	0	0	$V_3 + (V_2 - V_3) \times 7/8$
09_H	0	0	1	0	0	1	$V_3 + (V_2 - V_3) \times 6/8$
$0A_H$	0	0	1	0	1	0	$V_3 + (V_2 - V_3) \times 5/8$
$0B_H$	0	0	1	0	1	1	$V_3 + (V_2 - V_3) \times 4/8$
$0C_H$	0	0	1	1	0	0	$V_3 + (V_2 - V_3) \times 3/8$
$0D_H$	0	0	1	1	0	1	$V_3 + (V_2 - V_3) \times 2/8$
$0E_H$	0	0	1	1	1	0	$V_3 + (V_2 - V_3) \times 1/8$
$0F_H$	0	0	1	1	1	1	V_3
10_H	0	1	0	0	0	0	$V_4 + (V_3 - V_4) \times 7/8$
11_H	0	1	0	0	0	1	$V_4 + (V_3 - V_4) \times 6/8$
12_H	0	1	0	0	1	0	$V_4 + (V_3 - V_4) \times 5/8$
13_H	0	1	0	0	1	1	$V_4 + (V_3 - V_4) \times 4/8$
14_H	0	1	0	1	0	0	$V_4 + (V_3 - V_4) \times 3/8$
15_H	0	1	0	1	0	1	$V_4 + (V_3 - V_4) \times 2/8$
16_H	0	1	0	1	1	0	$V_4 + (V_3 - V_4) \times 1/8$
17_H	0	1	0	1	1	1	V_4
18_H	0	1	1	0	0	0	$V_5 + (V_4 - V_5) \times 7/8$
19_H	0	1	1	0	0	1	$V_5 + (V_4 - V_5) \times 6/8$
$1A_H$	0	1	1	0	1	0	$V_5 + (V_4 - V_5) \times 5/8$
$1B_H$	0	1	1	0	1	1	$V_5 + (V_4 - V_5) \times 4/8$
$1C_H$	0	1	1	1	0	0	$V_5 + (V_4 - V_5) \times 3/8$
$1D_H$	0	1	1	1	0	1	$V_5 + (V_4 - V_5) \times 2/8$
$1E_H$	0	1	1	1	1	0	$V_5 + (V_4 - V_5) \times 1/8$
$1F_H$	0	1	1	1	1	1	V_5
20_H	1	0	0	0	0	0	$V_6 + (V_5 - V_6) \times 7/8$
21_H	1	0	0	0	0	1	$V_6 + (V_5 - V_6) \times 6/8$
22_H	1	0	0	0	1	0	$V_6 + (V_5 - V_6) \times 5/8$
23_H	1	0	0	0	1	1	$V_6 + (V_5 - V_6) \times 4/8$
24_H	1	0	0	1	0	0	$V_6 + (V_5 - V_6) \times 3/8$
25_H	1	0	0	1	0	1	$V_6 + (V_5 - V_6) \times 2/8$
26_H	1	0	0	1	1	0	$V_6 + (V_5 - V_6) \times 1/8$
27_H	1	0	0	1	1	1	V_6
28_H	1	0	1	0	0	0	$V_7 + (V_6 - V_7) \times 7/8$
29_H	1	0	1	0	0	1	$V_7 + (V_6 - V_7) \times 6/8$
$2A_H$	1	0	1	0	1	0	$V_7 + (V_6 - V_7) \times 5/8$
$2B_H$	1	0	1	0	1	1	$V_7 + (V_6 - V_7) \times 4/8$
$2C_H$	1	0	1	1	0	0	$V_7 + (V_6 - V_7) \times 3/8$
$2D_H$	1	0	1	1	0	1	$V_7 + (V_6 - V_7) \times 2/8$
$2E_H$	1	0	1	1	1	0	$V_7 + (V_6 - V_7) \times 1/8$
$2F_H$	1	0	1	1	1	1	V_7
30_H	1	1	0	0	0	0	$V_8 + (V_7 - V_8) \times 7/8$
31_H	1	1	0	0	0	1	$V_8 + (V_7 - V_8) \times 6/8$
32_H	1	1	0	0	1	0	$V_8 + (V_7 - V_8) \times 5/8$
33_H	1	1	0	0	1	1	$V_8 + (V_7 - V_8) \times 4/8$
34_H	1	1	0	1	0	0	$V_8 + (V_7 - V_8) \times 3/8$
35_H	1	1	0	1	0	1	$V_8 + (V_7 - V_8) \times 2/8$
36_H	1	1	0	1	1	0	$V_8 + (V_7 - V_8) \times 1/8$
37_H	1	1	0	1	1	1	V_8
38_H	1	1	1	0	0	0	$V_9 + (V_8 - V_9) \times 6/7$
39_H	1	1	1	0	0	1	$V_9 + (V_8 - V_9) \times 5/7$
$3A_H$	1	1	1	0	1	0	$V_9 + (V_8 - V_9) \times 4/7$
$3B_H$	1	1	1	0	1	1	$V_9 + (V_8 - V_9) \times 3/7$
$3C_H$	1	1	1	1	0	0	$V_9 + (V_8 - V_9) \times 2/7$
$3D_H$	1	1	1	1	0	1	$V_9 + (V_8 - V_9) \times 1/7$
$3E_H$	1	1	1	1	1	0	V_9
$3F_H$	1	1	1	1	1	1	V_{10}

γ-Corrected Power Circuit

The reference power supply of the D/A converter consists of a ladder circuit with a total of 64 resistors, and resistance Σri between γ-corrected power pins differs depending on each pair of γ-corrected power pins. One pair of γ-corrected power pins consists of seven or eight series resistors, and resistance Σri in the figure below is indicated as the sum of the seven of eight resistors. The resistance ratio between the γ-corrected power pins (Σri ratio) is designed to be a value relatively close to the ratio of the γ-corrected voltages V_1 through V_9 (gray scale voltages in 8 steps) used in an actual LCD panel. Under ideal conditions where there is no difference between the two, therefore, there is no voltage difference between the voltage of the γ-corrected power supplies and the gray scale voltages in 8 steps of the resistor ladder circuits of the μPD16641, and no current flows into the γ-corrected power pins V_1 through V_9. As a result, a voltage follower circuit is not necessary.



Relation between Input Data and Output Data

Data format : 1 pixel data (6 bits) × RGB (3 dots)

Input width : 18 bits

R/$\overline{L}$ = H (right shift)

Output	S_1	S_2	S_3	⋯	S_{239}	S_{240}
Data	D_{00} to D_{05}	D_{10} to D_{15}	D_{20} to D_{25}	⋯	D_{10} to D_{15}	D_{20} to D_{25}

R/$\overline{L}$ = L (left shift)

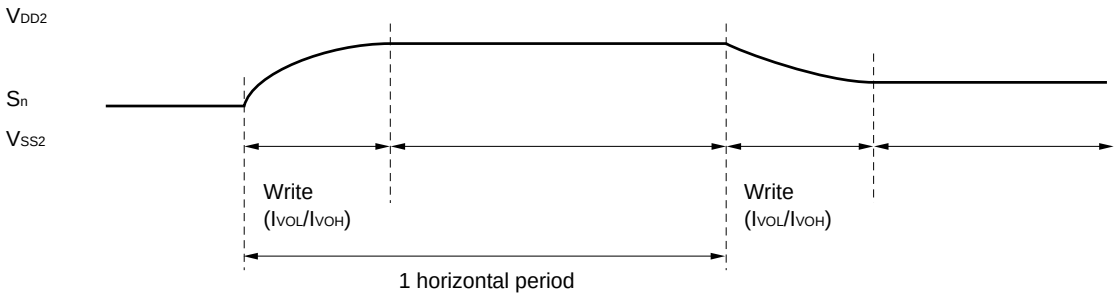
Output	S_1	S_2	S_3	⋯	S_{239}	S_{240}
Data	D_{00} to D_{05}	D_{10} to D_{15}	D_{20} to D_{25}	⋯	D_{10} to D_{15}	D_{20} to D_{25}

5. OPERATION OF OUTPUT BUFFER

The output buffer consists of an operational amplifier circuit that does not perform precharge operation. Therefore, driver output current $I_{VOH1/2}$ is the charging current to the LCD, and $I_{VOL1/2}$ is the discharging current.

The chip has the driving capability to charge or discharge a liquid load with C_L = 80 pF to 3 τ in less than 10 μs.

<LCD panel driving waveform of μPD16641>



6. ELECTRIC SPECIFICATION

Absolute Maximum Ratings (V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD1}	–0.3 to +4.5	V
Supply voltage	V_{DD2}	–0.3 to +7.0	V
Input voltage	V_I	–0.3 to $V_{DD1, 2}$ + 0.3	V
Output voltage	V_O	–0.3 to $V_{DD1, 2}$ + 0.3	V
Permissible dissipation	P_D	150	mW
Operating temperature range	T_A	–10 to +75	°C
Storage temperature range	$T_{stg.}$	–55 to +125	°C

Recommended Operating Range (T_A = –10 to +75°C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Logic supply voltage	V_{DD1}		3.0	3.3	3.6	V
Driver supply voltage	V_{DD2}	V_{sel} = H	3.0	3.3	3.6	V
Driver supply voltage	V_{DD2}	V_{sel} = L	4.5	5.0	5.5	V
γ-corrected power	V_0 to V_{10}		V_{SS2} + 0.1		V_{DD2} – 0.1	V
Maximum clock frequency	$f_{max.}$		33			MHz
Output load capacitance	C_L				150	pF

Electrical Characteristics (T_A = –10 to +75°C, V_{DD1} = 3.0 to 3.6 V, V_{DD2} = 3.0 to 3.6 V or 4.5 to 5.5 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
High-level input voltage	V_{IH}	R/$\overline{L}$, CLK, STB, STHR (L), D_{00-05}, D_{10-15}, D_{20-25}		0.7V_{DD1}		V_{DD1}	V
Low-level input voltage	V_{IL}			0		0.3V_{DD1}	V
Input leakage current	I_L	D_{00-05}, D_{10-15}, D_{20-25} R/$\overline{L}$, CLK, STB, STHR (L)				±1.0	μA
Pull-up resistor	R_{PU}	V_{sel}, V_{DD2} = 5.0 V, V_{sel}, = 0 V		40	100	250	kΩ
High-level output voltage	V_{OH}	STHR (L), I_O = –1.0 mA		V_{DD1} – 0.5			V
Low-level output voltage	V_{OL}	STHR (L), I_O = +1.0 mA				0.5	V
Static current consumption of γ-corrected power (V_{DD2} = 3.3 V)	I_{Vn1}	V_{DD1} = 3.3 V, V_{DD2} = 3.3 V V_0 = 3.20 V, V_6 = 1.95 V V_1 = 3.07 V, V_7 = 1.70 V V_2 = 2.80 V, V_8 = 1.46 V V_3 = 2.57 V, V_9 = 1.11 V V_4 = 2.34 V, V_{10} = 0.10 V V_5 = 2.12 V,[Note]	V_{10}	–200	–150		μA
			V_9 to V_1		±10		μA
			V_0		150	200	μA
Static current consumption of γ-corrected power (V_{DD2} = 5.0 V)	I_{Vn2}	V_{DD1} = 3.3 V, V_{DD2} = 5.0 V V_0 = 4.90 V, V_6 = 2.96 V V_1 = 4.69 V, V_7 = 2.58 V V_2 = 4.28 V, V_8 = 2.20 V V_3 = 3.92 V, V_9 = 1.66 V V_4 = 3.56 V, V_{10} = 0.1 V V_5 = 3.23 V,[Note]	V_{10}	–300	–250		μA
			V_9 to V_1		±10		μA
			V_0		250	300	μA

(V_X is output voltage of analog output pin S_1 to S_{240}. V_{OUT} is the voltage applied to analog output pin S_1 to S_{240}.)

Note Apply ideal voltage to V_1 to V_9 that is calculated from internal resistor.

Electrical Characteristics (T_A = –10 to +75°C, V_{DD1} = 3.0 to 3.6 V, V_{DD2} = 3.0 to 3.6 V or 4.5 to 5.5 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Driver output current (V_{DD2} = 3.3 V)	I_{VOH1}	STB = 3.3 V V_{OUT} = 2.2 V, V_X = 3.2 V V_{DD1} = V_{DD2} = 3.3 V		–0.3	–0.075	mA
	I_{VOL1}	STB = 3.3 V V_{OUT} = 1.1 V, V_X = 0.1 V V_{DD1} = V_{DD2} = 3.3 V	0.075	0.25		mA
Driver output current (V_{DD2} = 5.0 V)	I_{VOH2}	STB = 5.0 V V_{OUT} = 3.9 V, V_X = 4.9 V V_{DD1} = 3.3 V, V_{DD2} = 5.0 V		–0.3	–0.1	mA
	I_{VOL2}	STB = 5.0 V V_{OUT} = 1.1 V, V_X = 0.1 V V_{DD1} = 3.3 V, V_{DD2} = 5.0 V	0.1	0.25		mA
Output voltage deviation	ΔV_O	V_{DD1} = 3.3 V, V_{DD2} = 3.3 V V_{OUT} = 1.65		±20	±25	mV
		V_{DD1} = 3.3 V, V_{DD2} = 5.0 V V_{OUT} = 2.50 V		±20	±25	mV
Output voltage range	V_O	Input data: 00_H to $3F_H$	V_{SS2} + 0.1		V_{DD2} – 0.1	V
Dynamic logic current consumption	I_{DD1}	No load[Note]			2.0	mA
Dynamic driver current consumption	I_{DD21}	No load, V_{DD2} = 3.3 V ± 0.3 V[Note]			5.0	mA
Dynamic driver current consumption	I_{DD22}	No load, V_{DD2} = 5.0 V ± 0.5 V[Note]			6.5	mA

Note The STB cycle is specified at 31 μs and f_{CLK} = 16 MHz. Input data: 1010… (checkerboard pattern)
Refers to current consumption per driver when cascades are connected under the assumption of VGA single-sided mounting (8 units).

Switching Characteristics (T_A = –10 to +75°C, V_{DD1} = 3.0 to 3.6 V, V_{DD2} = 3.0 to 3.6 V or 4.5 to 5.5 V, V_{SS1} = V_{SS2} = 0 V, t_r = t_f = 3.0 ns)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Start pulse delay time	t_{PLH1}	C_L = 15 pF		2.0		17	ns
Start pulse delay time	t_{PHL1}	C_L = 15 pF		2.0		17	ns
Driver output delay time 1	t_{PLH21}	V_{DD2} = 3.3 V 2 kΩ + 75 pF × 2	V_O: 0.1 V → 3.2 V		6.0	12	μs
Driver output delay time 2	t_{PLH31}				8.0	14	μs
Driver output delay time 1	t_{PHL21}		V_O: 3.2 V → 0.1 V		6.0	10	μs
Driver output delay time 2	t_{PHL31}				8.0	12	μs
Driver output delay time 1	t_{PLH22}	V_{DD2} = 5.0 V 2 kΩ + 75 pF × 2	V_O: 0.1 V → 4.9 V		6.0	10	μs
Driver output delay time 2	t_{PLH32}				8.0	12	μs
Driver output delay time 1	t_{PHL22}		V_O: 4.9 V → 0.1 V		6.0	8.0	μs
Driver output delay time 2	t_{PHL32}				8.0	10	μs
Input capacitance	C_{I1}	V_0 to V_{10}, T_A = 25°C			100		pF
Input capacitance	C_{I2}	STHR (L), T_A = 25°C			10	15	pF
Input capacitance	C_{I3}	STHR (L), other than V_0 to V_{10} T_A = 25°C			7.0	10	pF

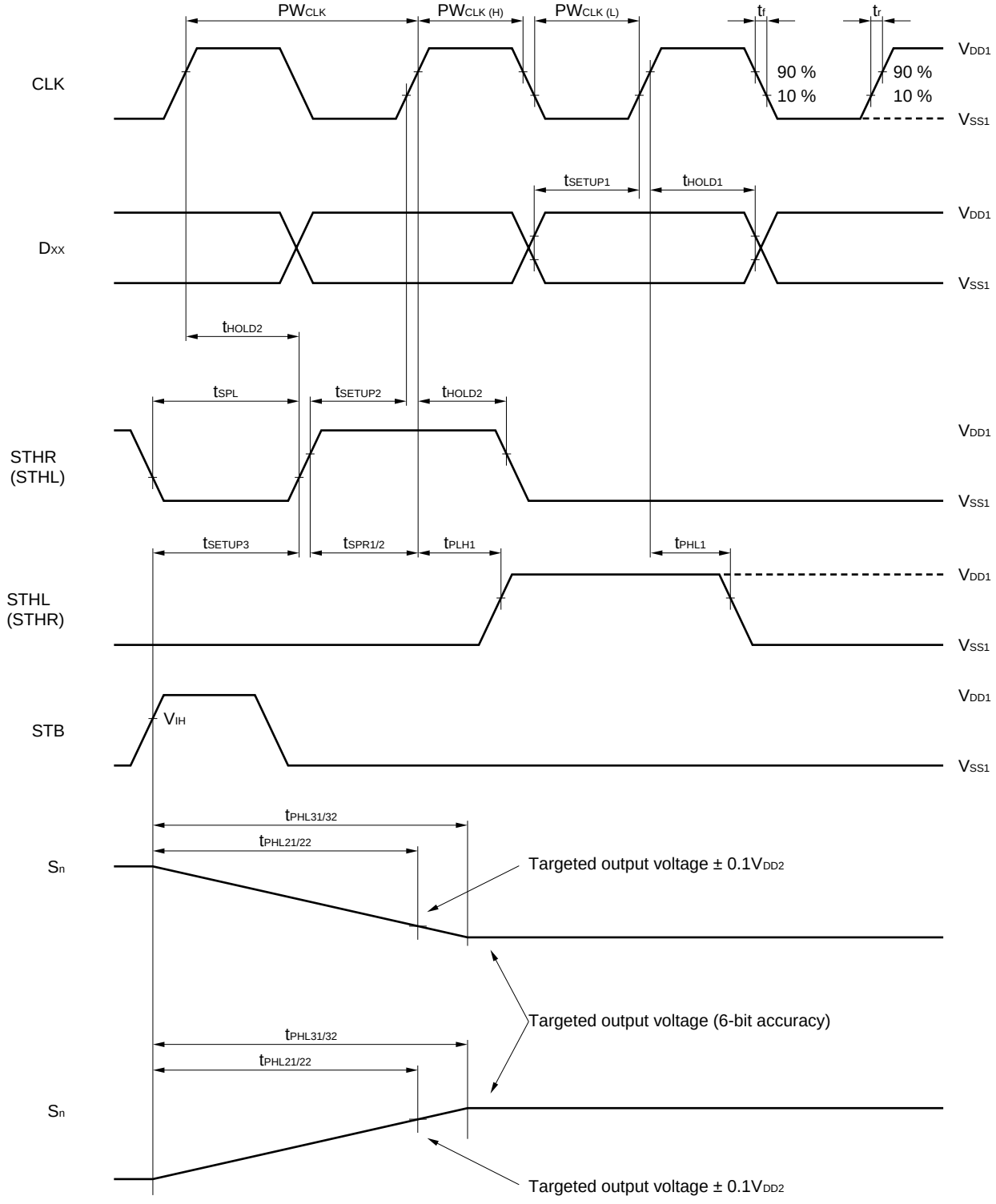
Timing Requirements (T_A = –10 to +75°C, V_{DD1} = 3.0 to 3.6 V, V_{DD2} = 3.0 to 3.6 V or 4.5 to 5.5 V, V_{SS1} = V_{SS2} = 0 V, t_r = t_f = 3.0 ns)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock pulse width	PW_{CLK}		22			ns
Clock low period	$PW_{CLK(L)}$		4.0			ns
Clock high period	$PW_{CLK(H)}$		4.0			ns
Data setup time	t_{SETUP1}		2.0			ns
Data hold time	t_{HOLD1}		2.0			ns
Start pulse setup time	t_{SETUP2}		2.0			ns
Start pulse hold time	t_{HOLD2}		2.0			ns
Start pulse low period	t_{SPL}		2			CLK
Start pulse rise time	t_{SPR}			80		CLK
STB setup time	t_{SETUP3}		1			CLK
Data invalid period	t_{INV}			1		CLK
Final data timing	t_{LDT}				1	CLK
CLK-STB time	$t_{CLK-STB}$	CLK ↑ → STB ↑ or ↓	7.0			ns
STB-CLK time	$t_{STB-CLK}$	STB ↑ or ↓ → CLK ↑	7.0			ns

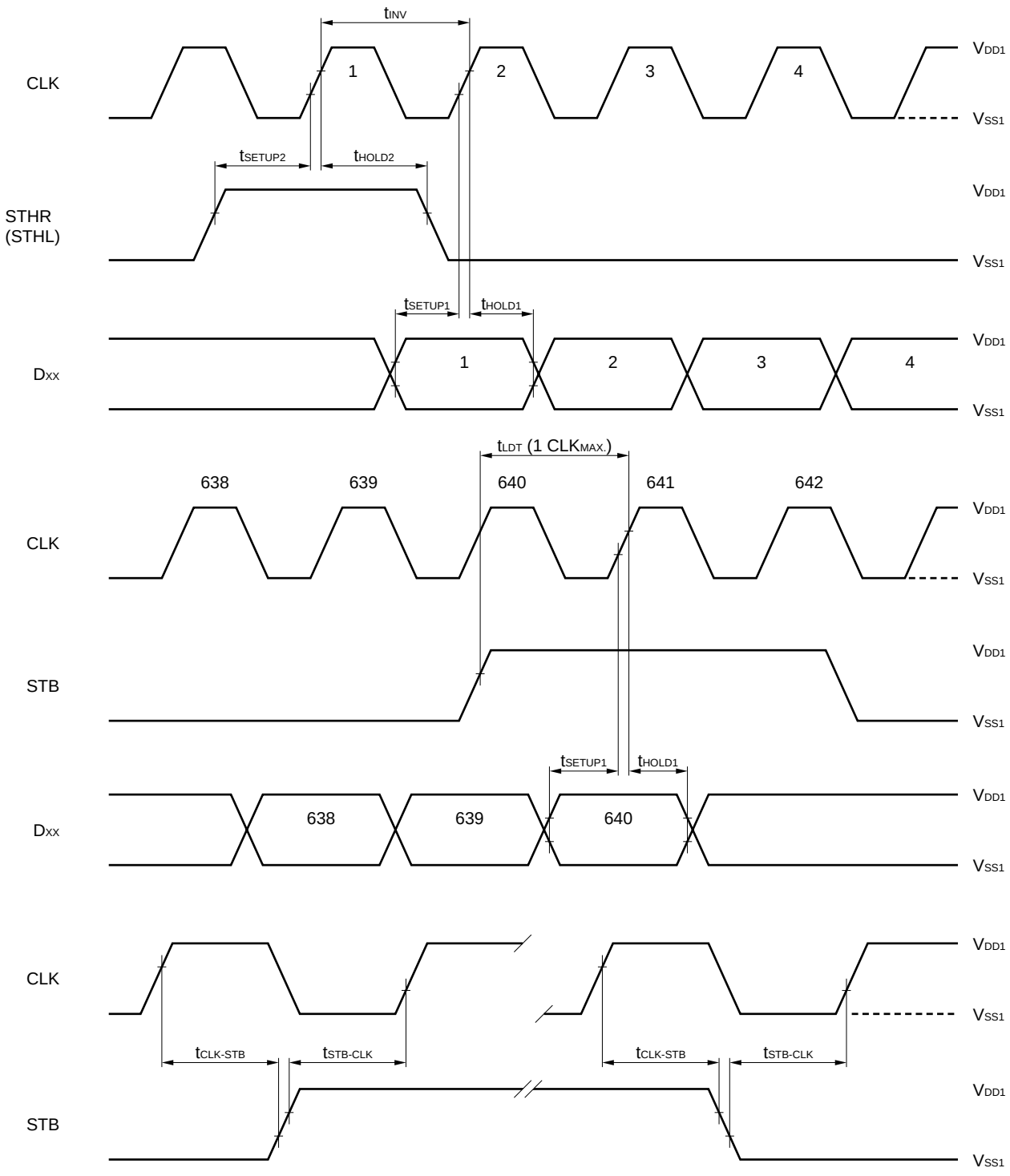
7. SWITCHING CHARACTERISTIC WAVEFORM (R/$\overline{L}$ = H)

Unless otherwise specified, the input level is V_{IH} = 0.7 V_{DD1}, V_{IL} = 0.3 V_{DD1}.

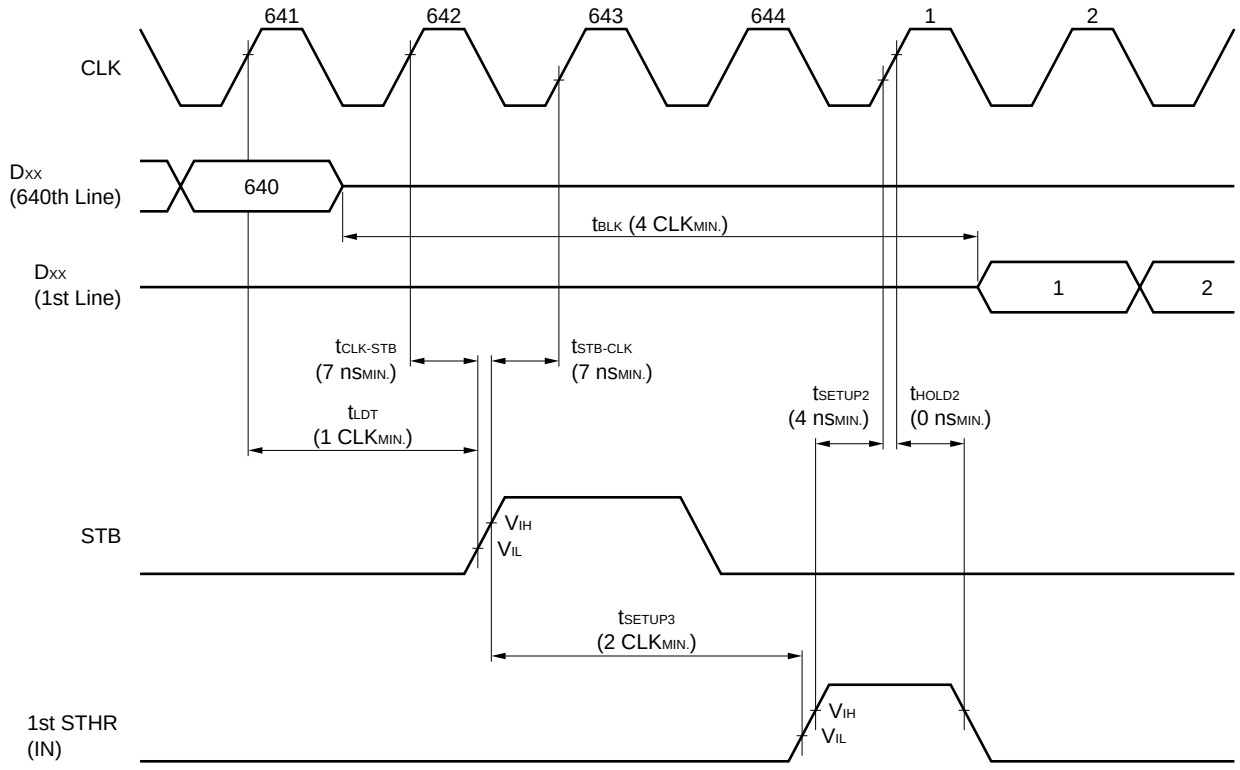
The figures in parenthesis indicate R/$\overline{L}$ = L



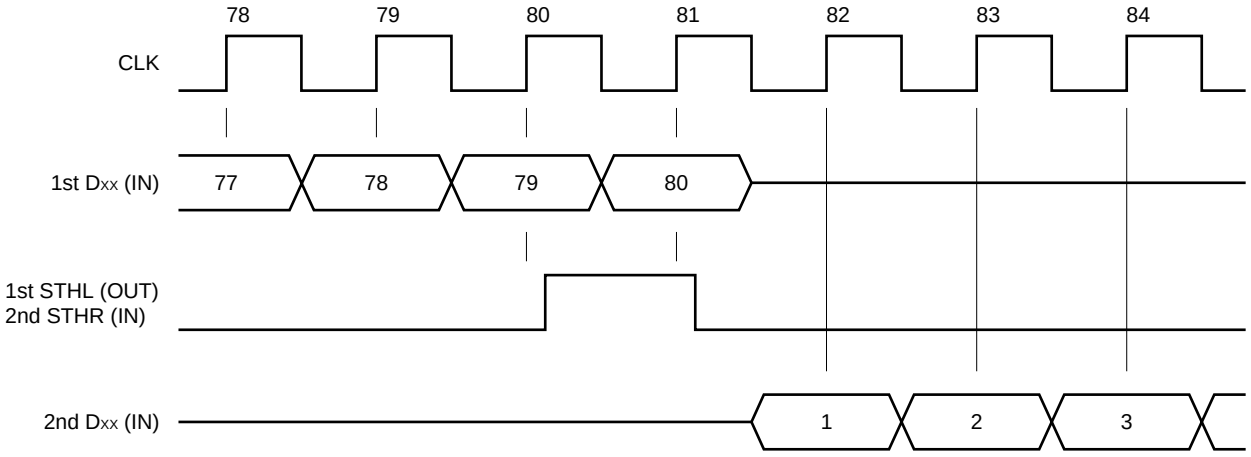
Switching Characteristic Waveform

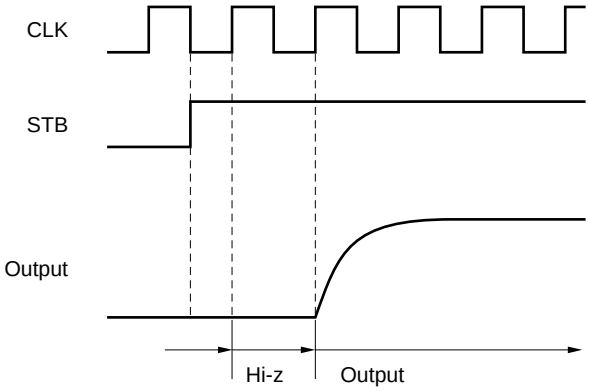


8. RELATION BETWEEN STB/STHR, STHL AND BLANKING PERIOD



9. DATA INPUT TIMING IN CASCADE CONNECTION





10. RECOMMENDED MOUNTING CONDITIONS

Mounting this product under the following conditions is recommended.

For the mounting methods and conditions other than those recommended, consult NEC.

Mounting Conditions	Mounting Method	Conditions
Thermocompression bonding	Soldering	Heating tool: 300 to 350°C, Heating time: 2 to 3 seconds, Pressure: 100 g (per product)
	ACF (sheet adhesive)	Preliminary adhesion: 70 to 100°C, Pressure: 3 to 8 kg/cm^2, Time: 3 to 5 seconds Real adhesion: 165 to 180°C, Pressure: 25 to 45 kg/cm^2, Time 30 to 40 seconds (when SUMIZAC1003 of Sumitomo Bakelite is used)

Note For the mounting conditions for ACF, consult the ACF manufacturer.
Do not use two or more mounting methods in combination.

Reference

NEC Semiconductor Device Reliability/Quality Control System (C10983E)

Quality Grades to NEC's Semiconductor Devices (C11531E)

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