

256/263-OUTPUT TFT-LCD GATE DRIVER

DESCRIPTION

The μ PD16702 is a TFT-LCD gate driver equipped with 256/263-output lines. It can output a high-gate scanning voltage in response to CMOS level input because it provided with a level-shift circuit inside the IC circuit. It can also drive the XGA/SXGA, and SXGA+ panel.

FEATURES

- CMOS level input (3.3 V/2.5 V)
- 256/263 outputs
- High-output voltage (V_{DD2} to V_{EE2} = amplitude: 40 V MAX.)
- Capable of All-on outputting (/AO)

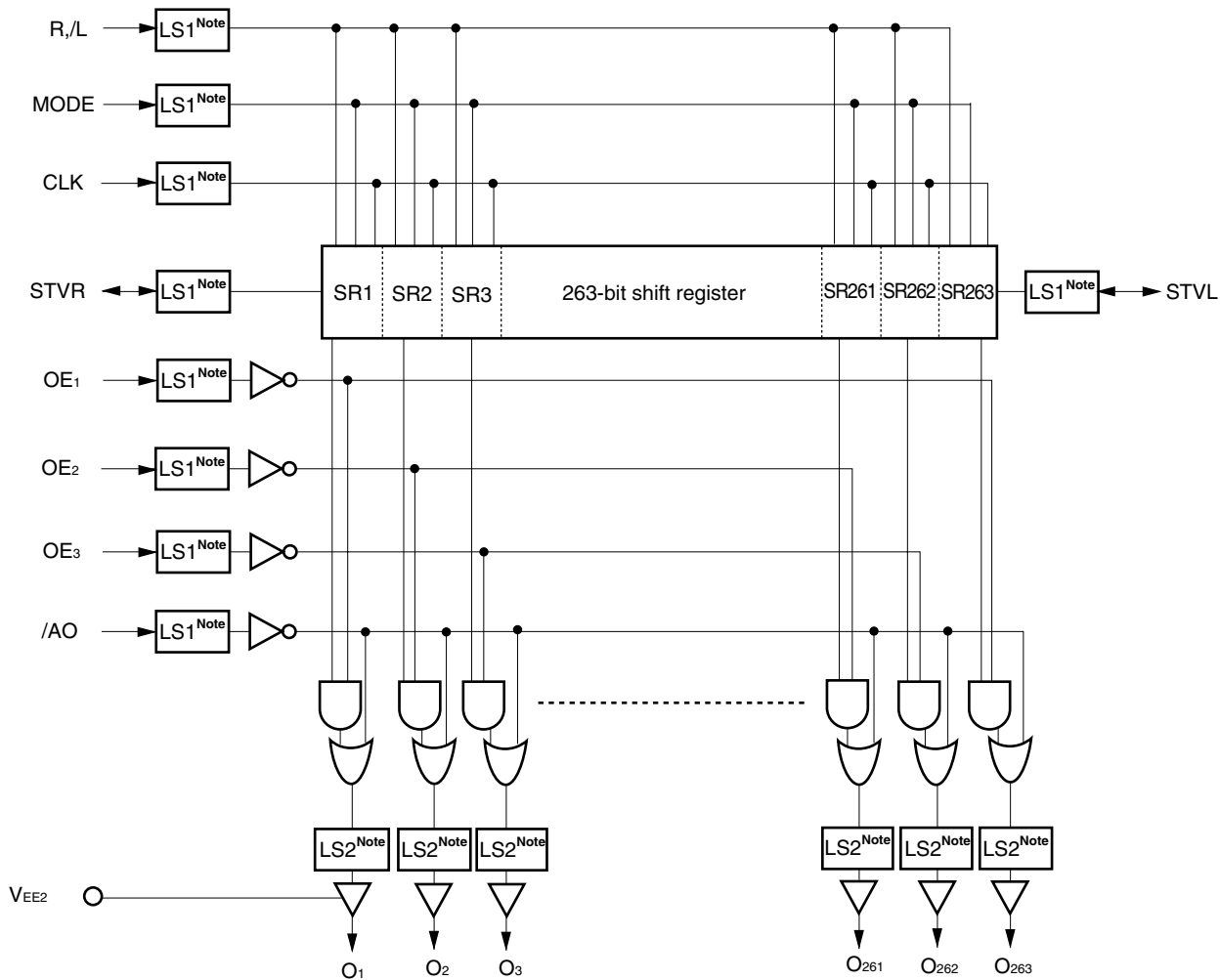
ORDERING INFORMATION

Part Number	Package
μ PD16702N-xxx	TCP (TAB package)

Remark The TCP's external shape is customized. To order the required shape, please contact one of our sales representatives.

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.
 Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

★ 1. BLOCK DIAGRAM

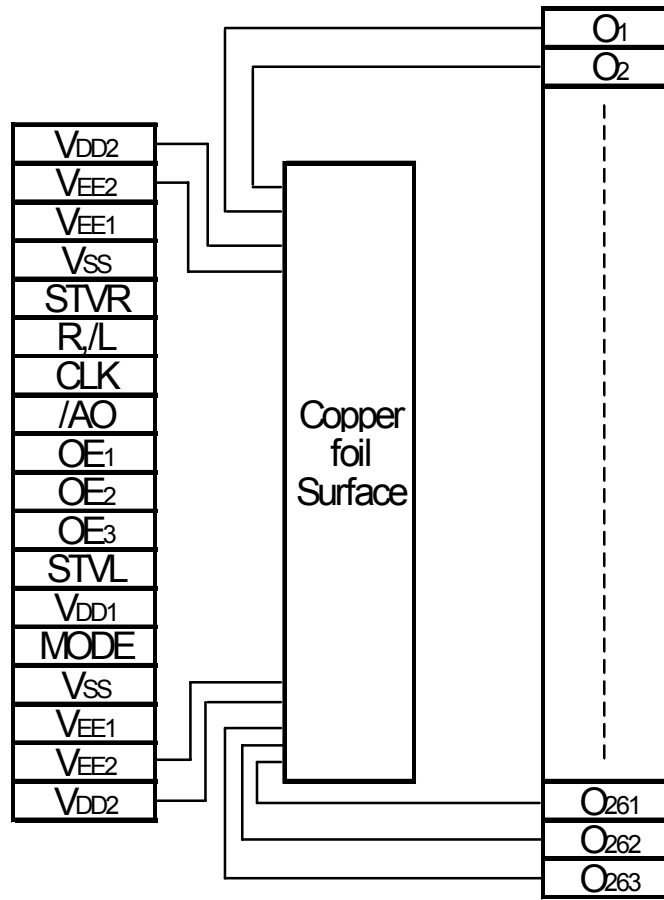


Note LS1: shifts CMOS level and internal level, LS2: shifts interval level and output level (V_{DD2} to V_{EE2}).

Remark /xxx indicates active low signal.

★ 2. PIN CONFIGURATION (Top of copper foil surface, Face-up)

μ PD16702N-xxx: TCP (TAB package)

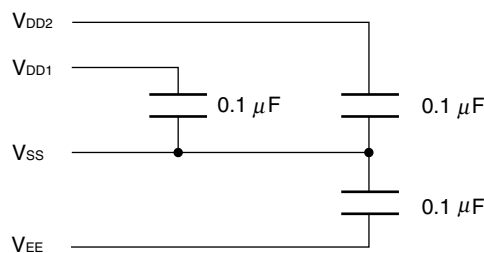


Remark This figure does not specify the TCP package.

★ 3. PIN FUNCTIONS

Pin Symbol	Pin Name	I/O	Description
O ₁ to O ₂₆₃	Driver output	Output	These pins output scan signals that drive the vertical direction (gate lines) of a TFT-LCD. The output signals change in synchronization with the rising edge of shift clock CLK. The driver output amplitude is V _{DD2} to V _{EE2} .
R,/L	Shift direction select input	Input	R,/L = H (right shift): STVR → O ₁ → O ₂₆₃ → STVL R,/L = L (left shift): STVL → O ₂₆₃ → O ₁ → STVR
STVR, STVL	Start pulse input/output	I/O	This is the input of the internal shift register. The start pulse is read at the rising edge of shift clock CLK, and scan signals are output from the driver output pins. The input level is a V _{DD1} to V _{SS} (logic level). When in MODE = H, the start pulse is output at the falling edge of the 263rd clock of shift clock CLK, and is cleared at the falling edge of the 264th clock. The output level is V _{DD1} to V _{SS} (logic level).
CLK	Shift clock input	Input	This pin inputs a shift clock to the internal shift register. The shift operation is performed in synchronization with the rising edge of this input.
OE ₁ , OE ₂ , OE ₃	Output enable input	Input	When this pin goes high level, the driver output is fixed to V _{EE2} level. The shift register is not cleared. CLK is asynchronous in the clock. Note that the output terminal which can be controlled by the enable signal changes refers to 4. RELATIONS OF ENABLE INPUT AND OUTPUT TERMINAL.
/AO	All-on control	Input	When this pin goes low level, the driver output is fixed to V _{DD2} level. The shift register is not cleared. This pin has priority over OE ₁ to OE ₃ . This pin is pulled up to V _{DD1} power supply inside μ PD16702. CLK is asynchronous in the clock.
MODE	Selection of Number of outputs	Input	MODE = V _{DD1} or open: 263 outputs MODE = V _{SS} : 256 outputs (Outputs pins O ₁₂₉ to O ₁₃₅ are invalid in 256-output mode.) Input level is V _{DD1} to V _{SS} (logic level) This pin is pulled up to V _{DD1} power supply inside μ PD16702.
V _{DD1}	Logic power supply	–	2.3 to 3.6 V
V _{DD2}	Driver positive power supply	–	15 to 25 V The driver output: high level
V _{SS}	Logic ground	–	Connect this pin to the ground of the system.
V _{EE1}	Negative Power supply for internal operation	–	–15 to –5 V
V _{EE2}	Driver negative power supply	–	The driver output: low level (V _{EE2} to V _{EE1} < 6.0 V)

- Cautions**
1. To prevent latch-up, turn on power to V_{DD1}, V_{EE1/2}, V_{DD2}, and logic input in this order. Turn off power in the reverse order. These power up/down sequence must be observed also during transition period.
 2. Insert a capacitor of about 0.1 μF between each power line, as shown below, to secure noise margin such as V_{IH} and V_{IL}.



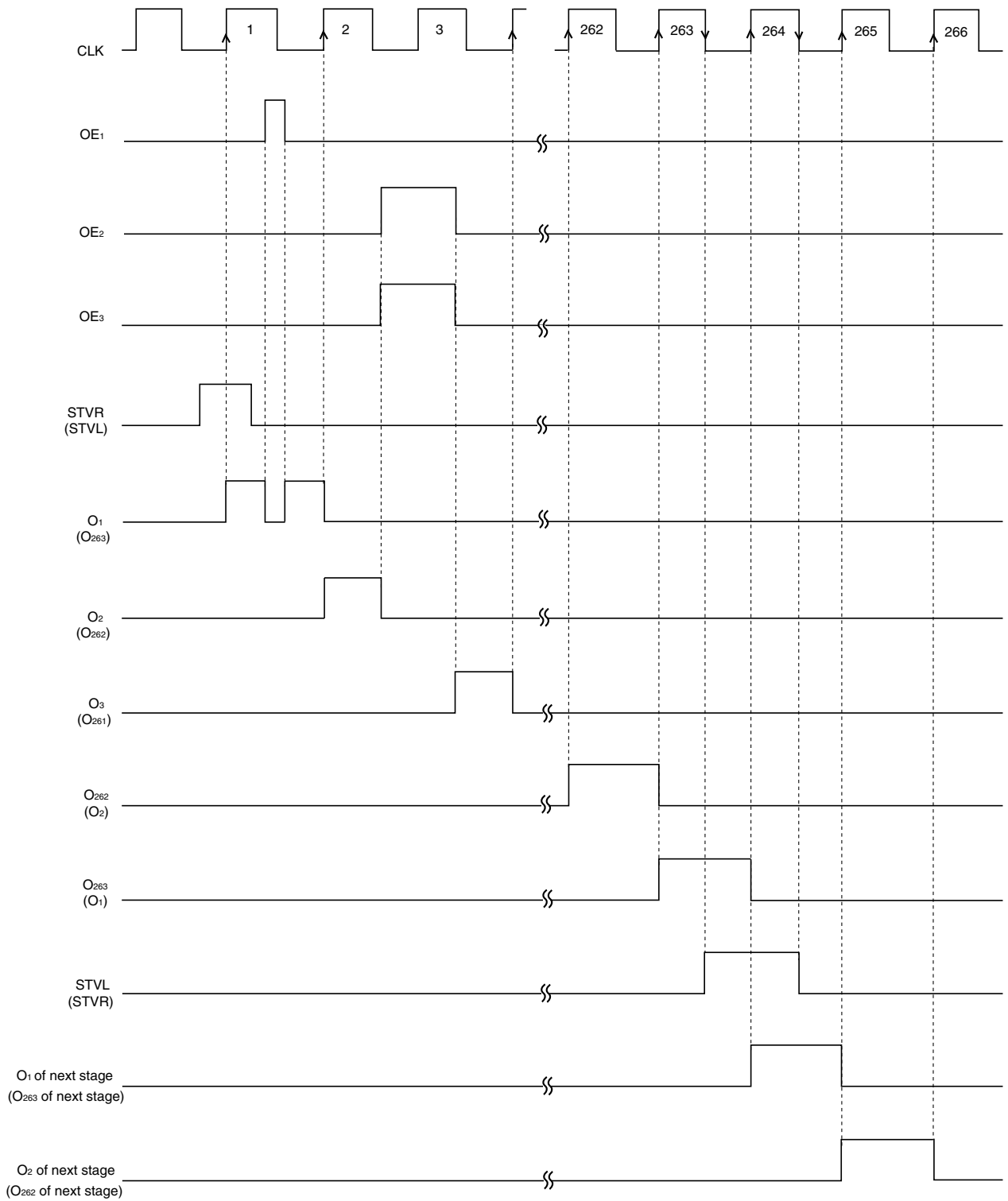
★ 4. RELATIONS OF ENABLE INPUT AND OUTPUT TERMINAL

Switching is possible for 263/256 with μ PD16702 by the MODE pin. And, the output terminal which can be controlled by the enable signal changes as follows along with this function.

263 Output TCP		256 Output TCP	
263 Output Mode (MODE = H)	256 Output Mode (MODE = L)	263 Output Mode (MODE = H)	256 Output Mode (MODE = L)
O ₁ (OE ₁)	O ₁ (OE ₁)	O ₁ (OE ₁)	O ₁ (OE ₁)
O ₂ (OE ₂)	O ₂ (OE ₂)	O ₂ (OE ₂)	O ₂ (OE ₂)
O ₃ (OE ₃)	O ₃ (OE ₃)	O ₃ (OE ₃)	O ₃ (OE ₃)
O ₄ (OE ₁)	O ₄ (OE ₁)	O ₄ (OE ₁)	O ₄ (OE ₁)
O ₅ (OE ₂)	O ₅ (OE ₂)	O ₅ (OE ₂)	O ₅ (OE ₂)
O ₆ (OE ₃)	O ₆ (OE ₃)	O ₆ (OE ₃)	O ₆ (OE ₃)
↓	↓	↓	↓
O ₁₂₇ (OE ₁)	O ₁₂₇ (OE ₁)	O ₁₂₇ (OE ₁)	O ₁₂₇ (OE ₁)
O ₁₂₈ (OE ₂)	O ₁₂₈ (OE ₂)	O ₁₂₈ (OE ₂)	O ₁₂₈ (OE ₂)
O ₁₂₉ (OE ₃)	V _X = V _{EE2}		
O ₁₃₀ (OE ₁)	V _X = V _{EE2}		
O ₁₃₁ (OE ₂)	V _X = V _{EE2}		
O ₁₃₂ (OE ₃)	V _X = V _{EE2}		
O ₁₃₃ (OE ₁)	V _X = V _{EE2}		
O ₁₃₄ (OE ₂)	V _X = V _{EE2}		
O ₁₃₅ (OE ₃)	V _X = V _{EE2}		
O ₁₃₆ (OE ₁)	O ₁₃₆ (OE ₃)	O ₁₃₆ (OE ₁)	O ₁₃₆ (OE ₃)
O ₁₃₇ (OE ₂)	O ₁₃₇ (OE ₁)	O ₁₃₇ (OE ₂)	O ₁₃₇ (OE ₁)
↓	↓	↓	↓
O ₂₅₉ (OE ₁)	O ₂₅₉ (OE ₃)	O ₂₅₉ (OE ₁)	O ₂₅₉ (OE ₃)
O ₂₆₀ (OE ₂)	O ₂₆₀ (OE ₁)	O ₂₆₀ (OE ₂)	O ₂₆₀ (OE ₁)
O ₂₆₁ (OE ₃)	O ₂₆₁ (OE ₂)	O ₂₆₁ (OE ₃)	O ₂₆₁ (OE ₂)
O ₂₆₂ (OE ₁)	O ₂₆₂ (OE ₃)	O ₂₆₂ (OE ₁)	O ₂₆₂ (OE ₃)
O ₂₆₃ (OE ₂)	O ₂₆₃ (OE ₁)	O ₂₆₃ (OE ₂)	O ₂₆₃ (OE ₁)

Remark V_X is power-supply voltage of output pin O₁ to O₂₆₃.

5. TIMING CHART (R,/L = H, /AO = H, MODE = H)



6. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C, V_{SS} = 0 V)

Parameter	Symbol	Rating	Unit
Logic Supply Voltage	V _{DD1}	-0.5 to +7.0	V
Driver Positive Supply Voltage	V _{DD2}	-0.5 to +28	V
Power Supply Voltage	V _{DD2} to V _{EE1} , V _{EE2}	-0.5 to +42	V
Internal Operation Negative Supply Voltage	V _{EE1}	-16 to +0.5	V
Driver Negative Supply Voltage	V _{EE2}	V _{EE1} - 0.3 to V _{EE1} + 7.0	V
Input Voltage	V _I	-0.5 to V _{DD1} + 0.5	V
Operating Ambient Temperature	T _A	-20 to +75	°C
Storage Temperature	T _{stg}	-55 to +125	°C

Caution Product qualify may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Range (T_A = -20 to +75°C, V_{SS} = 0 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Logic Supply Voltage	V _{DD1}	2.3	3.3	3.6	V
Driver Positive Supply Voltage	V _{DD2}	15	23	25	V
Internal Operation Negative Supply Voltage	V _{EE1}	-15	-10	-5.0	V
Power Supply Voltage	V _{DD2} to V _{EE1}	20	33	40	V
	V _{EE2} to V _{EE1}	0		6.0	V
Clock Frequency	f _{CLK}			100	kHz

Electrical Characteristics (T_A = -20 to +75°C, V_{DD1} = 2.3 to 3.6 V, V_{DD2} = 23 V, V_{EE1} = V_{EE2} = -10 V, V_{SS} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High-level Input Voltage	V _{IH}	CLK, STVR (STVL), R _i /L _i ,	0.8 V _{DD1}		V _{DD1}	V
Low-level Input Voltage	V _{IL}	OE ₁ to OE ₃	V _{SS}		0.2 V _{DD1}	V
High-level Output Voltage	V _{OH}	STVR (STVL), I _{OH} = -40 μA	V _{DD1} - 0.4		V _{DD1}	V
Low-level Output Voltage	V _{OL}	STVR (STVL), I _{OL} = +40 μA	V _{SS}		V _{SS} + 0.4	V
LCD Driver Output ON Resistance	R _{ON}	V _{OUT} = V _{EE2} + 1.0 V, or V _{DD2} - 1.0 V			1.0	kΩ
Pull-up Resistance	R _{PU}	V _{DD1} = 3.3 V, /AO, MODE	15	35	80	kΩ
Input Leak Current	I _{IL}	V _i = 0 V or 3.6 V, except for /AO, MODE			±1.0	μA
Static Current Dissipation	I _{DD1}	V _{DD1} , f _{CLK} = 50 kHz, OE ₁ = OE ₂ = OE ₃ = L, f _{STV} = 60 Hz, no load		550 ^{Note}	1000	μA
	I _{DD2}	V _{DD2} , f _{CLK} = 50 kHz, OE ₁ = OE ₂ = OE ₃ = L, f _{STV} = 60 Hz, no load		10 ^{Note}	100	μA
	I _{EE}	V _{EE1} , f _{CLK} = 50 kHz, OE ₁ = OE ₂ = OE ₃ = L, f _{STV} = 60 Hz, no load	-1100	-550 ^{Note}		μA

Remark STV: STVR (STVL)

Note The TYP. values refer to V_{DD1} = 3.3 V, T_A = 25°C.

Switching Characteristics (T_A = -20 to +75°C, V_{DD1} = 2.3 to 3.6 V, V_{DD2} = 23 V, V_{EE1} = V_{EE2} = -10 V, V_{SS} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Cascade Output Delay Time	t _{PHL1}	C _L = 20 pF, CLK → STVL (STVR)			800	ns
	t _{PLH1}				800	ns
Driver Output Delay Time	t _{PHL2}	C _L = 300 pF, CLK → O _n			800	ns
	t _{PLH2}				800	ns
	t _{PHL3}	C _L = 300 pF, OE _n → O _n			800	ns
	t _{PLH3}				800	ns
Output Rise Time	t _{TLH}	C _L = 300 pF			350	ns
Output Fall Time	t _{THL}				350	ns
Input Capacitance	C _i	T _A = 25°C			15	pF

Timing Requirements (T_A = -20 to +75°C, V_{DD1} = 2.3 to 3.6 V, V_{DD2} = 23 V, V_{EE1} = V_{EE2} = -10 V, V_{SS} = 0 V)

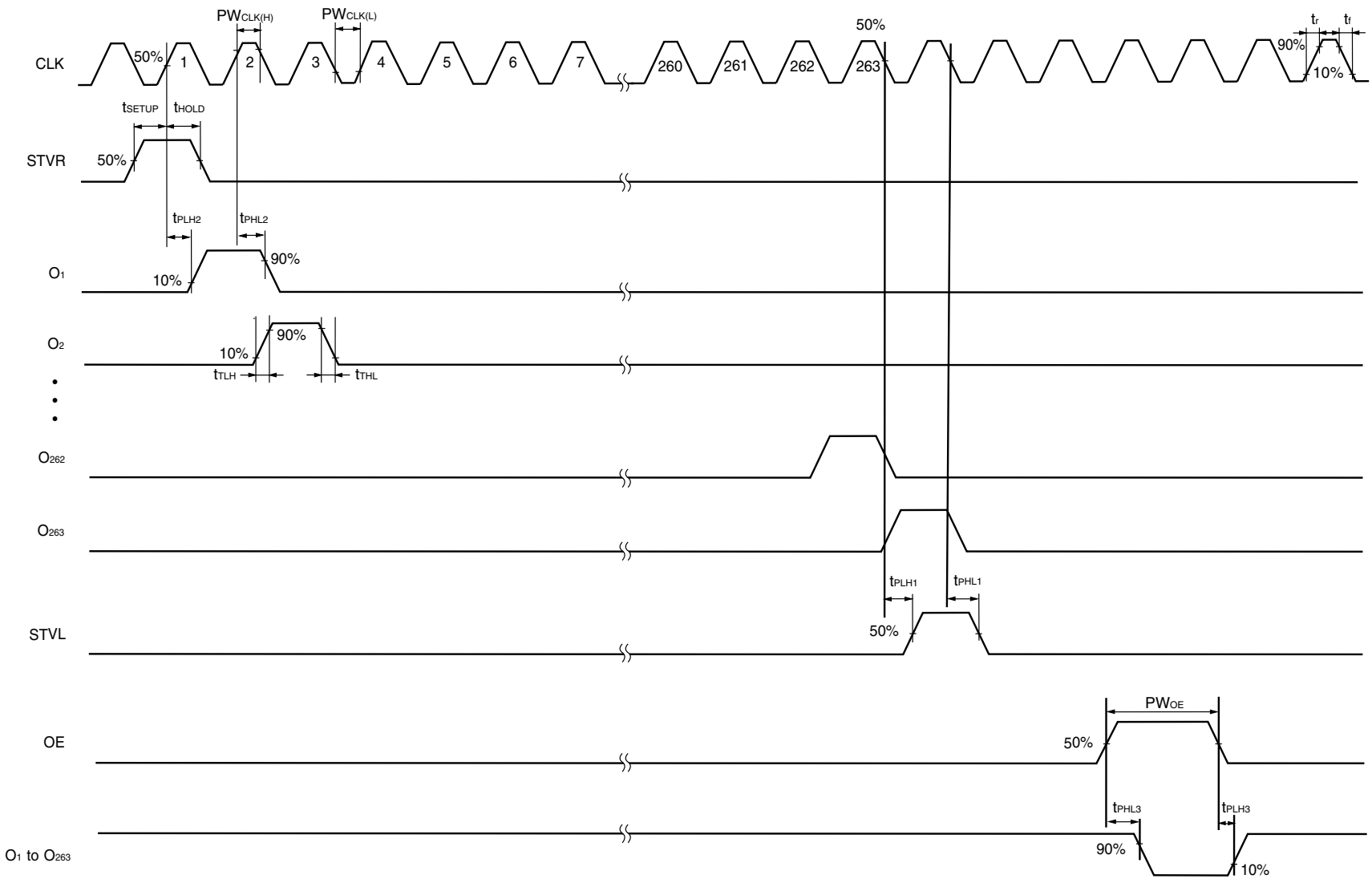
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock Pulse High Width	PW _{CLK(H)}		500			ns
Clock Pulse Low Width	PW _{CLK(L)}		500			ns
★ Enable Pulse Width	PW _{OE}		1000			ns
Data Setup Time	t _{SETUP}	STVR (STVL) ↑ → CLK ↑	200			ns
Data Hold Time	t _{HOLD}	CLK ↑ → STVR (STVL) ↓	200			ns

Remark Unless otherwise specified, the input level is defined to be V_{IH} = 0.8 V_{DD1}, V_{IL} = 0.2 V_{DD1}.

Caution Keep the time and fall time of the logic input to t_r = t_f = 20 ns (10 to 90% of the rated values).

Switching Characteristics Waveform (R_I/L=H, MODE = H)

Unless otherwise specified, the input level is defined to be V_{IH} = 0.8 V_{DD1}, V_{IL} = 0.2 V_{DD1}.



7. RECOMMENDED MOUNTING CONDITIONS

The following conditions must be met for mounting conditions of the μ PD16702.

For more details, refer to the **Semiconductor Device Mounting Technology Manual (C10535E)**.

Please consult with our sales offices in case other mounting process is used, or in case the mounting is done under different conditions.

μ PD16702N-xxx: TCP (TAB Package)

Mounting Condition	Mounting Method	Condition
Thermocompression	Soldering	Heating tool 300 to 350°C, heating for 2 to 3 seconds : pressure 100g (per solder)
	ACF (Adhesive Conductive Film)	Temporary bonding 70 to 100°C: pressure 3 to 8 kg/cm ² : time 3 to 5 sec. Real bonding 165 to 180°C: pressure 25 to 45 kg/cm ² : time 30 to 40 sec. (When using the anisotropy conductive film SUMIZAC1003 of Sumitomo Bakelite,Ltd).

Caution To find out the detailed conditions for mounting the ACF part, please contact the ACF manufacturing company. Be sure to avoid using two or more mounting methods at a time.

[MEMO]

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES**① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Reference Documents

NEC Semiconductor Device Reliability/Quality Control System (C10983E)

Quality Grades On NEC Semiconductor Devices (C11531E)

- **The information in this document is current as of September, 2001. The information is subject to change without notice. For actual design-in, refer to the latest publications of NEC's data sheets or data books, etc., for the most up-to-date specifications of NEC semiconductor products. Not all products and/or types are available in every country. Please check with an NEC sales representative for availability and additional information.**
 - No part of this document may be copied or reproduced in any form or by any means without prior written consent of NEC. NEC assumes no responsibility for any errors that may appear in this document.
 - NEC does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from the use of NEC semiconductor products listed in this document or any other liability arising from the use of such products. No license, express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC or others.
 - Descriptions of circuits, software and other related information in this document are provided for illustrative purposes in semiconductor product operation and application examples. The incorporation of these circuits, software and information in the design of customer's equipment shall be done under the full responsibility of customer. NEC assumes no responsibility for any losses incurred by customers or third parties arising from the use of these circuits, software and information.
 - While NEC endeavours to enhance the quality, reliability and safety of NEC semiconductor products, customers agree and acknowledge that the possibility of defects thereof cannot be eliminated entirely. To minimize risks of damage to property or injury (including death) to persons arising from defects in NEC semiconductor products, customers must incorporate sufficient safety measures in their design, such as redundancy, fire-containment, and anti-failure features.
 - NEC semiconductor products are classified into the following three quality grades:
 "Standard", "Special" and "Specific". The "Specific" quality grade applies only to semiconductor products developed based on a customer-designated "quality assurance program" for a specific application. The recommended applications of a semiconductor product depend on its quality grade, as indicated below. Customers must check the quality grade of each semiconductor product before using it in a particular application.
 "Standard": Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots
 "Special": Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
 "Specific": Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems and medical equipment for life support, etc.
- The quality grade of NEC semiconductor products is "Standard" unless otherwise expressly specified in NEC's data sheets or data books, etc. If customers wish to use NEC semiconductor products in applications not intended by NEC, they must contact an NEC sales representative in advance to determine NEC's willingness to support a given application.
- (Note)
- (1) "NEC" as used in this statement means NEC Corporation and also includes its majority-owned subsidiaries.
 - (2) "NEC semiconductor products" means any semiconductor product developed or manufactured by or for NEC (as defined above).