DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD6222

I²C-BUS COMPATIBLE 8BIT 12CHANNEL D/A CONVERTER

DESCRIPTION

The μPD6222 is an 8-bit monolithic CMOS digital-to-analog converter using the R-2R technique. The μPD6222 incorporates a 12-channel digital-to-analog converters and I²C-bus compatible interface. The designer needs only 2 signals (Serial Data and Serial Clock) to interface and can use 8-ICs (96-channels) on same bus to control chip-select terminals.

The μPD6222 incorporates Output CMOS Buffer to achieve wide output voltage range and two reference voltage terminals.

The μPD6222 is ideal for automatic control for color-television.

FEATURES

- 12-channel 8-bit digital-to-analog converter using the R-2R ladder technique
- I²C-bus compatible serial interface (Serial Data and Serial Clock)
- 8-ICs (96-channels) can be connected by chip-select terminals
- Output CMOS Buffer to achieve wide output voltage range
- Two reference voltage

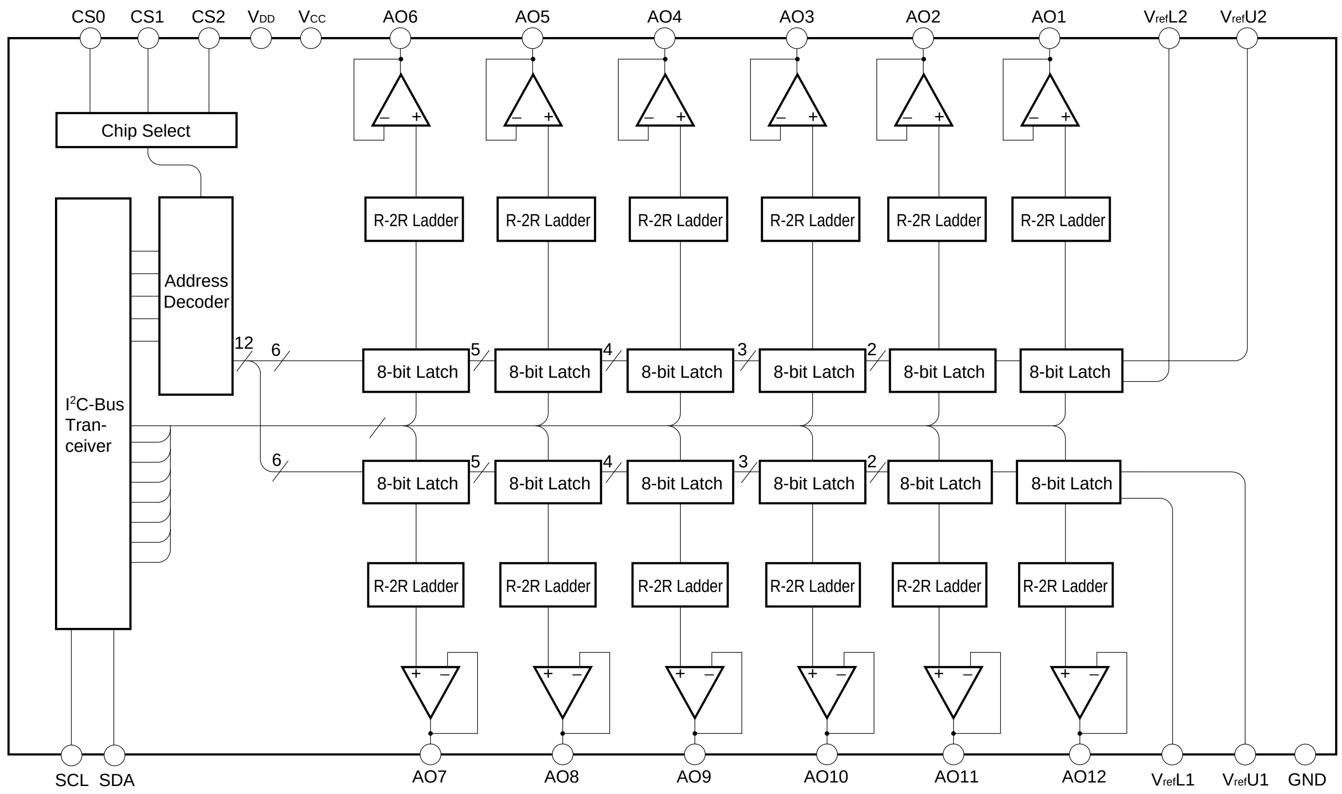
ORDERING INFORMATION

PART NO.	PACKAGE
μPD6222CS	24-pin plastic shrink DIP (300 mil)
μPD6222GS	24-pin plastic SOP (300 mil)

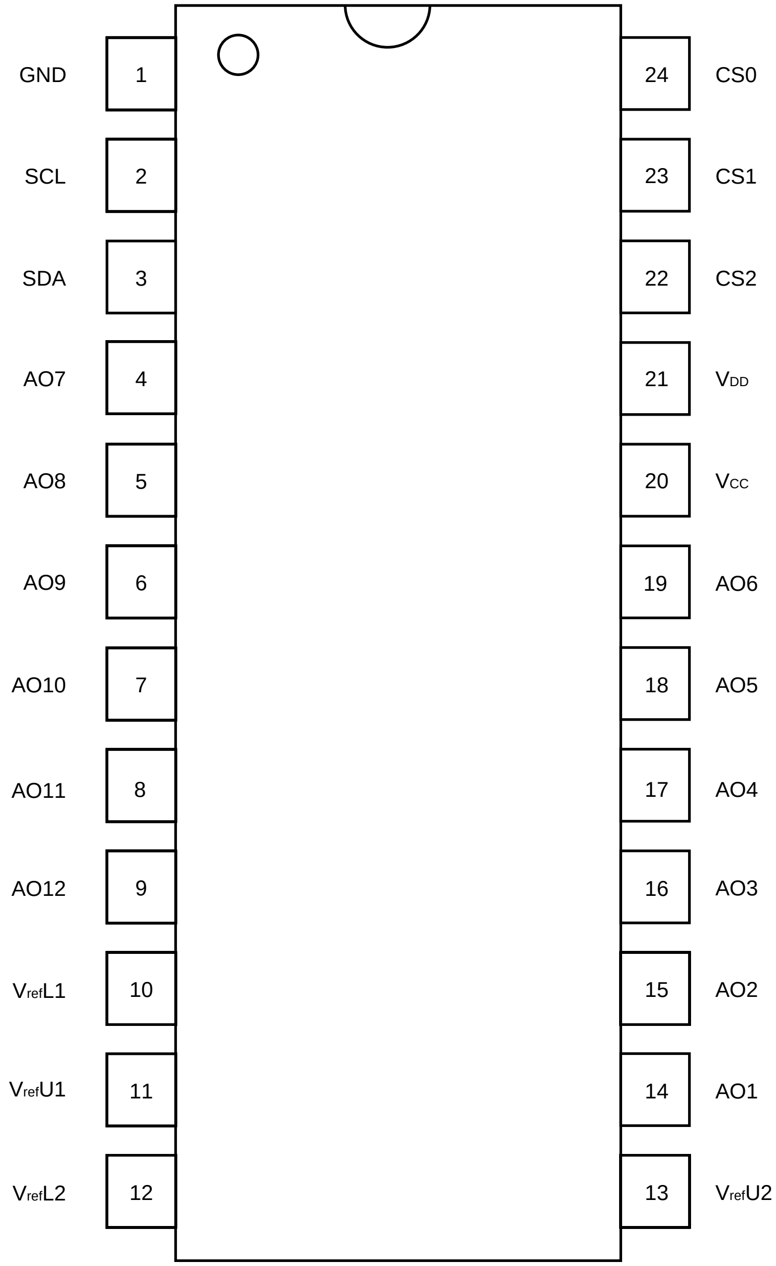
Caution Purchase of NEC I²C components conveys a license under the Philips I²C patent Right to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

Document No. S11067EJ2V0DS00 (2nd edition)
Date Published November 1998 N CP(K)
Printed in Japan

BLOCK DIAGRAM



PIN CONNECTION DIAGRAM (Top View)



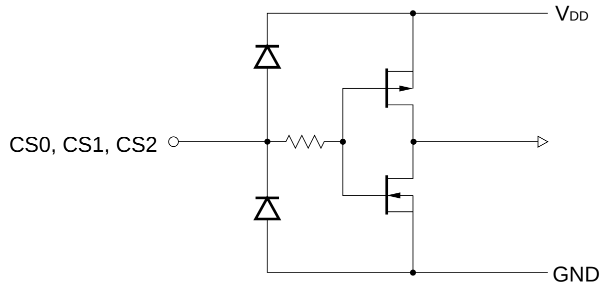
PIN CONFIGURATION

PIN NO.	SYMBOL	FUNCTION
1	GND	Ground
2	SCL	Serial Clock Input
3	SDA	Serial Data Input (Output: acknowledgement signal)
4	AO7	Analog Output Channel 7
5	AO8	Analog Output Channel 8
6	AO9	Analog Output Channel 9
7	AO10	Analog Output Channel 10
8	AO11	Analog Output Channel 11
9	AO12	Analog Output Channel 12
10	$V_{ref}L1$	GND Side Reference Voltage Input 1 (The current of $I_{ref}L1$ flows out from IC.)
11	$V_{ref}U1$	V_{CC} Side Reference Voltage Input 1 (The current of $I_{ref}U1$ flows into IC.)
12	$V_{ref}L2$	GND Side Reference Voltage Input 2 (The current of $I_{ref}L2$ flows out from IC.)
13	$V_{ref}U2$	V_{CC} Side Reference Voltage Input 2 (The current of $I_{ref}U2$ flows into IC.)
14	AO1	Analog Output Channel 1
15	AO2	Analog Output Channel 2
16	AO3	Analog Output Channel 3
17	AO4	Analog Output Channel 4
18	AO5	Analog Output Channel 5
19	AO6	Analog Output Channel 6
20	V_{CC}	Analog Power Supply
21	V_{DD}	Digital Power Supply
22	CS2	Chip Select 2
23	CS1	Chip Select 1
24	CS0	Chip Select 0

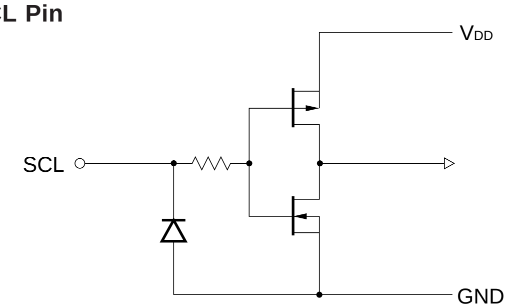
Note For “Power On Reset” function, when this IC is powered on, Analog Output Data (D0, D1 ··· D7) will be set all 0. And the all Analog Output will be Zero Scale (1LSB + $V_{ref}L$).

EQUIVALENT CIRCUIT OF PIN

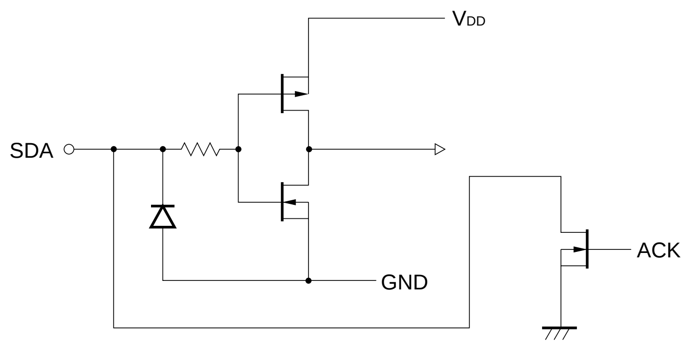
- **Equivalent Circuit of CS0, CS1, CS2 Pins**



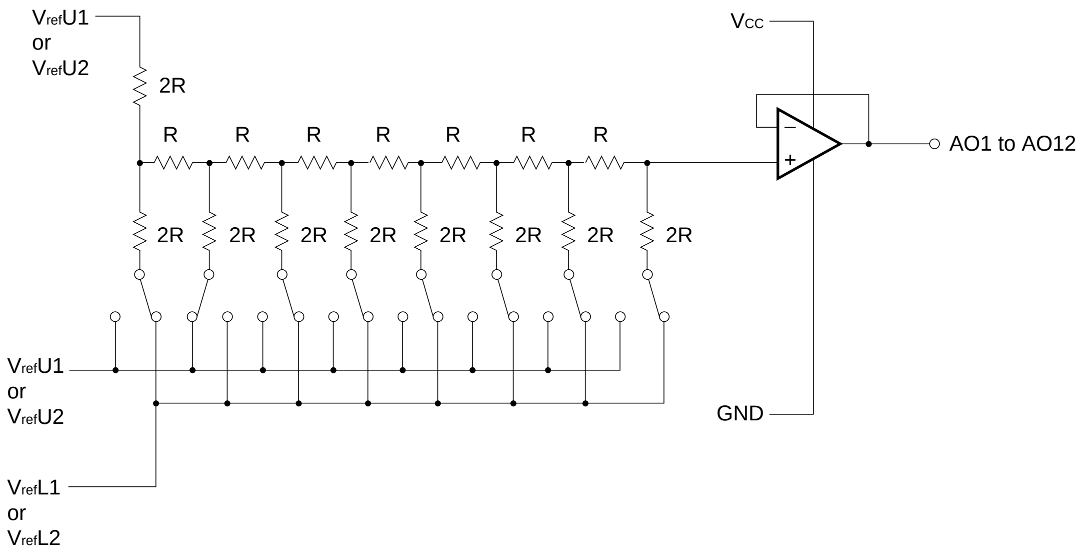
- **Equivalent Circuit of SCL Pin**



- **Equivalent Circuit of SDA Pin**



- **Equivalent Circuit of V_{ref}U1, V_{ref}U2, V_{ref}L1, V_{ref}L2 and AO1 to 12 Pins**



ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL	LIMITS	UNIT
Digital Supply Voltage		V_{DD}	–0.3 to +7.0	V
Analog Supply Voltage		V_{CC}	–0.3 to V_{DD} + 0.3	V
V_{CC} Side Reference Voltage		V_{ref}U1, U2	–0.3 to V_{CC} + 0.3	V
GND Side Reference Voltage		V_{ref}L1, L2	–0.3 to V_{CC} + 0.3	V
Digital Input Voltage		V_{IN}	–0.3 to V_{DD} + 0.3	V
Output Voltage		V_{OUT}	–0.3 to V_{CC} + 0.3	V
Power Dissipation	CS Package	P_D	500	mW
	GS Package		200	mW
Operating Temperature Range		T_A	–20 to +85	°C
Storage Temperature Range		T_{stg}	–55 to +125	°C

RECOMMENDED OPERATION CONDITIONS

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Digital Supply Voltage	V_{DD}	V_{DD} = V_{CC}	4.5	5.0	5.5	V
Analog Supply Voltage	V_{CC}					
Input Voltage of V_{CC} Side Reference Voltage Range	V_{ref}U1, U2	This parameter is not same as D/A output voltage. D/A output is defined by the ability of Output Buffer Amp.	V_{ref}L		V_{CC}	V
Input Voltage of GND Side Reference Voltage Range	V_{ref}L1, L2		GND		V_{ref}U	V
Output Capacitance Load	C_O				0.1	μF

ELECTRICAL CHARACTERISTICS
DIGITAL BLOCK
(V_{CC}, V_{DD}, V_{ref}U1, 2 = +4.5 to +5.5 V, V_{ref}U1, 2 ≤ V_{CC}, V_{ref}L1, 2 = GND = 0 V, T_A = –20 to +85 °C)

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Digital Supply Current	I_{DD}	CLK = 1 MHz, I_{AO} = 0 μA			1.0	mA
Input Leak Current	$I_{I\ LEAK}$	V_{IN} = 0 to V_{DD}	–10		10	μA
Low-Level Input Voltage	V_{IL}				0.2 V_{DD}	V
High-Level Input Voltage	V_{IH}		0.8 V_{DD}			V

ANALOG BLOCK
(V_{CC}, V_{DD}, $V_{ref}U1, 2$ = +4.5 to +5.5 V, $V_{ref}U1, 2 \leq V_{CC}$, $V_{ref}L1, 2$ = GND = 0 V, T_A = –20 to +85 °C)

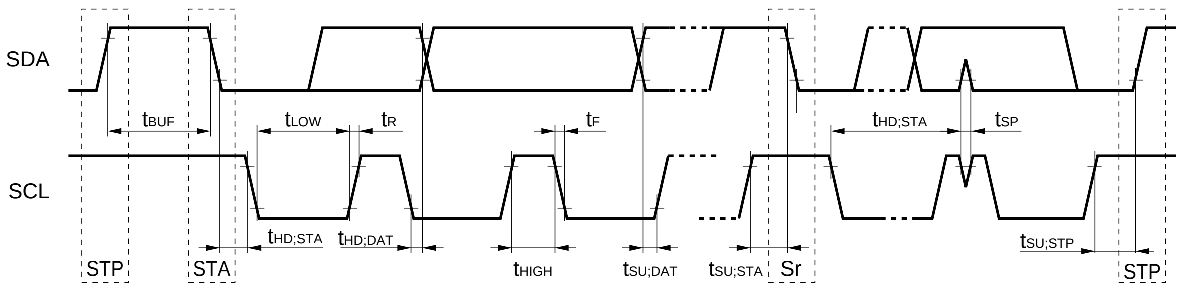
PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Analog Supply Current	I_{CC}	CLK = 1 MHz, I_{AO} = 0 μA		1.0	4.8	mA
Input Current of V_{CC} Side Reference Voltage	$I_{ref}U$	$V_{ref}U$ = 5 V, $V_{ref}L$ = 0 V, Data: Maximum Current		1.2	3.0	mA
Output Voltage Range of Output Buffer Amp.	V_{AO}	I_{AO} = ±100 μA	0.1		V_{CC} – 0.1	V
		I_{AO} = ±500 μA	0.2		V_{CC} – 0.2	
Output Current of Output Buffer Amp.	I_{AO}	V_{AO} = 4.7 V			–1.0	mA
		V_{AO} = 0.2 V	+1.0			
Differential Nonlinearity	N_{DL}	$V_{ref}U$ = 4.79 V $V_{ref}L$ = 0.95 V V_{CC} = 5.5 V (15 mV/LSB) No Load (I_{AO} = 0 A)			±0.8	LSB
Nonlinearity	N_L				±0.8	LSB
Zero Scale Error	N_Z				±1.2	LSB
Full Scale Error	N_F				±1.2	LSB
Error between each Channel	N_{ch}				±1.2	LSB
Output Impedance of Output Buffer Amp.	R_O			5.0		Ω

I²C-BUS TRANSFER STANDARD

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
SCL clock frequency	f_{SCL}	0	100	kHz
Time the bus must be free before a new transmission can start	t_{BUF}	4.7	–	μs
Hold time START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	4.0	–	μs
LOW period of the clock	t_{LOW}	4.7	–	μs
HIGH period of the clock	t_{HIGH}	4.0	–	μs
Set-up time for START condition (Only relevant for a repeated START condition)	$t_{SU;STA}$	4.7	–	μs
Hold time DATA for I²C ICs	$t_{HD;DAT}$	0[Note]	–	ns
Set-up time DATA	$t_{SU;DAT}$	250	–	ns
Rise time of both SDA and SCL lines	t_R	–	1	μs
Fall time of both SDA and SCL lines	t_F	–	300	ns
Set-up time for STOP condition	$t_{SU;STP}$	4.0	–	μs

Note Note that a transmitter must internally provide at least a hold time to bridge the undefined region (max. 300 ns) of the falling edge of SCL.

Timing requirements for the I²C-bus



I^2C-BUS FORMAT

STA	SLAVE ADDRESS DATA	W	ACK	SUB ADDRESS DATA	ACK	D/A DATA	ACK	STP

- STA: START condition
- W : This bit is a data-transfer direction bit. A 'Zero' (LOW) is set at sending a data from master to slave.
- ACK: This is an acknowledge bit. The receiver responses a 'Zero' (LOW) to the transmitter when the receiver acknowledges data reception.
- STP: STOP condition

DIGITAL DATA FORMAT

- SLAVE ADDRESS DATA

First MSB — Last LSB

1	0	0	1	A2	A1	A0

Chip Select Data (A2, A1, A0)

- SUB ADDRESS DATA

First MSB — Last LSB

×	×	×	×	S3	S2	S1	S0

Don't care (×) — Channel Select Data (S3–S0)

Chip Select Data

MSB LSB

A2	A1	A0	CS2	CS1	CS0
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	1

This chip will be selected only when A0, A1 and A2 are equal to CS0, CS1 and CS2.

Channel Select Data

MSB LSB

S3	S2	S1	S0	Channel Select
0	0	0	0	Don't care
0	0	0	1	ch1
0	0	1	0	ch2
⋮	⋮	⋮	⋮	⋮
1	0	1	1	ch11
1	1	0	0	ch12
1	1	0	1	Don't care
1	1	1	0	
1	1	1	1	Inhibit[Note]

Note Internally Test Mode

- D/A DATA

First MSB — Last LSB

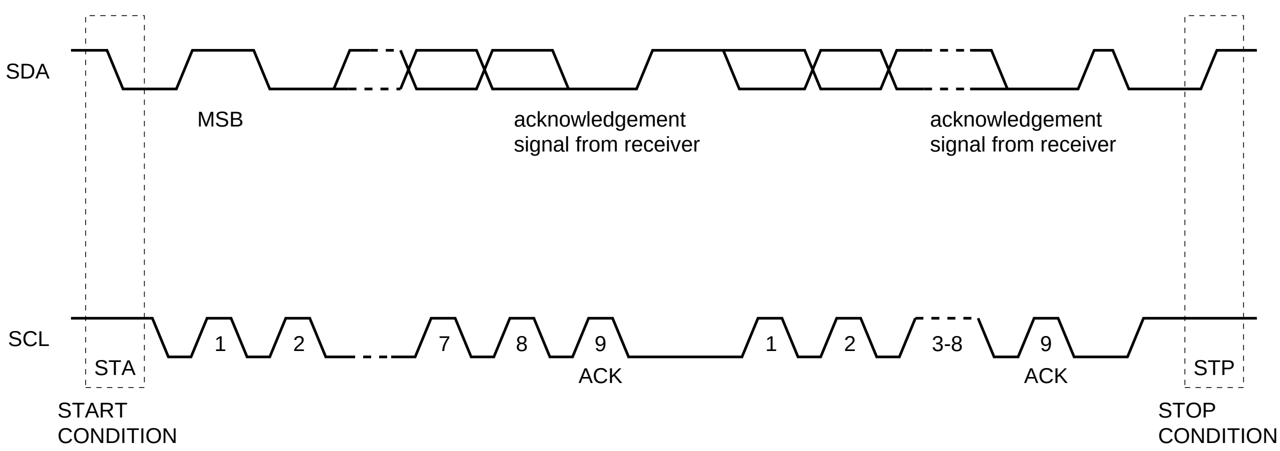
D7	D6	D5	D4	D3	D2	D1	D0

D/A Output Data

First MSB — Last LSB

D7	D6	D5	D4	D3	D2	D1	D0	D/A OUTPUT
0	0	0	0	0	0	0	0	$(V_{ref}U - V_{ref}L) / 256 \times 1 + V_{ref}L$
0	0	0	0	0	0	0	1	$(V_{ref}U - V_{ref}L) / 256 \times 2 + V_{ref}L$
0	0	0	0	0	0	1	0	$(V_{ref}U - V_{ref}L) / 256 \times 3 + V_{ref}L$
0	0	0	0	0	0	1	1	$(V_{ref}U - V_{ref}L) / 256 \times 4 + V_{ref}L$
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	1	1	0	$(V_{ref}U - V_{ref}L) / 256 \times 255 + V_{ref}L$
1	1	1	1	1	1	1	1	$V_{ref}U$

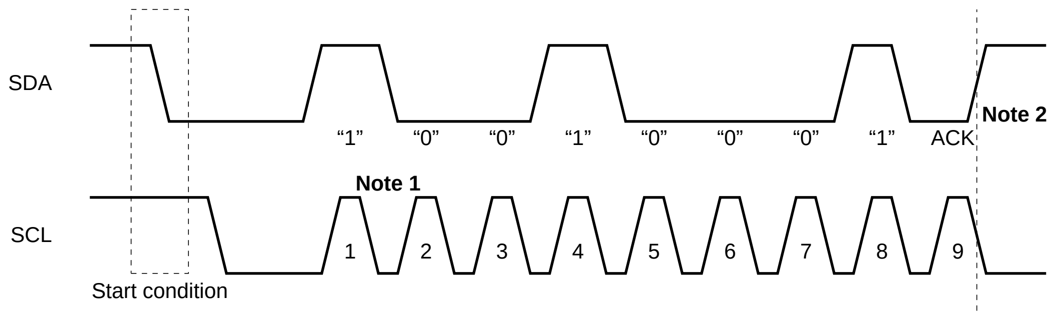
DATA TRANSFER ON THE I²C-BUS



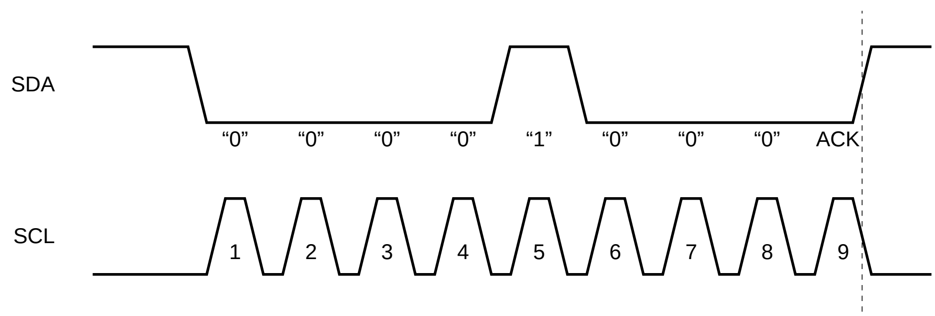
I²C BUS ACCESS

Data example; (CS2, CS1, CS0) = (A2, A1, A0) = (0, 0, 1)
(S3, S2, S1, S0) = (0, 1, 0, 0) Select output 4ch
Digital Data = (0, 1, 0, 1, 0, 1, 0, 1)

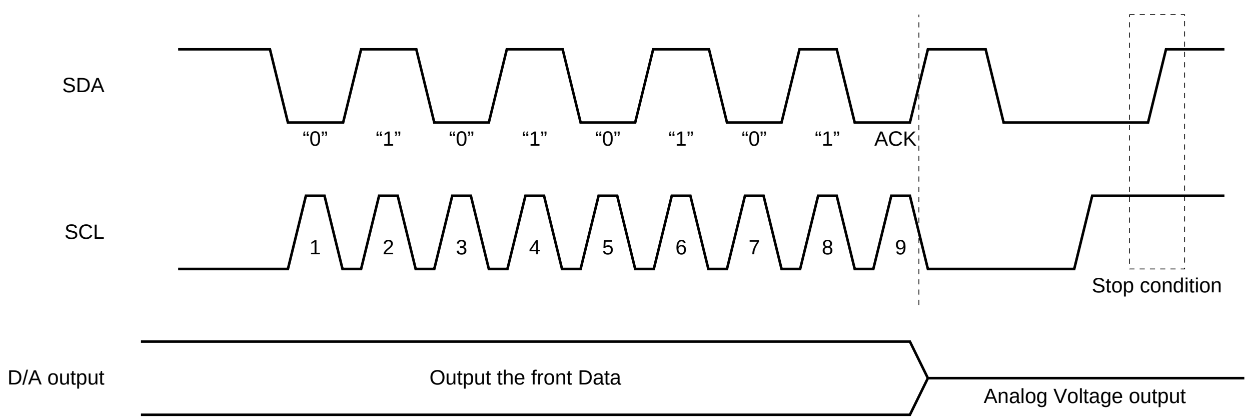
SLAVE ADDRESS DATA BLOCK



SUB ADDRESS DATA BLOCK



D/A DATA BLOCK

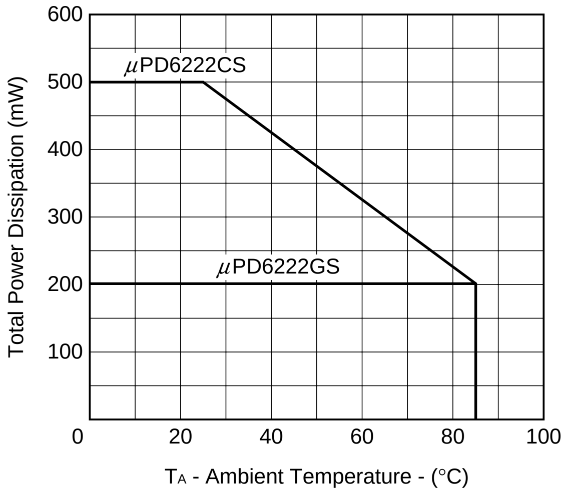


Notes 1. The timing of reading data in SDA is the falling edge of SCL.

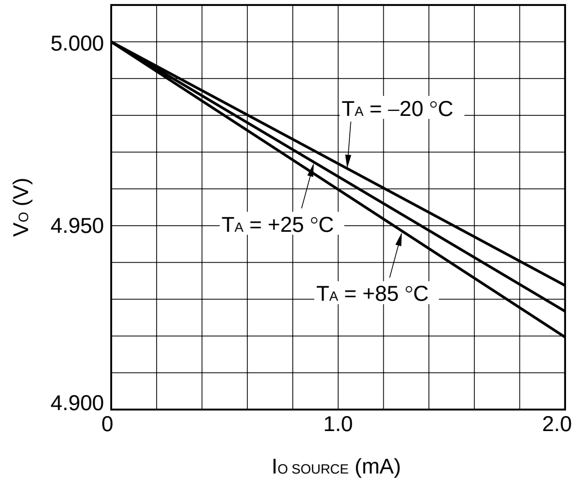
2. The acknowledgement signal is output from SDA in fall-timing of SCL8, and releases SDA line in the fall-timing of SCL9.

CHARACTERISTICS CURVES (TYP.)

P_T - T_A Characteristic (Absolute Maximum Rating)

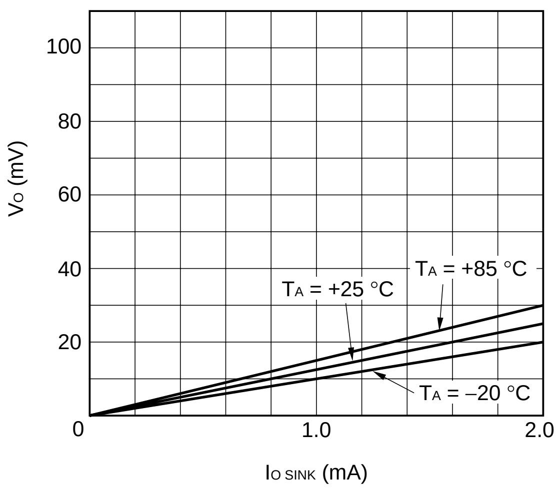


V_O - $I_{O\ SOURCE}$ Characteristic



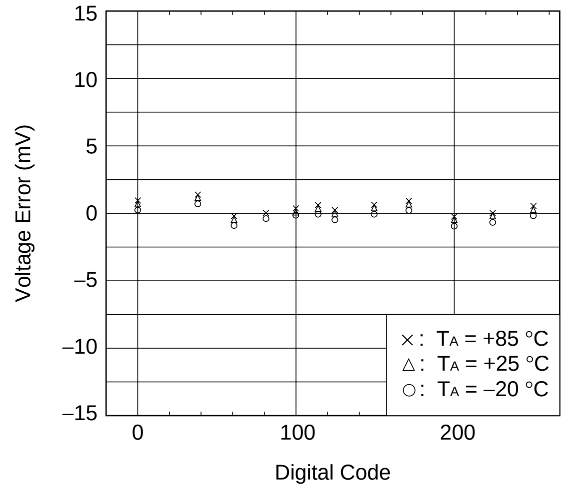
Condition:
V_{CC} = V_{ref}U = +5.0 V
V_{ref}L = 0 V
Non Load

V_O - $I_{O\ SINK}$ Characteristic



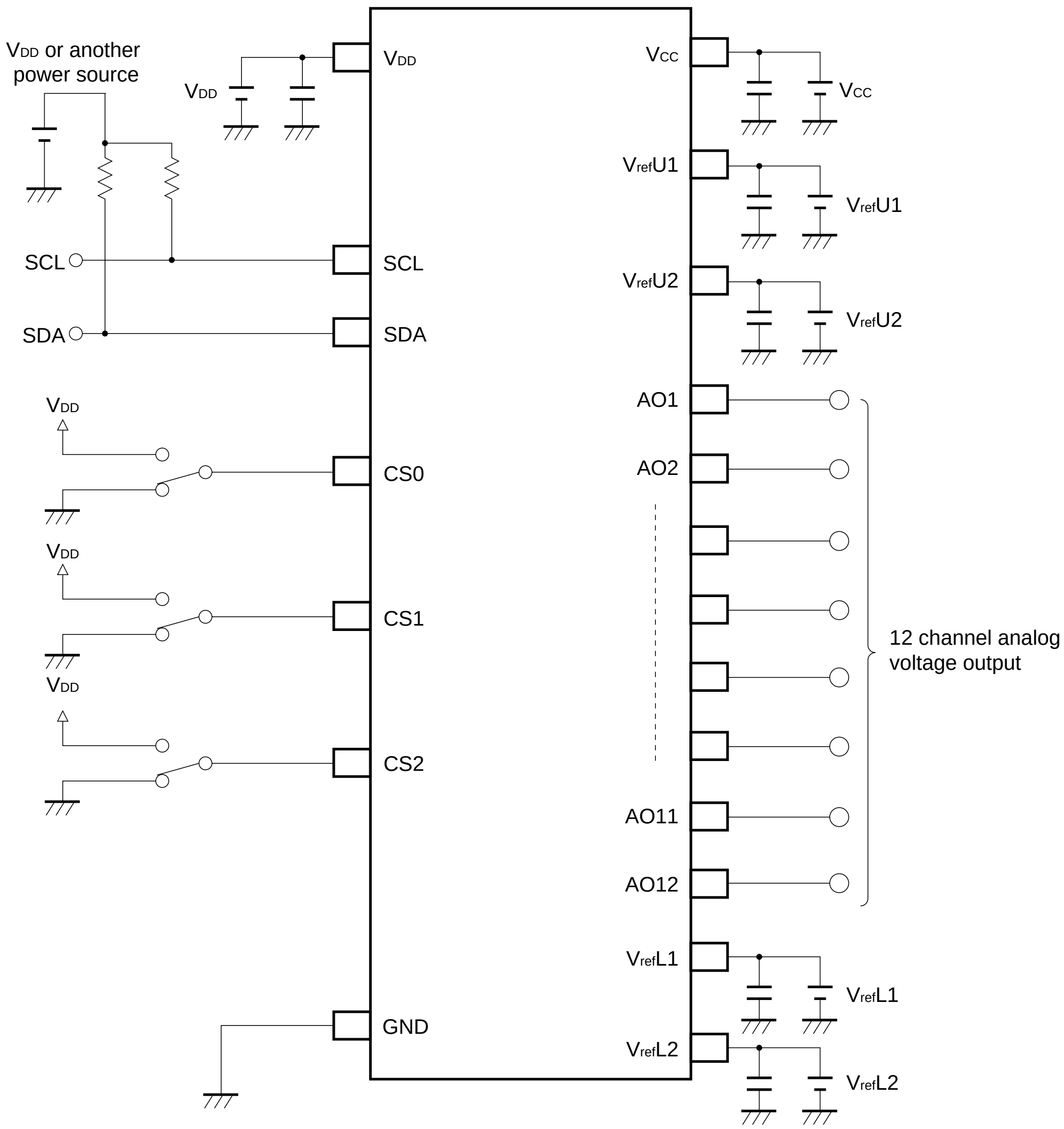
Condition:
V_{CC} = V_{ref}U = +5.0 V
V_{ref}L = 0 V
Non Load

Liniarity of D/A Output



Condition:
V_{CC} = +5.5 V
V_{ref}U = +4.79 V
V_{ref}L = +0.95 V (15 mV/LSB)
Non Load

APPLICATION EXAMPLE



NOTE FOR USE

- **ABOUT INPUT VOLTAGE**

  This IC's V_{DD}, V_{CC}, $V_{ref}U1$, $V_{ref}U2$, $V_{ref}L1$, $V_{ref}L2$ pins must be supplied the stable voltage. When the voltage-level of these pins are added any noise signal, the analog accuracy of output voltage may be influenced by any noise signal.

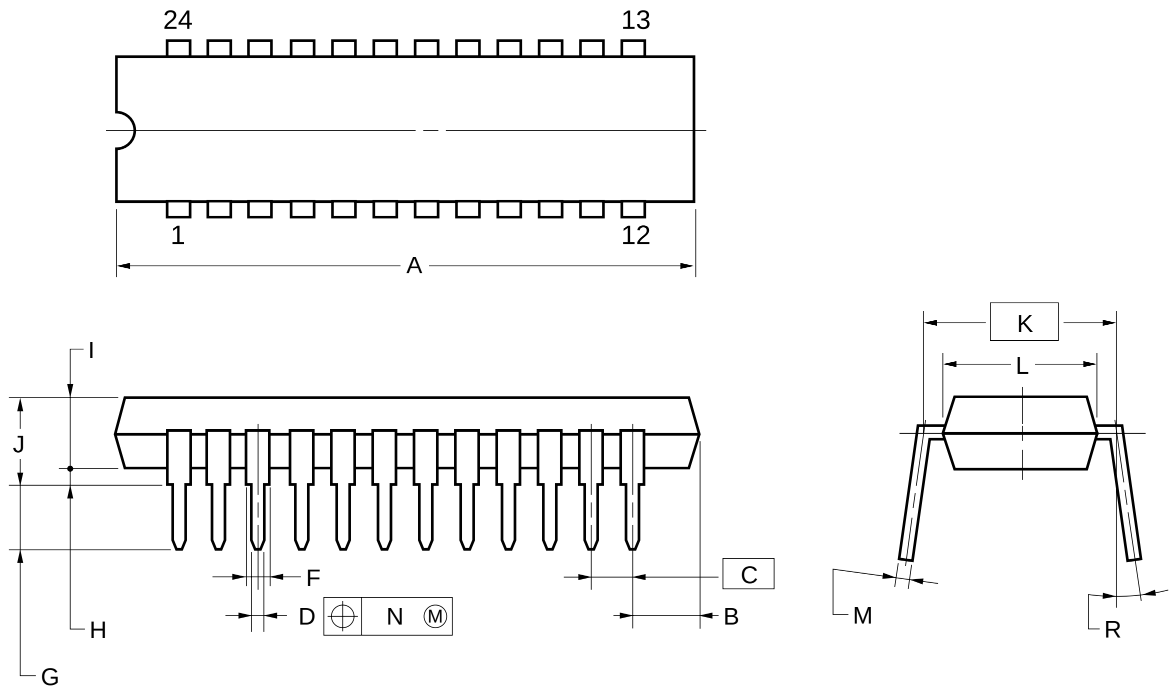
  Therefore, the bypass condenser is connected between these pins and GND pins for keeping the analog accuracy. And it's necessary that the bypass condenser is near IC.

- **HANDLING RELATED TO THE UNUSED PINS**

  The output pins have a possibility of being unused pins.

  If there are unused pins, they must not be connected.

24PIN PLASTIC SHRINK DIP (300 mil)



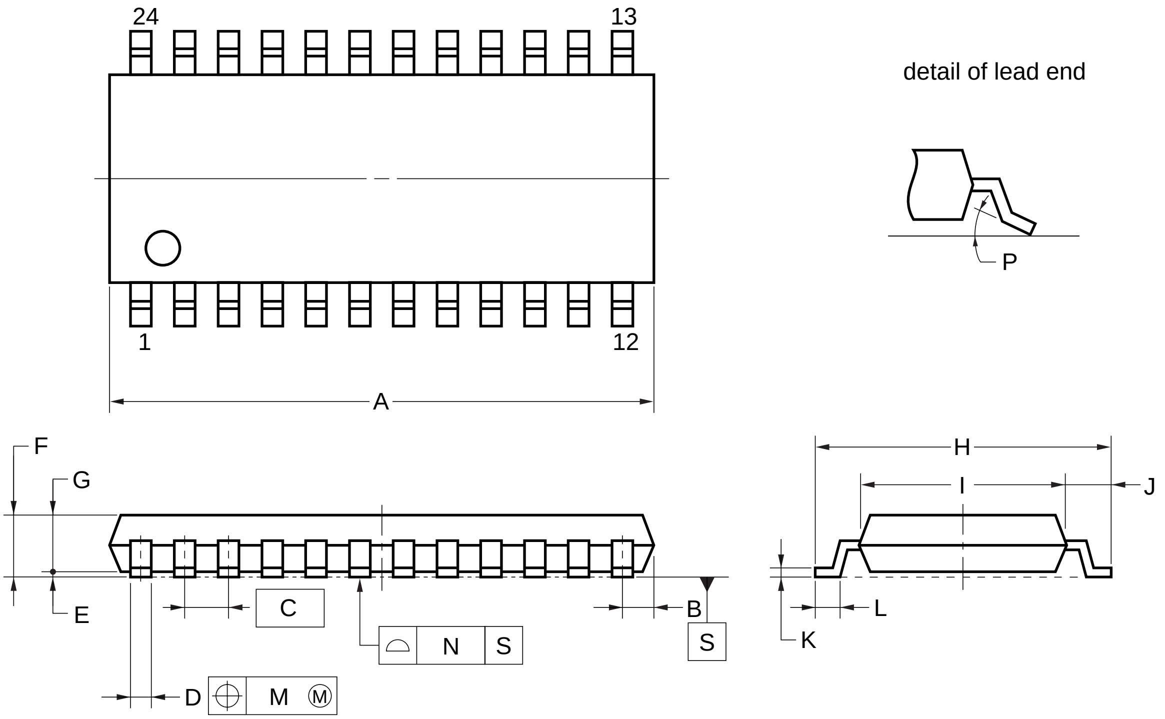
NOTES

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	25.40 MAX.	1.000 MAX.
B	3.0 MAX.	0.119 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50±0.10	$0.020^{+0.004}_{-0.005}$
F	0.85 MIN.	0.033 MIN.
G	3.5±0.3	0.138±0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.4	0.252
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007
R	0~15	0~15

24 PIN PLASTIC SOP (300 mil)



NOTE

1. Controlling dimension —— millimeter.
2. Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	15.3±0.24	0.602±0.010
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.1±0.1	0.004±0.004
F	1.8 MAX.	0.071 MAX.
G	1.55±0.05	0.061±0.002
H	7.7±0.3	0.303±0.012
I	5.6±0.15	$0.220^{+0.007}_{-0.006}$
J	1.05±0.2	$0.041^{+0.009}_{-0.008}$
K	$0.22^{+0.08}_{-0.07}$	$0.009^{+0.003}_{-0.004}$
L	0.6±0.2	$0.024^{+0.008}_{-0.009}$
M	0.12	0.005
N	0.10	0.004
P	$3°^{+7°}_{-3°}$	$3°^{+7°}_{-3°}$

P24GM-50-300B-5

RECOMMENDED SOLDERING CONDITIONS

The following conditions (see tables below) must be met when soldering this product.

Please consult with our sales offices in case other soldering process is used, or in case other soldering is done under different conditions.

TYPES OF SURFACE MOUNT DEVICE

For more details, refer to our document "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

[μPD6222GS]

Soldering method	Soldering conditions	Recommended condition symbol
Infrared ray reflow	Peak package's surface temperature: 235 °C or below, Reflow time: 30 seconds or below (210 °C or higher), Number of reflow process: 3, Exposure limit[Note]: None	IR35-00-3
VPS	Peak package's surface temperature: 215 °C or below, Reflow time: 40 seconds or below (200 °C or higher), Number of reflow process: 2, Exposure limit[Note]: None	VP15-00-2
Wave soldering	Solder temperature: 260 °C or below, Flow time: 10 seconds or below, Number of flow process: 1, Exposure limit[Note]: None	WS60-00-1
Partial heating method	Terminal temperature: 300 °C or below, Flow time: 3 seconds or below, Exposure limit[Note]: None	

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than a single process at once, except for "Partial heating method".

TYPES OF THROUGH HOLE DEVICE

[μPD6222CS]

Soldering method	Soldering conditions	Recommended condition symbol
Wave soldering	Solder temperature: 260 °C or below, Flow time: 10 seconds or below	

REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system	IEI-1212
Quality grade on NEC semiconductor devices	C11531E
Semiconductor device mounting technology manual	C10535E
NEC IC Package Manual (CD-ROM)	C13388E
Guide to quality assurance for semiconductor devices	MEI-1202
Semiconductor selection guide	X10679E

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR MOS DEVICES

Note: No connection for MOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. MOS device behaves differently than Bipolar device. Input levels of MOS device must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

[MEMO]