NEC

MOS INTEGRATED CIRCUIT

μPD6323

LATCH and DRIVER for FIP COMOS LSI

DESCRIPTION

The μPD6323 is a latch and driver CMOS IC for FIP (Fluorescent Indicator Panel). For multiplex wiring, the μPD6323 is supplied with the serial interface circuit, 21 bit shift register, 21 bit data latch and 21 outputs. The serial data transfer from the data source to the μPD6323 is accomplished with 3 signals.

FEATURES

- Direct Connection to Battery enable.
- Wide Supply Voltage V_{DD} = 8.0 to 14 (V)
- Serial Input 21 bit Shift Register Incorporated.
- Data Control by Transmission Clock (External) and Latch.
- Suitable for Static Display by Buffer Register.
- Brightness Control Enable: External Duty Control.
- Output Characteristics V_{out} = 40 V,
  I_{out} = 5.0 mA.
- Serial Interface Format: Compatible with NEC microcomputer.

- Difference of μPD6323C/BC

PARAMETER	SYMBOL	μPD6323C	μPD6323BC
Output Voltage	V_{O0} to V_{O20}	–25 V	–40 V
Low Supply Voltage	$V_{DD\ (L)}$	—	4 V[Note]

Notes 1. Function Operate

ORDERING INFORMATION

PART NUMBER	PACKAGE
μPD6323C	28 pin Plastic DIP (400 mil)
μPD6323BC	28 pin Plastic DIP (400 mil)

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(Previous No. IC-2289)
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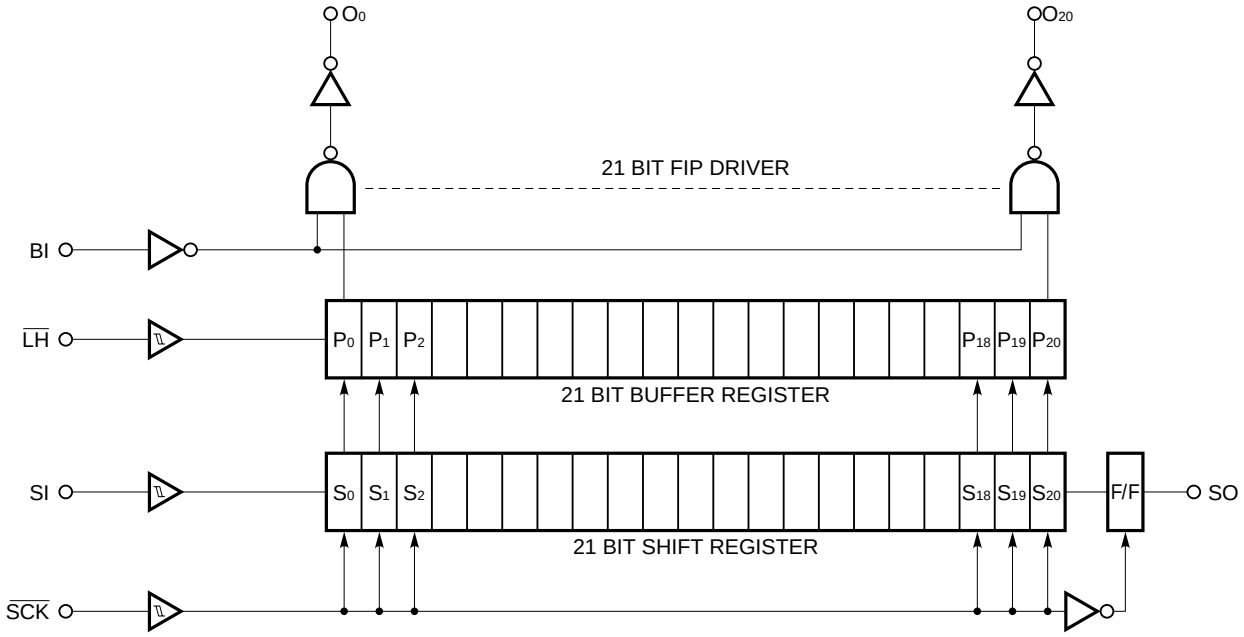
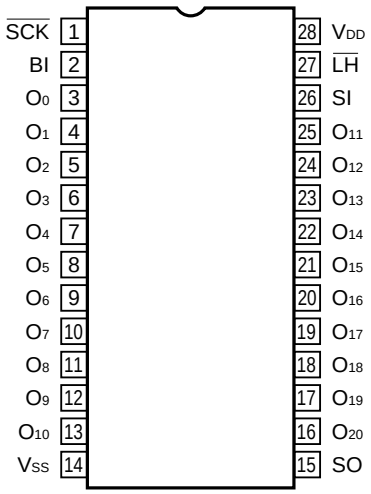
Printed in Japan

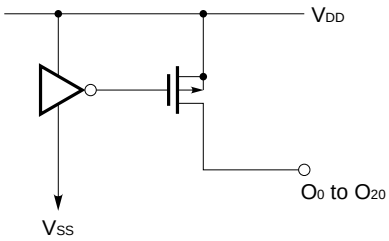
BLOCK DIAGRAM



PIN CONNECTION (Top View)



FUNCTION

PIN No.	SYMBOL	FUNCTION	INPUT/OUTPUT	EXPLANATION
1	$\overline{SCK}$	Serial Clock Input	INPUT	The SI data are read and stored in the 21 bit shift register at the rising edge of $\overline{SCK}$. DATA output from SO at the dropping edge of $\overline{SCK}$.
2	BI	Blanking Input	INPUT	When "L" level signal is supplied to the B1, O0 to O20 are active. "H": O_0 to O_{20} are disabled. Dimmer function is possible by external duty control.
3	O_0	Segment and Driver for FIP (O_0 to O_{10})	OUTPUT	Outputs are, Pch MOS Open Drain. These 11 Outputs are the Outputs of 11 bit output data latch, which can drive FIP directly. 
4	O_1			
5	O_2			
6	O_3			
7	O_4			
8	O_5			
9	O_6			
10	O_7			
11	O_8			
12	O_9			
13	O_{10}			
14	V_{SS}	GND		Connection to GND.
15	SO	Serial Data Output	OUTPUT	Serial data output at the dropping edge of $\overline{SCK}$. In case "n" pieces of μPD6323AC are serial connected, so it is possible to connect one to next SI.
16	O_{20}	Segment and driver for FIP (O_{11} to O_{20})	OUTPUT	Outputs are, Pch MOS Open Drain. These 10 outputs are the Outputs of 10 bit output data latch, which can drive FIP directly.
17	O_{19}			
18	O_{18}			
19	O_{17}			
20	O_{16}			
21	O_{15}			
22	O_{14}			
23	O_{13}			
24	O_{12}			
25	O_{11}			
26	SI	Serial data Input	INPUT	Serial Data Input. The SI data are read and stored in the 21 bit shift register at the rising edge of $\overline{SCK}$.
27	$\overline{LH}$	Latch and Hold Input	INPUT	When "H" level signal is supplied to the $\overline{LH}$, the data of 21 bit shift register are normally transferred to the 21 bit output data latch. At the time of the rising edge of $\overline{LH}$; the data of 21 bit output data latch are held. "L": The data of 21 bit output data latch are protected.
28	V_{DD}	Supply Voltage at V_{DD} terminal		V_{DD} = 8.0 to 14 (V)

***** To prevent latch up breakdown, the power should be turned ON in order V_{DD}, logic input. It should be turned OFF in opposite order. This relationship should be followed during transition period as well.

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage at V_{DD} terminal	V_{DD}	18	V
Input Voltage	V_{IN}	–0.3 to V_{DD}	V
Output Voltage (μPD6323C)	V_{O0} to V_{O20}	–25 Note 1	V
Output Voltage (μPD6323AC/BC)	V_{O0} to V_{O20}	–40 Note 1	V
Output Current	I_{O0} to I_{O20}	–5.0	mA
Operating Temperature	T_A	–40 to +85	°C
Storage Temperature	T_{stg}	–55 to +125	°C

Notes 1. These Voltages are referenced to the V_{DD}.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Operating Temperature	T_A	–40		+85	°C
Operating Supply Voltage	V_{DD}	8.0		14	V
Output Voltage (μPD6323C) Note 2	V_{O0} to V_{O20}		–19	–24	V
Output Voltage (μPD6323AC/BC) Note 2	V_{O0} to V_{O20}		–19	–35	V
Output Current	I_{O0} to I_{O20}		–2.0	–5.0	mA
Input Voltage High	V_{IH}	3.5		V_{DD}	V
Input Voltage Low	V_{IL}	V_{SS}		1.0	V
$\overline{SCK}$ Frequency	f_{SCK}			500	KHz
$\overline{SCK}$ Cycle Time Note 3	t_{KCY}	2.0			μs
$\overline{SCK}$ High Level Pulse Width Note 3	t_{KHW}	0.9			μs
$\overline{SCK}$ Low Level Pulse Width Note 3	t_{KLW}	0.9			μs
SI Setup Time to $\overline{SCK}$ ↑ Note 3	t_{SIK}	0.4			μs
SI Hold Time Note 3	t_{KSI}	0.4			μs
$\overline{SCK}$ → $\overline{LH}$ Valid Time Note 4	t_{CLL}	1.8			μs
$\overline{LH}$ High Level Pulse Width Note 4	t_{LHW}	1.89			μs
BI High Level Pulse Width Note 5	t_{BHW}	0.4			μs

Notes 2. These Voltages are referenced to the V_{DD}.

3. See Fig. 1.

4. See Fig. 2.

5. See Fig. 3.

ELECTRICAL CHARACTERISTICS (Recommended operating conditions)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Input Leakage Current	I_{IL}			±10	μA	$V_{IN} = V_{SS}$ or $V_{IN} = V_{DD}$
SO Output Voltage High	V_{SOH}	$V_{DD} - 1.0$		V_{DD}	V	$I_{SOH} = -1.0$ mA
SO Output Voltage Low	V_{SOL}	V_{SS}		0.5	V	$I_{SOL} = 1.0$ mA
Output Voltage High	V_O	$V_{DD} - 1.5$		V_{DD}	V	$I_O = -5.0$ mA O_0 to O_{20} Output
Output Leakage Current	I_{OLL}			10	μA	V_{DD} to $V_O = 40$ V O_0 to O_{20} Output
Supply Current at V_{DD} Terminal	I_{DD}			2.0	mA	All Input = [High] All Output = Open
Supply Voltage at V_{DD} Terminal to Keep DATA	$V_{DD}(H)$	3.0			V	Drop V_{DD} on latch DATA (MIN.)
Input Capacitance	C_{IN}			15	pF	f = 1.0 MHz
$\overline{SCK} \downarrow \rightarrow$ SO Valid Time[Note 6]	t_{KSO}			0.5	μs	
BI $\rightarrow Q_n$ Valid Time[Note 5]	t_{BKO}			1.8	μs	
Low Supply Voltage (μPD6323BC)	$V_{DD(L)}$	4.0			V	Function Operate

Notes 6. See Fig. 4.

SWITCHING CHARACTERISTICS

Fig. 1

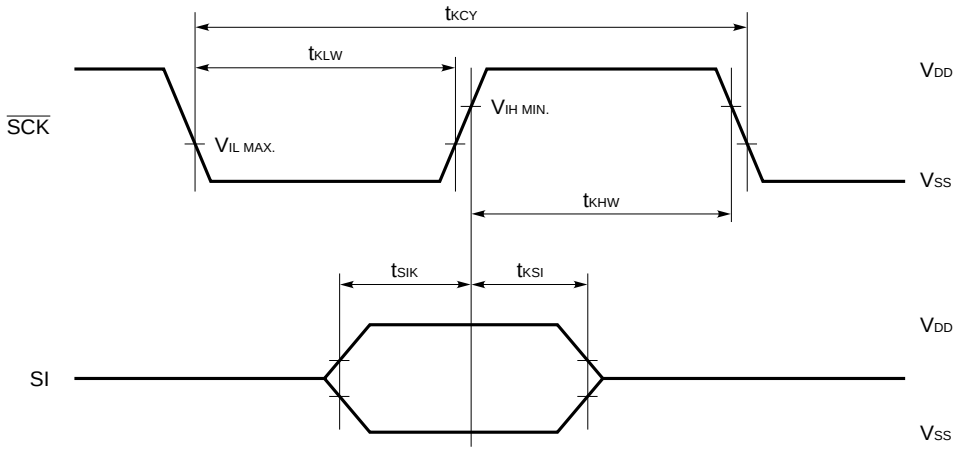


Fig. 2

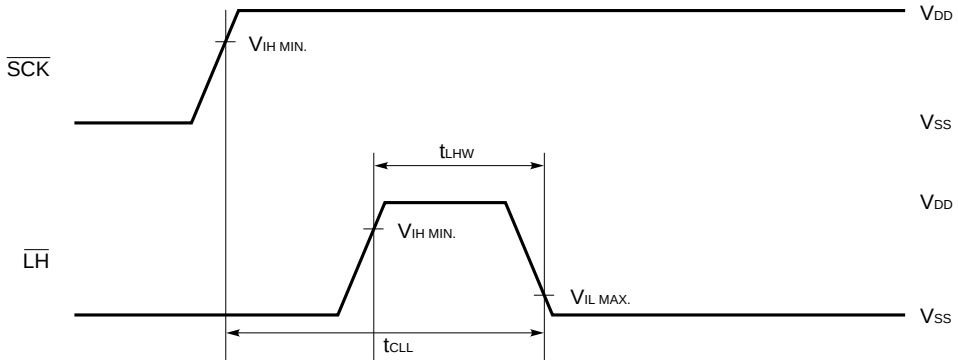


Fig. 3

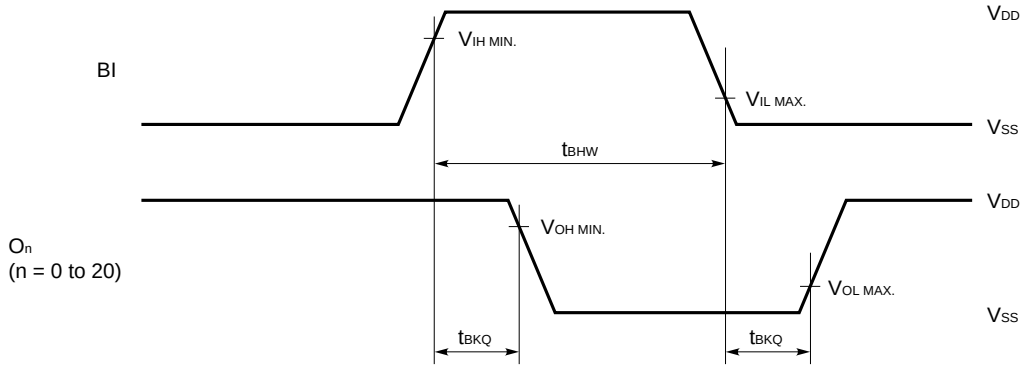
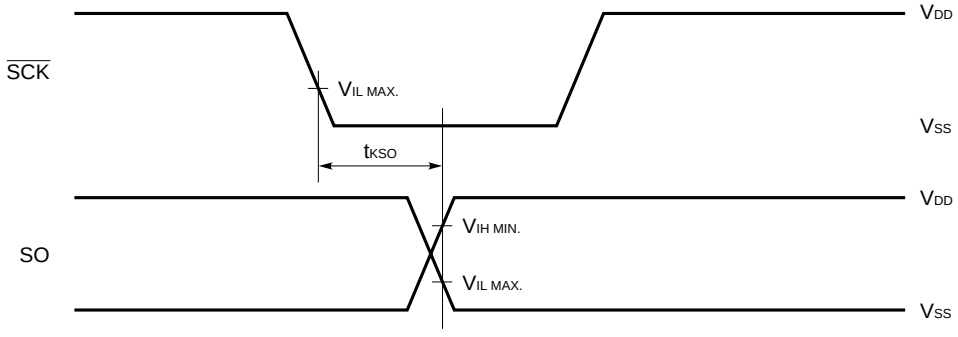
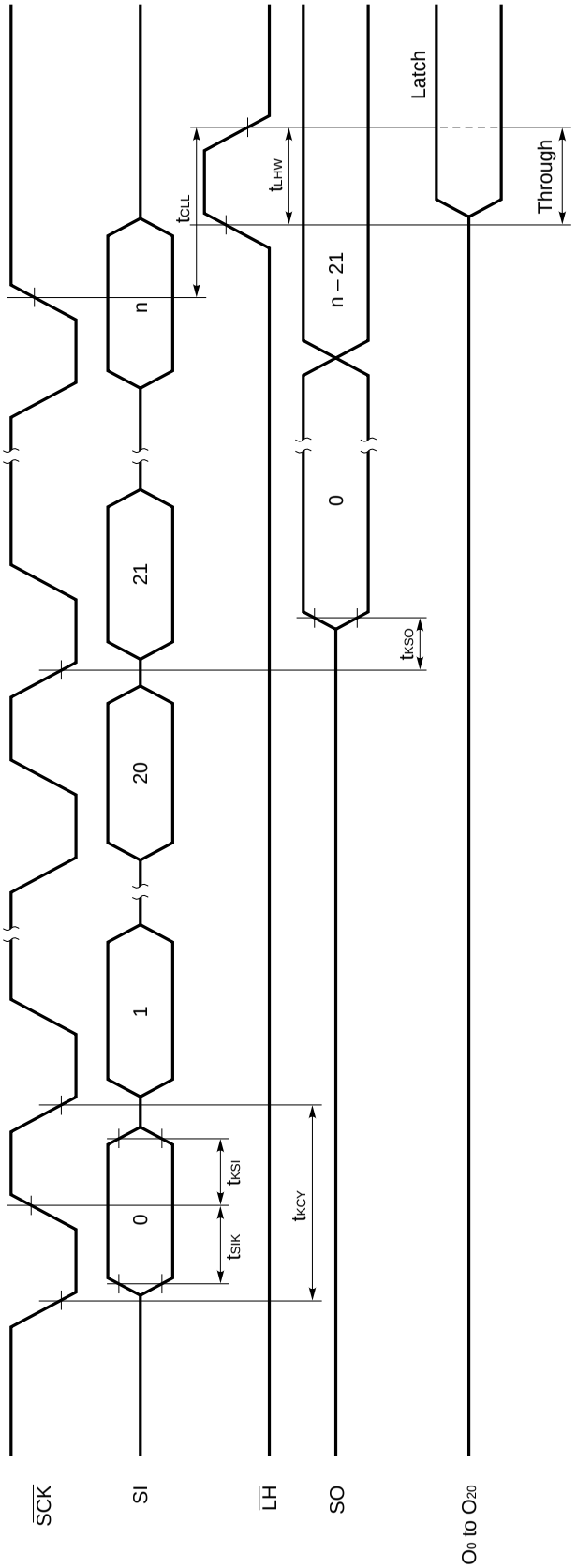


Fig. 4



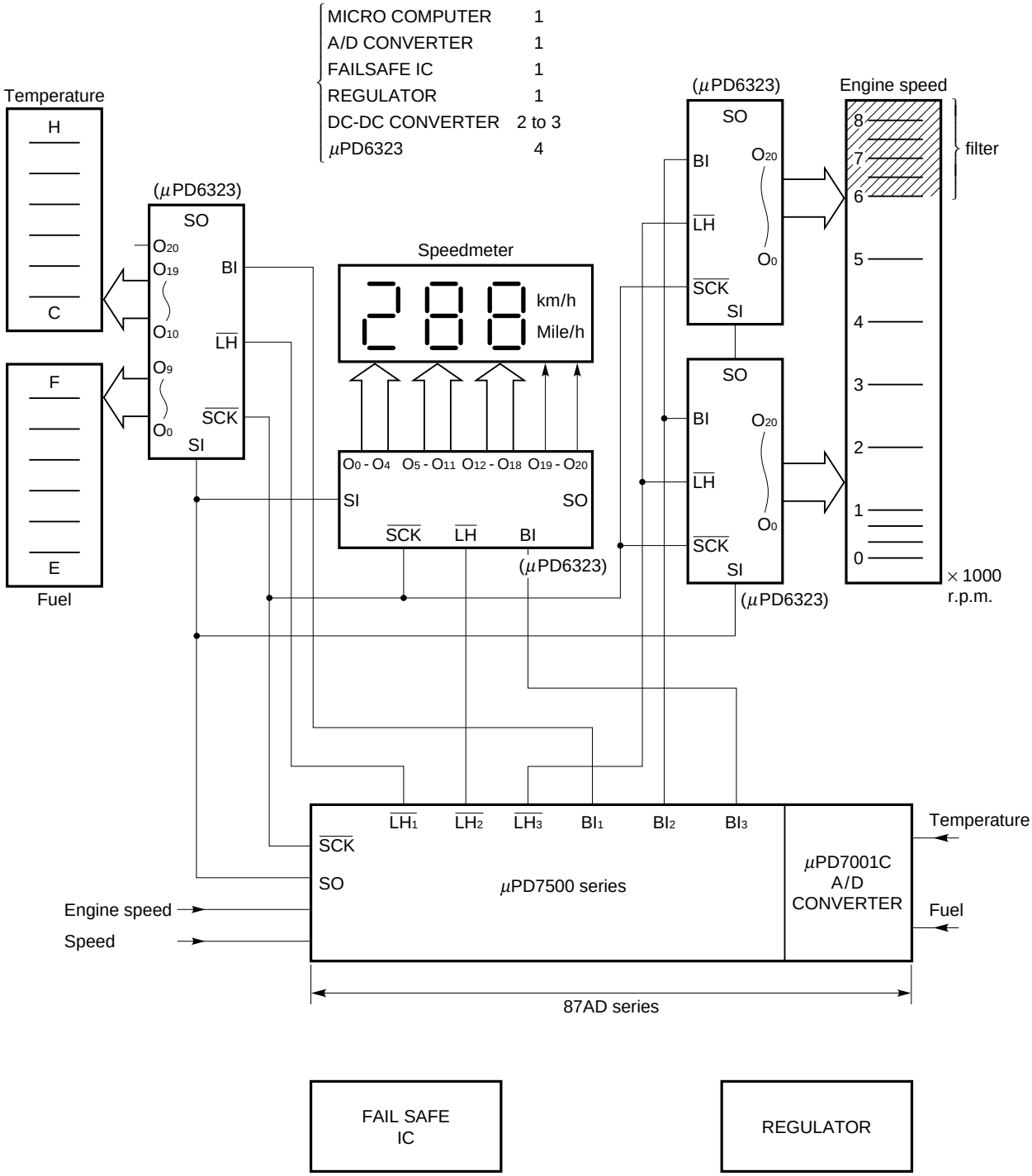
TIMING CHART



APPLICATION CIRCUIT

(1) AUTOMOTIVE DASHBOARD SYSTEM

SYSTEM CONSTRUCTION

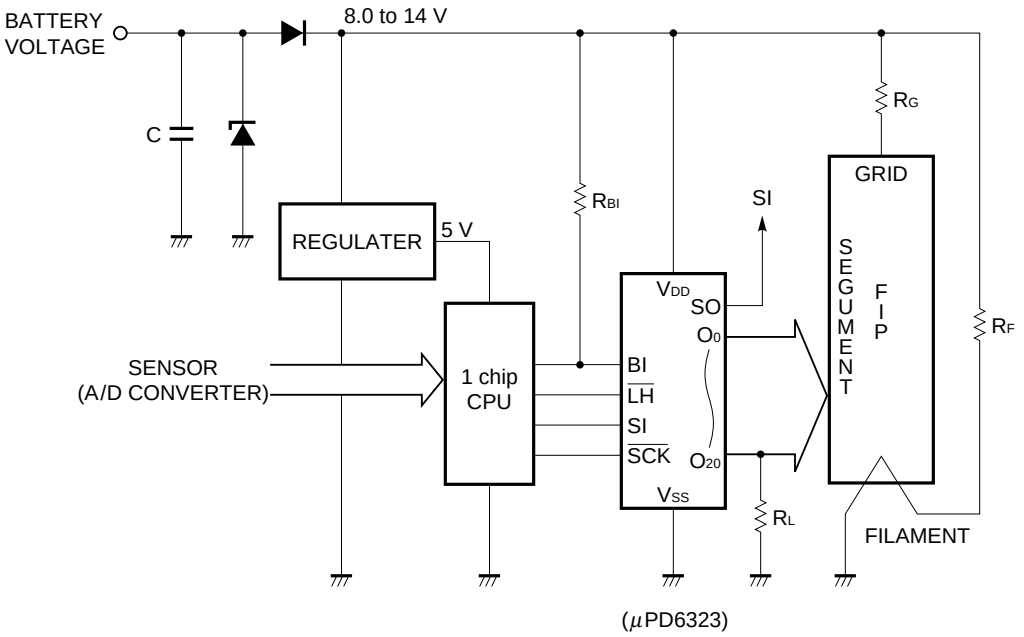


Each data of Engine speed, speed, temperature and fuel is divided to each group by $\overline{LH}$ control.

Each data is transferred by SI and $\overline{SCK}$ control.

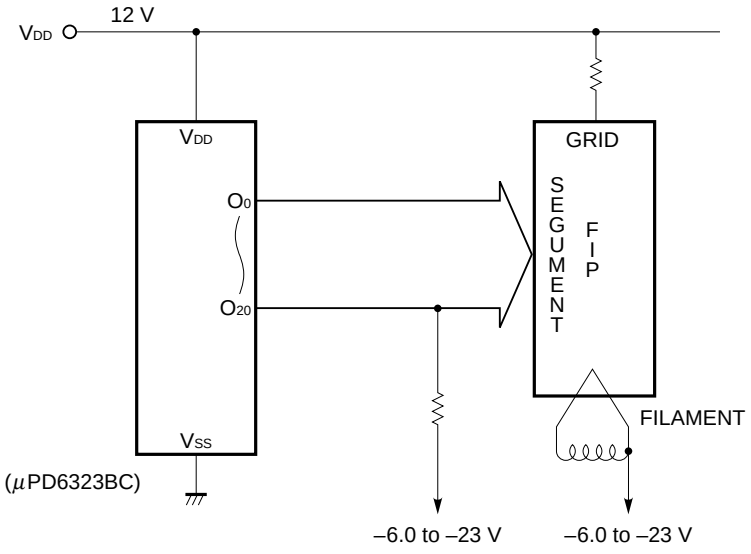
FIP dimmer control is capable by BI's duty control.

(2) 12 V FIP DRIVER CIRCUIT



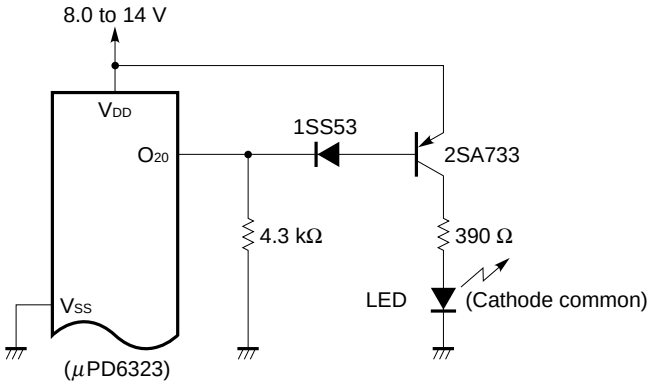
(μPD6323)

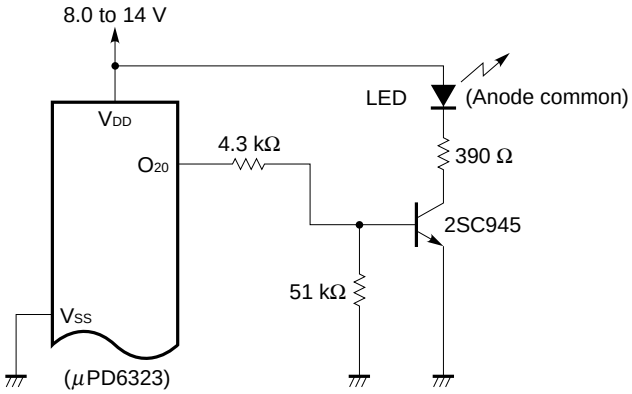
(3) HIGH VOLTAGE (18 to 35 V) FIP DRIVER CIRCUIT



(μPD6323BC)

(4) LED DRIVER CIRCUIT





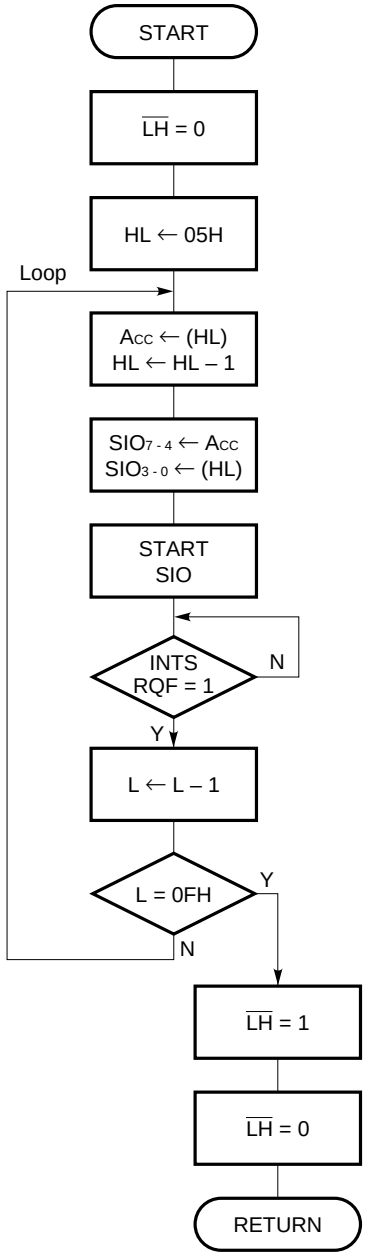
(5) EXAMPLE OF SOFTWARE

Using of serial I/O of μ-COM 75 series
Subroutine of 24 bit data transfer

```
SI OUT :  ANP     6, 7
          LHLI    05H
LOOP   :  LAM     HL–
          TAMSIO
          SIO
          SKI     2
          JCP     $–2
          DLS
          JCP     LOOP
          ORP     6, 8
          ANP     6, 7
          RT
```

RAM (ADD)	TRANSFER BIT			
	3	2	1	0
00H	O_3	O_2	O_1	O_0
01H	O_7	O_6	O_5	O_4
02H	O_{11}	O_{10}	O_9	O_8
03H	O_{15}	O_{14}	O_{13}	O_{12}
04H	O_{19}	O_{18}	O_{17}	O_{16}
05H	O_{23}	O_{22}	O_{21}	O_{20}

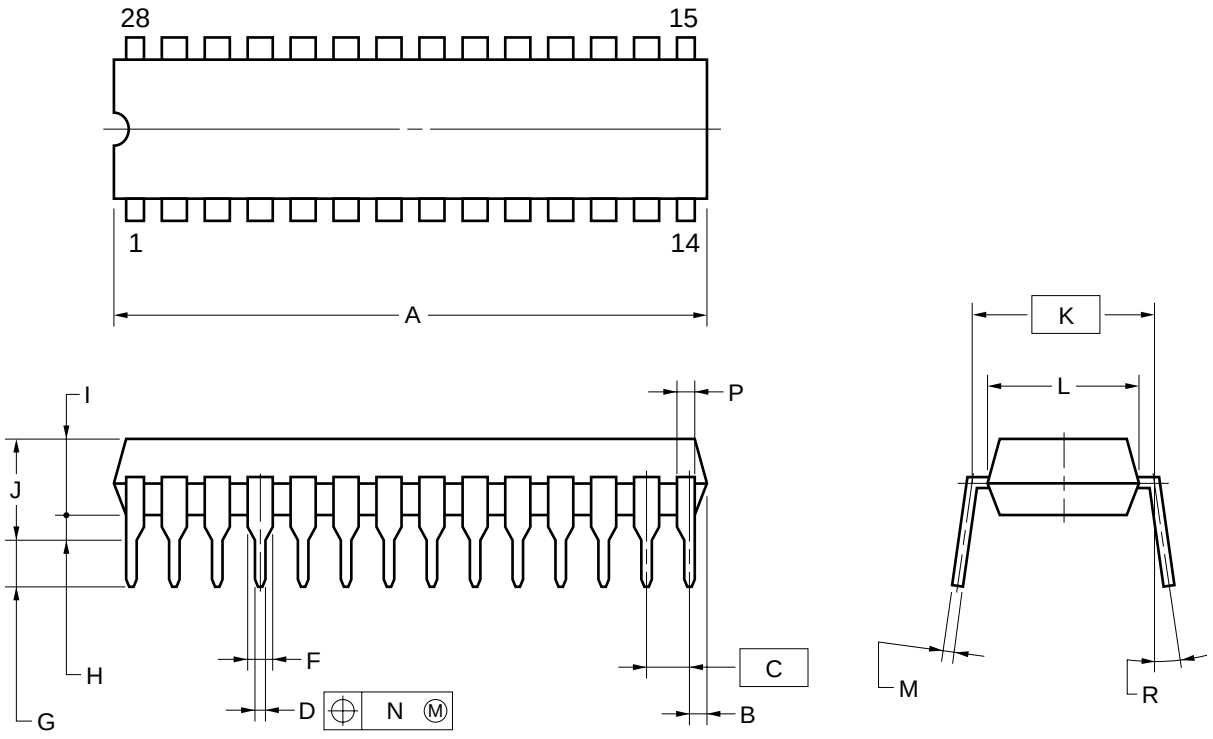
Allot port
P_{63} - $\overline{LH}$



PACKAGE DIMENSION

μPD6323C/BC

28PIN PLASTIC DIP (400 mil)



NOTES

1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	35.56 MAX.	1.400 MAX.
B	1.27 MAX.	0.050 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	0.50 ± 0.10	$0.020^{+0.004}_{-0.005}$
F	1.1 MIN.	0.043 MIN.
G	3.5 ± 0.3	0.138 ± 0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.72 MAX.	0.226 MAX.
K	10.16 (T.P.)	0.400 (T.P.)
L	8.6	0.339
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.25	0.01
P	0.9 MIN.	0.035 MIN.
R	0~15°	0~15°

P28C-100-400-1

RECOMMENDED SOLDERING CONDITIONS

The following conditions (see table below) must be met when soldering this product. Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

TYPES OF THROUGH HOLE MOUNT DEVICE

μPD6323C/BC

Soldering process	Soldering conditions	Symbol
Wave soldering	Solder temperature: 260 °C or below, Flow time: 10 seconds or below	

Reference

"Quality Grades On NEC Semiconductor Devices" (IEI-1209)

"NEC Semiconductor Device Reliability/Quality Controls" (IEI-1206)

"Semiconductor Device Mounting Technology Manual" (IEI-1207)

[MEMO]

The application circuits and their parameters are for references only and are not intended for use in actual design-in's.