

## LATCH and DRIVER for FIP COMOS LSI

## DESCRIPTION

The  $\mu$ PD6323 is a latch and driver CMOS IC for FIP (Fluorescent Indicator Panel). For multiplex wiring, the  $\mu$ PD6323 is supplied with the serial interface circuit, 21 bit shift register, 21 bit data latch and 21 outputs. The serial data transfer from the data source to the  $\mu$ PD6323 is accomplished with 3 signals.

## FEATURES

- Direct Connection to Battery enable.
- Wide Supply Voltage  $V_{DD} = 8.0$  to  $14$  (V)
- Serial Input 21 bit Shift Register Incorporated.
- Data Control by Transmission Clock (External) and Latch.
- Suitable for Static Display by Buffer Register.
- Brightness Control Enable: External Duty Control.
- Output Characteristics  $V_{out} = 40$  V,  
 $I_{out} = 5.0$  mA.
- Serial Interface Format: Compatible with NEC microcomputer.
- Difference of  $\mu$ PD6323C/BC

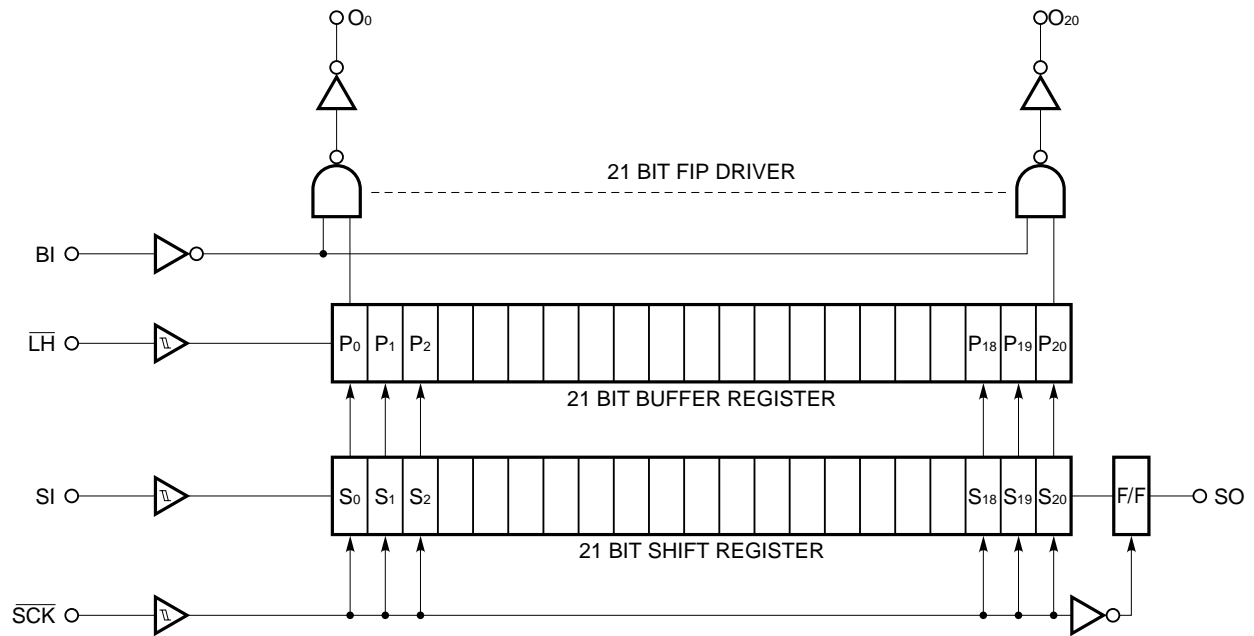
PARAMETER	SYMBOL	$\mu$ PD6323C	$\mu$ PD6323BC
Output Voltage	$V_{O0}$ to $V_{O20}$	-25 V	-40 V
Low Supply Voltage	$V_{DD}$ (L)	—	4 V <sup>Note</sup>

**Notes 1.** Function Operate

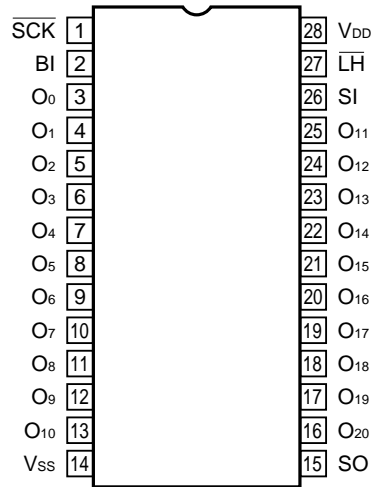
## ORDERING INFORMATION

PART NUMBER	PACKAGE
$\mu$ PD6323C	28 pin Plastic DIP (400 mil)
$\mu$ PD6323BC	28 pin Plastic DIP (400 mil)

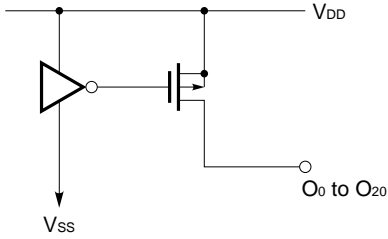
BLOCK DIAGRAM



PIN CONNECTION (Top View)



FUNCTION

PIN No.	SYMBOL	FUNCTION	INPUT/OUTPUT	EXPLANATION
1	$\overline{SCK}$	Serial Clock Input	INPUT	The SI data are read and stored in the 21 bit shift register at the rising edge of $\overline{SCK}$ . DATA output from SO at the dropping edge of $\overline{SCK}$ .
2	BI	Blanking Input	INPUT	When “L” level signal is supplied to the BI, O0 to O20 are active. “H”: O0 to O20 are disabled. Dimmer function is possible by external duty control.
3	O <sub>0</sub>	Segment and Driver for FIP (O <sub>0</sub> to O <sub>10</sub> )	OUTPUT	Outputs are, Pch MOS Open Drain. These 11 Outputs are the Outputs of 11 bit output data latch, which can drive FIP directly. 
4	O <sub>1</sub>			
5	O <sub>2</sub>			
6	O <sub>3</sub>			
7	O <sub>4</sub>			
8	O <sub>5</sub>			
9	O <sub>6</sub>			
10	O <sub>7</sub>			
11	O <sub>8</sub>			
12	O <sub>9</sub>			
13	O <sub>10</sub>			
14	V <sub>SS</sub>	GND		Connection to GND.
15	SO	Serial Data Output	OUTPUT	Serial data output at the dropping edge of $\overline{SCK}$ . In case “n” pieces of μPD6323AC are serial connected, so it is possible to connect one to next SI.
16	O <sub>20</sub>	Segment and driver for FIP (O <sub>11</sub> to O <sub>20</sub> )	OUTPUT	Outputs are, Pch MOS Open Drain. These 10 outputs are the Outputs of 10 bit output data latch, which can drive FIP directly.
17	O <sub>19</sub>			
18	O <sub>18</sub>			
19	O <sub>17</sub>			
20	O <sub>16</sub>			
21	O <sub>15</sub>			
22	O <sub>14</sub>			
23	O <sub>13</sub>			
24	O <sub>12</sub>			
25	O <sub>11</sub>			
26	SI	Serial data Input	INPUT	Serial Data Input. The SI data are read and stored in the 21 bit shift register at the rising edge of $\overline{SCK}$ .
27	$\overline{LH}$	Latch and Hold Input	INPUT	When “H” level signal is supplied to the $\overline{LH}$ , the data of 21 bit shift register are normally transferred to the 21 bit output data latch. At the time of the rising edge of $\overline{LH}$ ; the data of 21 bit output data latch are held. “L”: The data of 21 bit output data latch are protected.
28	V <sub>DD</sub>	Supply Voltage at V <sub>DD</sub> terminal		V <sub>DD</sub> = 8.0 to 14 (V)

\* To prevent latch up breakdown, the power should be turned ON in order V<sub>DD</sub>, logic input. It should be turned OFF in opposite order. This relationship should be followed during transition period as well.

**ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25 °C)**

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage at V <sub>DD</sub> terminal	V <sub>DD</sub>	18	V
Input Voltage	V <sub>IN</sub>	-0.3 to V <sub>DD</sub>	V
Output Voltage ( $\mu$ PD6323C)	V <sub>O0</sub> to V <sub>O20</sub>	-25 <sup>Note 1</sup>	V
Output Voltage ( $\mu$ PD6323AC/BC)	V <sub>O0</sub> to V <sub>O20</sub>	-40 <sup>Note 1</sup>	V
Output Current	I <sub>O0</sub> to I <sub>O20</sub>	-5.0	mA
Operating Temperature	T <sub>A</sub>	-40 to +85	°C
Storage Temperature	T <sub>stg</sub>	-55 to +125	°C

**Notes 1.** These Voltages are referenced to the V<sub>DD</sub>.

**RECOMMENDED OPERATING CONDITIONS**

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Operating Temperature	T <sub>A</sub>	-40		+85	°C
Operating Supply Voltage	V <sub>DD</sub>	8.0		14	V
Output Voltage ( $\mu$ PD6323C) <sup>Note 2</sup>	V <sub>O0</sub> to V <sub>O20</sub>		-19	-24	V
Output Voltage ( $\mu$ PD6323AC/BC) <sup>Note 2</sup>	V <sub>O0</sub> to V <sub>O20</sub>		-19	-35	V
Output Current	I <sub>O0</sub> to I <sub>O20</sub>		-2.0	-5.0	mA
Input Voltage High	V <sub>IH</sub>	3.5		V <sub>DD</sub>	V
Input Voltage Low	V <sub>IL</sub>	V <sub>SS</sub>		1.0	V
$\overline{\text{SCK}}$ Frequency	f <sub>SCK</sub>			500	KHz
$\overline{\text{SCK}}$ Cycle Time <sup>Note 3</sup>	t <sub>KCY</sub>	2.0			$\mu$ s
$\overline{\text{SCK}}$ High Level Pulse Width <sup>Note 3</sup>	t <sub>KHW</sub>	0.9			$\mu$ s
$\overline{\text{SCK}}$ Low Level Pulse Width <sup>Note 3</sup>	t <sub>KLW</sub>	0.9			$\mu$ s
SI Setup Time to $\overline{\text{SCK}}$ $\uparrow$ <sup>Note 3</sup>	t <sub>SIK</sub>	0.4			$\mu$ s
SI Hold Time <sup>Note 3</sup>	t <sub>KSI</sub>	0.4			$\mu$ s
$\overline{\text{SCK}}$ $\rightarrow$ LH Valid Time <sup>Note 4</sup>	t <sub>CLL</sub>	1.8			$\mu$ s
LH High Level Pulse Width <sup>Note 4</sup>	t <sub>LHW</sub>	1.89			$\mu$ s
BI High Level Pulse Width <sup>Note 5</sup>	t <sub>BHW</sub>	0.4			$\mu$ s

**Notes 2.** These Voltages are referenced to the V<sub>DD</sub>.

3. See Fig. 1.
4. See Fig. 2.
5. See Fig. 3.

**ELECTRICAL CHARACTERISTICS (Recommended operating conditions)**

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Input Leakage Current	$I_{IL}$			$\pm 10$	$\mu A$	$V_{IN} = V_{SS}$ or $V_{IN} = V_{DD}$
SO Output Voltage High	$V_{SOH}$	$V_{DD} - 1.0$		$V_{DD}$	V	$I_{SOH} = -1.0$ mA
SO Output Voltage Low	$V_{SOL}$	$V_{SS}$		0.5	V	$I_{SOL} = 1.0$ mA
Output Voltage High	$V_O$	$V_{DD} - 1.5$		$V_{DD}$	V	$I_O = -5.0$ mA $O_0$ to $O_{20}$ Output
Output Leakage Current	$I_{OLL}$			10	$\mu A$	$V_{DD}$ to $V_O = 40$ V $O_0$ to $O_{20}$ Output
Supply Current at $V_{DD}$ Terminal	$I_{DD}$			2.0	mA	All Input = [High] All Output = Open
Supply Voltage at $V_{DD}$ Terminal to Keep DATA	$V_{DD(H)}$	3.0			V	Drop $V_{DD}$ on latch DATA (MIN.)
Input Capacitance	$C_{IN}$			15	pF	$f = 1.0$ MHz
$\overline{SCK} \downarrow \rightarrow$ SO Valid Time <sup>Note 6</sup>	$t_{KSO}$			0.5	$\mu s$	
BI $\rightarrow$ $Q_n$ Valid Time <sup>Note 5</sup>	$t_{BKO}$			1.8	$\mu s$	
Low Supply Voltage ( $\mu$ PD6323BC)	$V_{DD(L)}$	4.0			V	Function Operate

**Notes 6.** See Fig. 4.

SWITCHING CHARACTERISTICS

Fig. 1

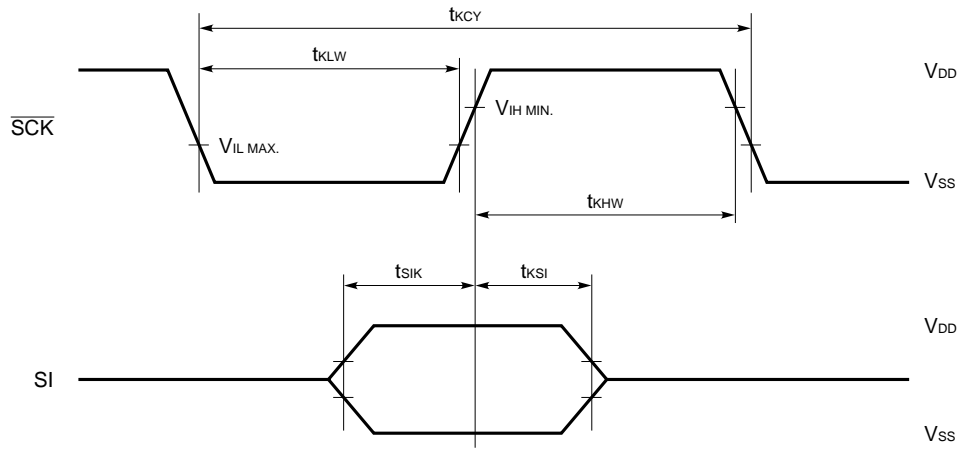


Fig. 2

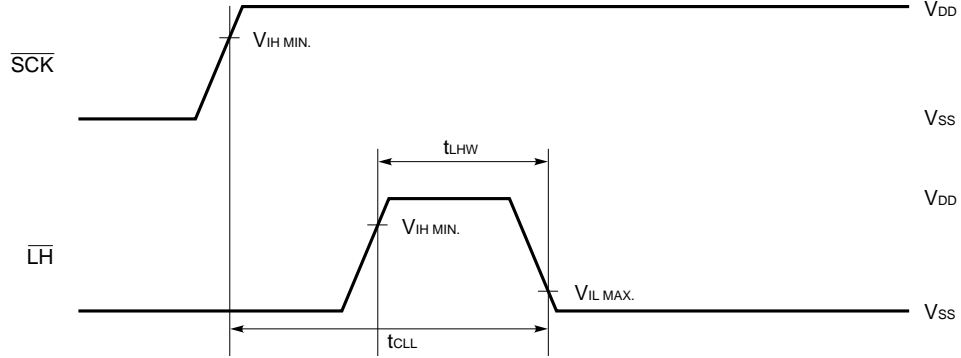


Fig. 3

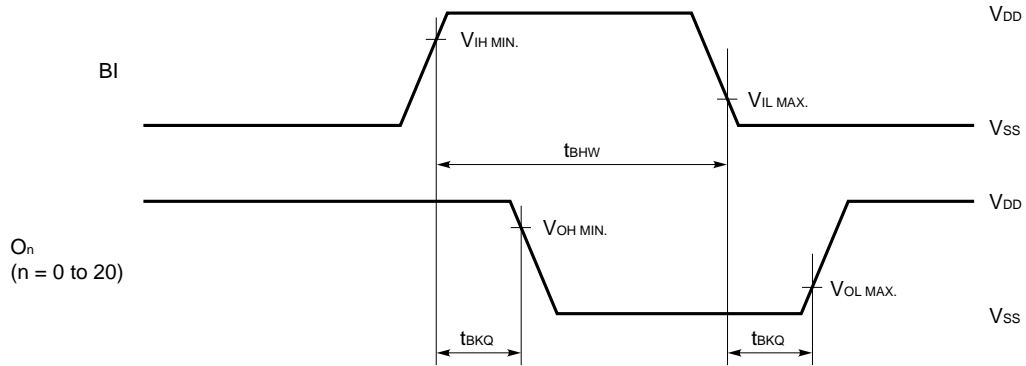
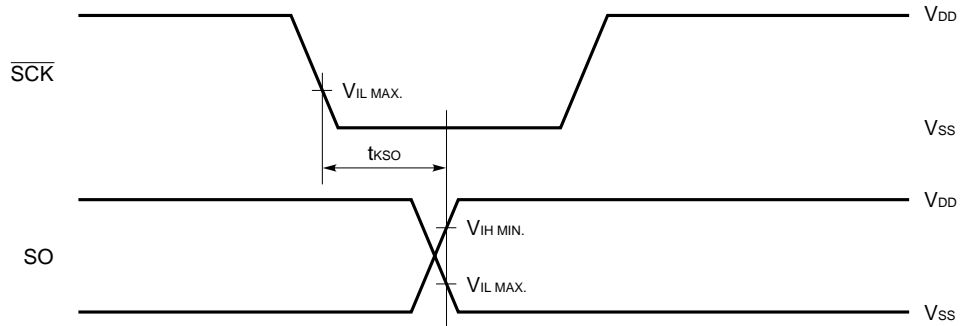
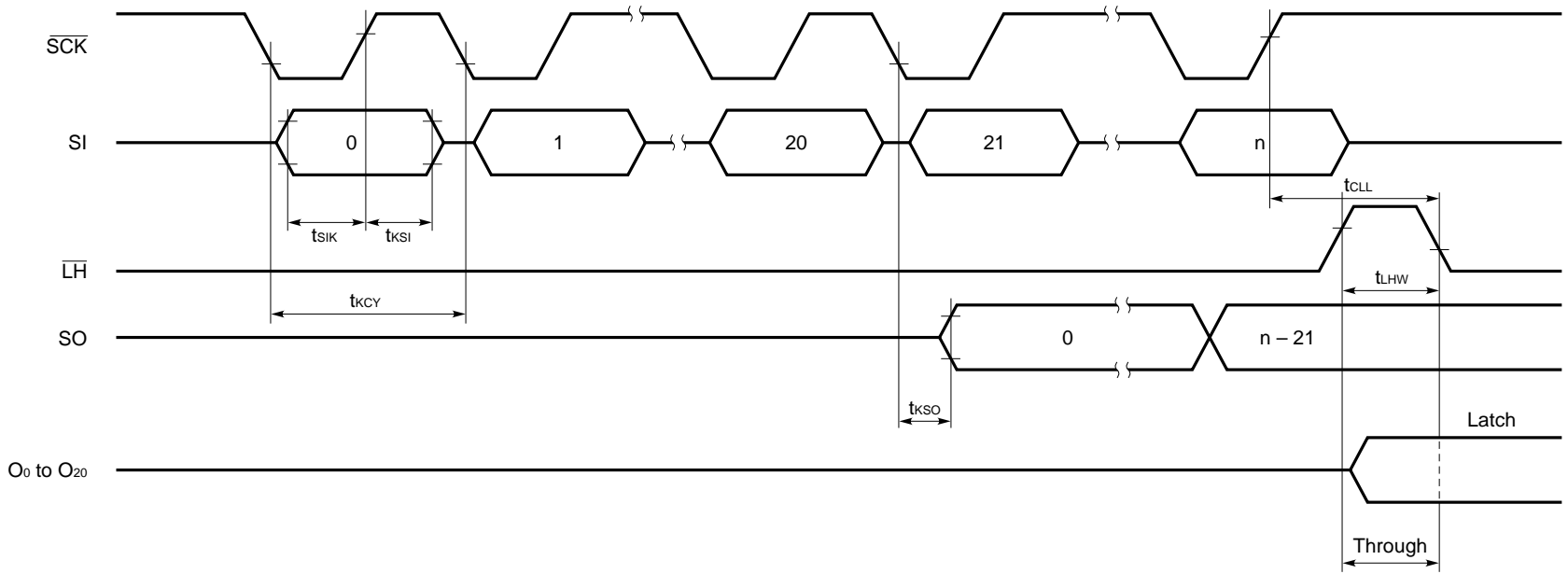


Fig. 4

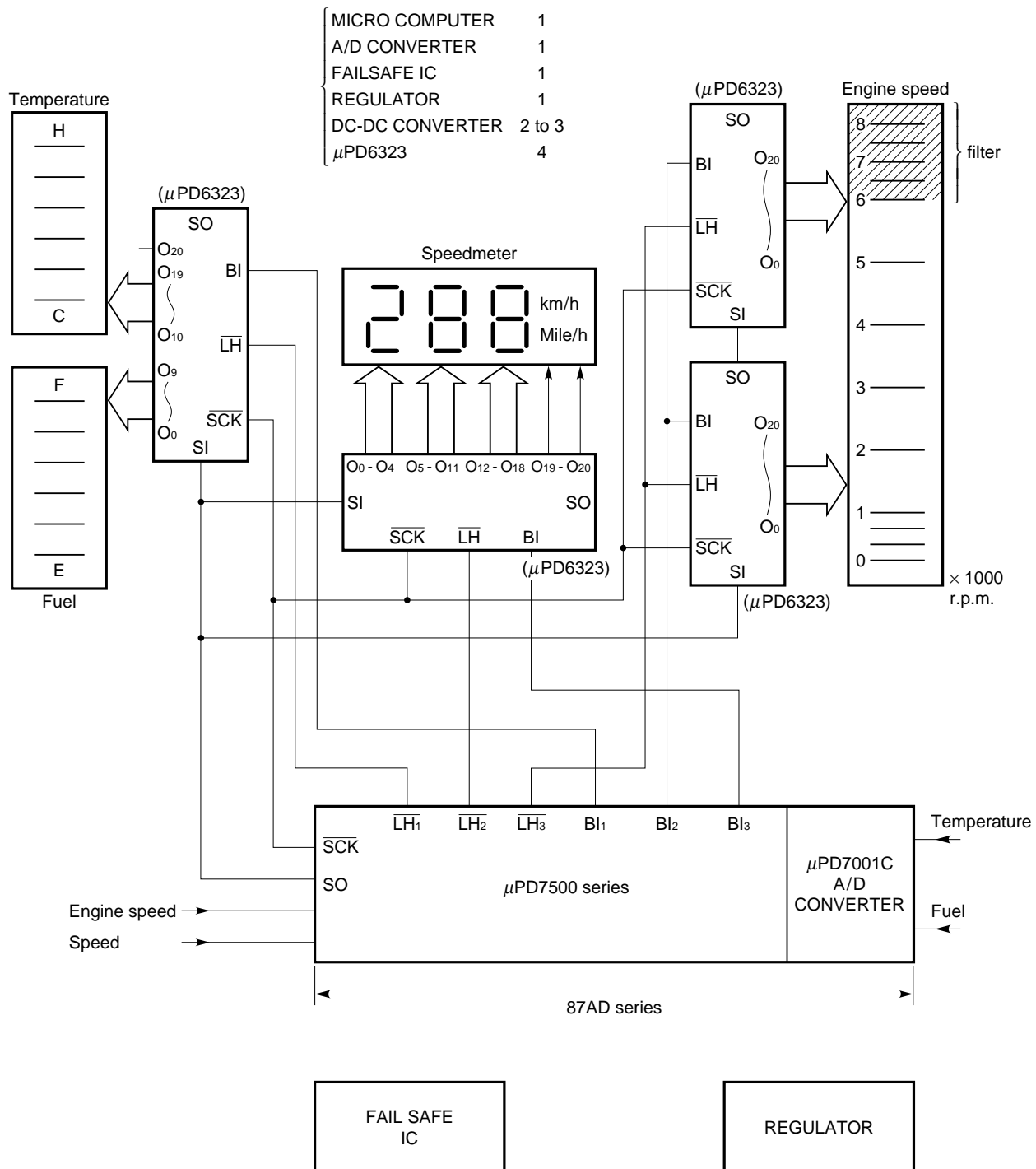


TIMING CHART



APPLICATION CIRCUIT

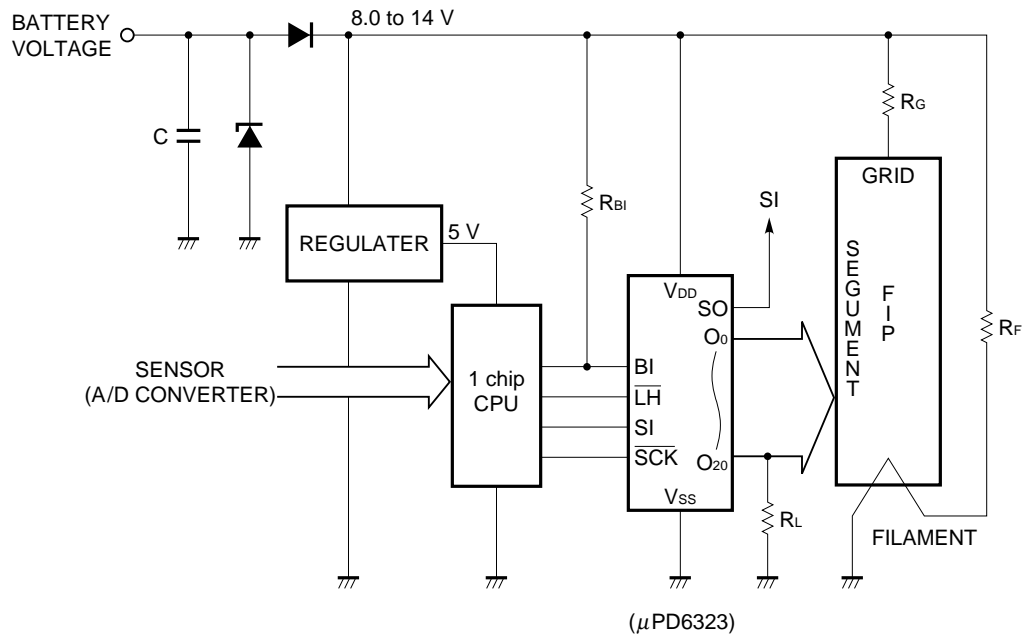
(1) AUTOMOTIVE DASHBOARD SYSTEM  
SYSTEM CONSTRUCTION



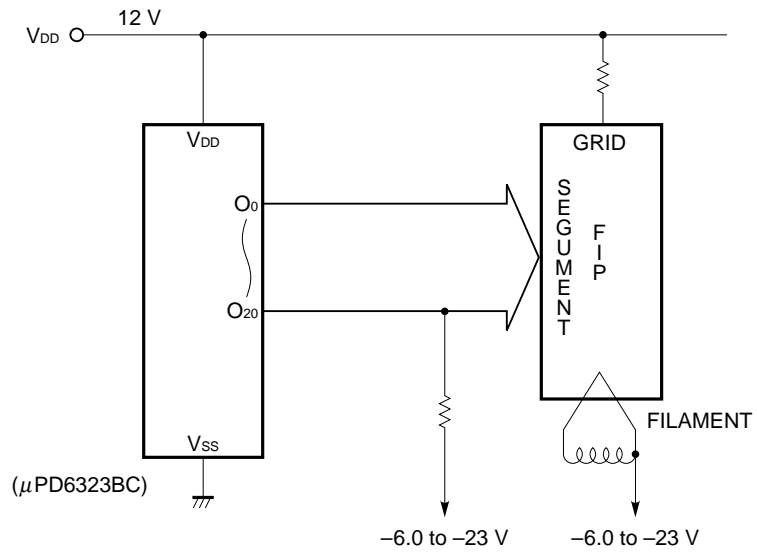
Each data of Engine speed, speed, temperature and fuel is divided to each group by  $\overline{LH}$  control.  
 Each data is transferred by SI and  $\overline{SCK}$  control.  
 FIP dimmer control is capable by BI's duty control.



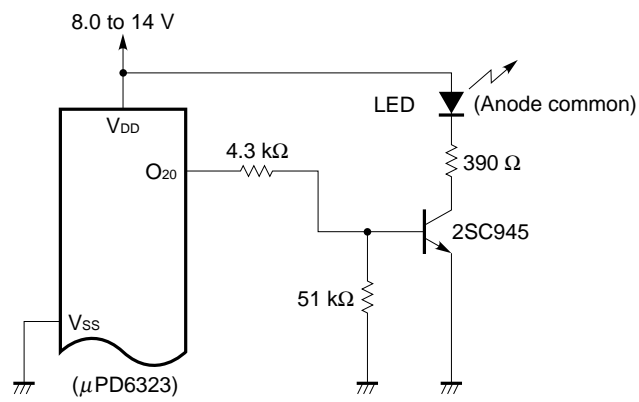
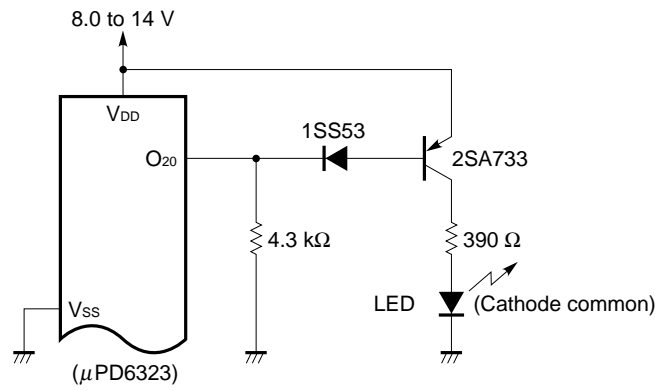
(2) 12 V FIP DRIVER CIRCUIT



(3) HIGH VOLTAGE (18 to 35 V) FIP DRIVER CIRCUIT



(4) LED DRIVER CIRCUIT



(5) EXAMPLE OF SOFTWARE

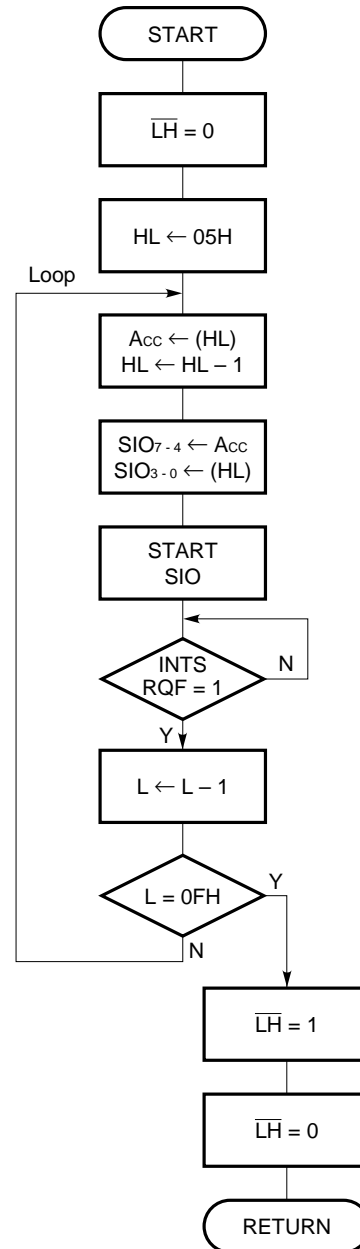
Using of serial I/O of μ-COM 75 series  
Subroutine of 24 bit data transfer

```

SI OUT : ANP    6, 7
        LHLD   05H
LOOP  : LAM    HL-
        TAMSIO
        SIO
        SKI    2
        JCP    $-2
        DLS
        JCP    LOOP
        ORP    6, 8
        ANP    6, 7
        RT
    
```

RAM (ADD)	TRANSFER BIT			
	3	2	1	0
00H	O <sub>3</sub>	O <sub>2</sub>	O <sub>1</sub>	O <sub>0</sub>
01H	O <sub>7</sub>	O <sub>6</sub>	O <sub>5</sub>	O <sub>4</sub>
02H	O <sub>11</sub>	O <sub>10</sub>	O <sub>9</sub>	O <sub>8</sub>
03H	O <sub>15</sub>	O <sub>14</sub>	O <sub>13</sub>	O <sub>12</sub>
04H	O <sub>19</sub>	O <sub>18</sub>	O <sub>17</sub>	O <sub>16</sub>
05H	O <sub>23</sub>	O <sub>22</sub>	O <sub>21</sub>	O <sub>20</sub>

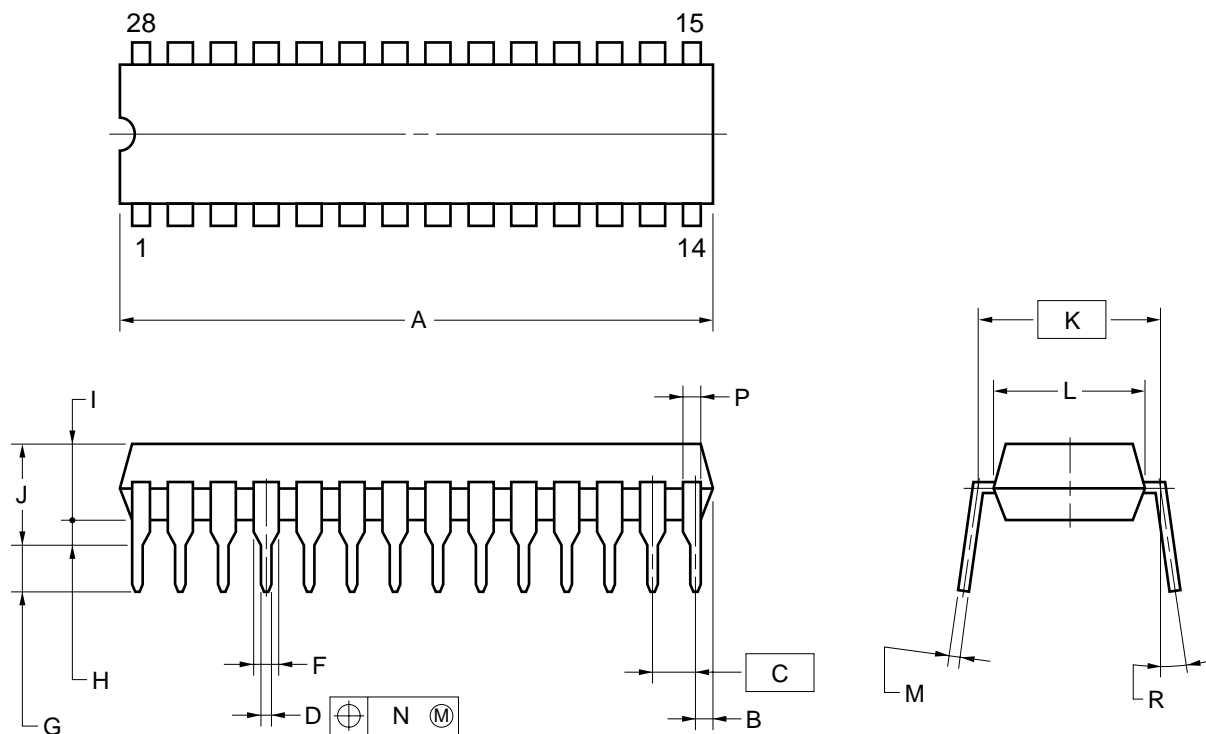
Allot port  
P<sub>63</sub> - LH



PACKAGE DIMENSION

μPD6323C/BC

28PIN PLASTIC DIP (400 mil)



NOTES

- 1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.
- 2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	35.56 MAX.	1.400 MAX.
B	1.27 MAX.	0.050 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	0.50±0.10	0.020 <sup>+0.004</sup> <sub>-0.005</sub>
F	1.1 MIN.	0.043 MIN.
G	3.5±0.3	0.138±0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.72 MAX.	0.226 MAX.
K	10.16 (T.P.)	0.400 (T.P.)
L	8.6	0.339
M	0.25 <sup>+0.10</sup> <sub>-0.05</sub>	0.010 <sup>+0.004</sup> <sub>-0.003</sub>
N	0.25	0.01
P	0.9 MIN.	0.035 MIN.
R	0~15°	0~15°

P28C-100-400-1

**RECOMMENDED SOLDERING CONDITIONS**

The following conditions (see table below) must be met when soldering this product. Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

**TYPES OF THROUGH HOLE MOUNT DEVICE**

μPD6323C/BC

Soldering process	Soldering conditions	Symbol
Wave soldering	Solder temperature: 260 °C or below, Flow time: 10 seconds or below	

**Reference**

- “Quality Grades On NEC Semiconductor Devices” (IEI-1209)
- “NEC Semiconductor Device Reliability/Quality Controls” (IEI-1206)
- “Semiconductor Device Mounting Technology Manual” (IEI-1207)

## [MEMO]

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Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots

Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

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The quality grade of NEC devices in “Standard” unless otherwise specified in NEC's Data Sheets or Data Books. If customers intend to use NEC devices for applications other than those specified for Standard quality grade, they should contact NEC Sales Representative in advance.

Anti-radioactive design is not implemented in this product.