XR-1099

7-Channel Graphic Equalizer Filter with A/D Converter and Improved μP Interface



September 1996-4

FEATURES

- Internal R/C Oscillator
- Provides seven filters in one 16-pin package
- Dual inputs for summing Left and Right Channels
- Provides 30dB of Gain
- Two auxiliary inputs
- Microprocessor Bus Interface
- On Chip A/D Converter

APPLICATIONS

- Graphic Equalizers
- Tape Recorders
- Receivers
- Portable Systems

GENERAL DESCRIPTION

The XR-1099 is a 7-point switched capacitor filter dedicated for use in audio applications. The 7 filters are spaced 1 1/2 octaves apart starting at 63Hz. The two filter inputs allow the left and right channels to be summed. This reduces the display space and prevents redundant audio information from being displayed. The 7 filter outputs, along with the peak value of all filters each go into a peak hold circuit with a slow decay time constant

(330ms). The eight filter outputs and 2 auxiliary inputs are multiplexed into an A/D converter which produces the digital output that is used by the system microprocessor.

The XR-1099 is fabricated in a low noise 2 micron double poly-silicon CMOS process and comes in a 16-pin plastic package. The device may be operated off of either $\pm 5 \text{V}$ or $\pm 6 \text{V}$ supplies. The chip oscillator operates at 400kHz and requires only an external resistor and capacitor.

ORDERING INFORMATION

Part No.	Package	Operating Temperature Range	
XR-1099CP	16 Lead 300 Mil PDIP	-30°C to 75°C	





BLOCK DIAGRAM

AUX1 AUX1-AUX2 🕽 AUX2 63Hz Peak Hold 63Hz Bandpass Filter Oscillator Clock-U Generator 160Hz Bandpass Filter Peak Hold 160Hz CLKR CLKC 400Hz Peak Hold Bandpass Filter 400Hz Test V_{REF} L 1kHz Peak Hold Bandpass Filter Ε 1kHz Mixer A/D х 3 Pole SC Converter Anti-Aliasing 2.5kHz Filter Ε Peak Hold Bandpass Filter 2.5kHz 2 Pole Continuous Time Anti-Aliasing Filter 6.3kHz Peak Hold Bandpass Filter 6.3kHz 2 Pole Continuous Time Anti-Aliasing Filter 16kHz Bandpass Filter Peak Hold 16kHz L_{IN} Peak Hold PEAK Shift Register → EOC + Digital Control DATAIN DATAOUT

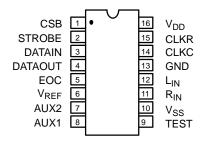
Figure 1. 7-Band Graphic Equalizer Display Filter with A/D Converter and Improved Microprocessor Interface

CS

STROBE



PIN CONFIGURATION



16 Lead PDIP (0.300")

PIN DESCRIPTION

Pin#	Symbol	Description
1	CSB	Chip Select Pin
2	STROBE	Clock Pin to Shift In/Out Data Through the Serial Port
3	DATAIN	Serial Port for Digital Signals from Microprocessor
4	DATAOUT	Serial Port for Digital Signals to Microprocessor
5	EOC	(A/D) End of Conversion Pin
6	VREF	A/D Converter Reference Voltage Input
7	AUX2	Auxiliary Input 2
8	AUX1	Auxiliary Input 1
9	TEST	For Testing Purposes Only; Not Designed to Drive Any Load
10	V _{SS}	Negative Supply Voltage
11	R _{IN}	Right Channel Input
12	L _{IN}	Left Channel Input
13	GND	Ground
14	CLKC	Clock Capacitor from this Pin to GND (Cnom = 1nF)
15	CLKR	Clock Resistor from this Pin to CLKC (Rnom = 14.6 k Ω)
16	V_{DD}	Positive Supply Voltage



ELECTRICAL CHARACTERISTICS:

Test Conditions: V_{DD} = +5V, V_{SS} = -5V, V_{REF} = 2.55 V, T_A = 25°C

Symbol	Parameter	Min.	Тур.	Max.	Units	Conditions
General Characteristics						
V_{DD}	Positive Supply Voltage	4.75		6	V	
V _{SS}	Negative Supply Voltage	-6		-4.75	V	
I _{DD5}	Supply Current		8	15	mA	
Digital Pins						
V_{IL}	Input Voltage Low			0.5	V	
V _{IH}	Input Voltage High	4.5			V	
V_{OL}	Output Voltage Low			0.5	V	
V _{OH}	Output Voltage High	4.5			V	
Analog And D	Digital Inputs					
ΙΙ _L	Input Leakage Current	-2.0		+2.0	μΑ	
Oscillator Cha	aracteristics					
TCLKRP	Clock Frequency	380	400	420	kHz	R =1.46 kΩ, C = 1nF
A/D Characte	ristics				•	
	Accuracy			8	bit	
	Error			±1	LSB	
V_{REF}	Reference Voltage		2.5		V	
TCONV	Conversion Time	400		440	μS	
Filter Charact	eristics	•	•	•	•	•
FOS	Filter Offset	0		+200	mV	mV
FG63	Filter Gain 63Hz	1.08	1.28	1.52	V	INPUT=40mVpk
		28.5	30.0	31.5	dB	f _{IN} =63Hz
		2.15	2.55	2.55	V	INPUT=80mVpk
FG160	Filter Gain 160Hz	1.08	1.28	1.52	V	INPUT=40mVpk
		28.5	30.0	31.5	dB	f _{IN} =160Hz
		2.15	2.55	2.55	V	INPUT=80mVpk
FG400	Filter Gain 400Hz	1.08	1.28	1.52	V	INPUT=40mVpk
		28.5	30.0	31.5	dB	f _{IN} =400Hz
		2.15	2.55	2.55	V	INPUT=80mVpk
FG1K	Filter Gain 1kHz	1.08	1.28	1.52	V	INPUT=40mVpk
		28.5	30.0	31.5	dB	f _{IN} =1kHz
		2.15	2.55	2.55	V	INPUT=80mVpk
FG2.5K	Filter Gain 2.5kHz	1.08	1.28	1.52	V	INPUT=40mVpk
		28.5	30.0	31.5	dB	f _{IN} =2.5kHz
		2.15	2.55	2.55	V	INPUT=80mVpk



ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Symbol	Parameter	Min.	Тур.	Max.	Units	Conditions		
Filter Charac	Filter Characteristics							
FG6.3K	Filter Gain 6.3kHz	1.08	1.28	1.52	V	INPUT=40mVpk		
		28.5	30.0	31.5	dB	f _{IN} =6.3kHz		
		2.15	2.55	2.55	V	INPUT=80mVpk		
FG16K	Filter Gain 16kHz	1.08	1.28	1.52	V	INPUT=40mVpk		
		28.5	30.0	31.5	dB	f _{IN} =16kHz		
		2.15	2.55	2.55	V	INPUT=80mVpk		
GPK	Peak Gain	1.08	1.28	1.52	V	INPUT=40mVpk		
		28.5	30.0	31.5	dB	f _{IN} =1kHz		
		2.15	2.55	2.55	V	INPUT=80mVpk		

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage ± 7V Storage Temperature -60°C to +150°C

SYSTEM DESCRIPTION

The XR-1099 generates its clocks with an internal oscillator and does not require an external clock source. This allows the designer to place the XR-1099 in any application where an active filter design is in place. The XR-1099 provides bandpass filters with center frequencies at 63Hz, 160Hz, 400Hz, 1kHz, 2.5kHz, 6.3kHz, and 16kHz. These frequencies are standards in the consumer audio industry. The peak detector outputs

referenced to 0V are multiplexed into an A/D converter. The digital interface allows the system microprocessor to control the multiplexer and the A/D externally. All digital outputs swing from GND to V_{DD} .

The XR-1099 contains a continuous time anti-aliasing filter with a corner frequency of 80kHz. This prevents most signals from affecting the performance of the filters.





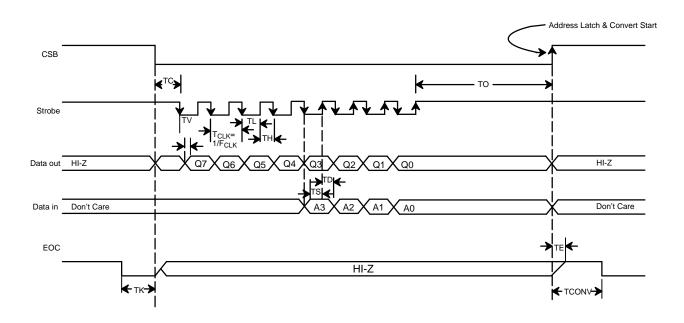


Figure 2. Microprocessor Interface Timing Diagram

Symbol	Parameter	Min.	Max.	Units
FCLK	STROBE Frequency ¹		2.5	MHz
TH	STROBE High Pulse Width	160		ns
TL	STROBE Low Pulse Width	160		ns
TS	DATA Set-Up Time	100		ns
TD	DATA Hold Time	100		ns
TO	STROBE to CSB	160		ns
TE	EOC Delay Time ²	100		ns
TCONV	A/D Conversion Time ³	400	440	μs
TK	EOC to CSB	100		ns
TC	CSB to STROBE	150		ns
TV	STROBE to Q7-Q0	150		ns

¹ TCLK = 400ns. minimum.

² After TE, EOC becomes a logical high. ³ After TCONV, EOC goes low, signaling the end of conversion.



A3	A2	A 1	A0	Selection
0	0	0	0	63Hz
0	0	0	1	160Hz
0	0	1	0	400Hz
0	0	1	1	1kHz
0	1	0	0	2.5kHz
0	1	0	1	6.3kHz
0	1	1	0	16kHz
0	1	1	1	PEAK
1	0	0	0	AUX1
1	0	0	1	AUX2
1	0	1	0	NONE
1	0	1	1	NONE
1	1	0	0	NONE
1	1	0	1	NONE
1	1	1	0	NONE
1	1	1	1	NONE

Table 1. Multiplexer Selection

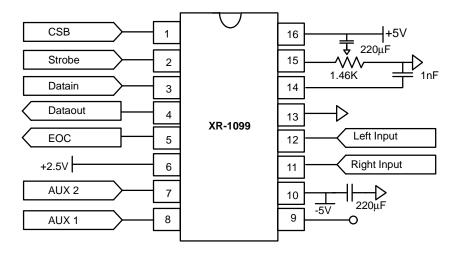
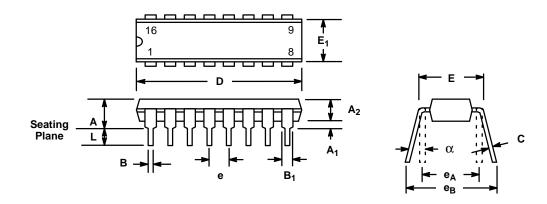


Figure 3. Typical Application Schematic



16 LEAD PLASTIC DUAL-IN-LINE (300 MIL PDIP)

Rev. 1.00



	INC	HES	MILLI	METERS	
SYMBOL	MIN	MAX	MIN	MAX	
А	0.145	0.210	3.68	5.33	
A ₁	0.015	0.070	0.38	1.78	
A ₂	0.115	0.195	2.92	4.95	
В	0.014	0.024	0.36	0.56	
B ₁	0.030	0.070	0.76	1.78	
С	0.008	0.014	0.20	0.38	
D	0.745	0.840	18.92	21.34	
E	0.300	0.325	7.62	8.26	
E ₁	0.240	0.280	6.10	7.11	
е	0.1	00 BSC	2.5	54 BSC	
e _A	0.3	0.300 BSC 7		7.62 BSC	
e _B	0.310	0.430	7.87	10.92	
L	0.115	0.160	2.92	4.06	
α	0°	15°	0°	15°	

Note: The control dimension is the inch column















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