

LM4040, LM4041

Precision Micro-Power Shunt Voltage References

Description

LM4040 and LM4041 are precision two-terminal shunt mode voltage references offered in factory programmed reverse breakdown voltages of 1.225 V, 2.500 V, 3.000 V, 3.300 V, 4.096 V, and 5.000 V.

ON Semiconductor's Charge Programmable floating gate technology ensures precise voltage settings offering five grades of initial accuracy; from 0.1% to 2%.

LM4040 and LM4041 operate over a shunt current range of 60 μ A to 15 mA with low dynamic impedance, and 100 ppm/ $^{\circ}$ C temperature coefficient ensuring stable reverse breakdown voltage accuracy over a wide range of operating conditions.

These shunt regulators do not require an external stabilizing capacitor but are stable with any capacitive load (up to 1 μ F).

Offered in space saving SOT-23 and SC-70 packages LM4040 and LM4041 are specified for operation over the full industrial temperature range of -40° C to $+85^{\circ}$ C.

Features

- Reverse Breakdown Voltages:
 - ◆ 1.225 V
 - ◆ 2.500 V
 - ◆ 3.000 V
 - ◆ 3.300 V
 - ◆ 4.096 V
 - ◆ 5.000 V
- Accuracy Grades:
 - ◆ A: $\pm 0.1\%$
 - ◆ B: $\pm 0.2\%$
 - ◆ C: $\pm 0.5\%$
 - ◆ D: $\pm 1.0\%$
 - ◆ E: $\pm 2.0\%$
- Operating Current: 60 μ A to 15 mA
- Low Output Noise: 35 μ V (10 Hz to 10 KHz)
- Small Package Size: SOT-23, SC-70
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Mobile Handheld Devices
- Industrial Process Control
- Instrumentation
- Laptop and Desktop PCs
- Automotive
- Energy Management



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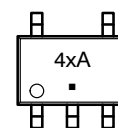
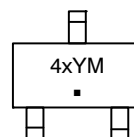


SOT-23 3 Lead
TB SUFFIX
CASE 527AG



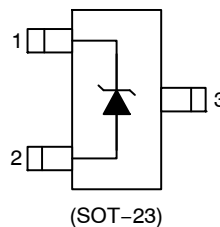
SC-70 5 Lead
SD SUFFIX
CASE 419AC

MARKING DIAGRAMS

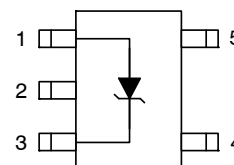


- 4x = Specific Device Code
(4L = LM4040, 4M = LM4041)
- A = Assembly Location Code
- Y = Production Year
- M = Production Month
- = Pb-Free Package

PIN CONNECTIONS



(SOT-23)



(SC-70)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 13 of this data sheet.

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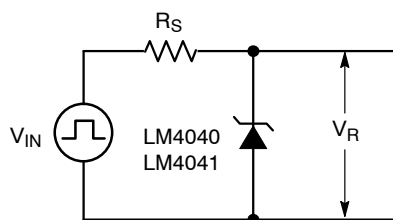


Figure 1. Test Circuit

Table 1. PIN DESCRIPTIONS

Pin		Name	Function
SOT-23	SC-70		
1	3	V+	Positive voltage
2	1	V-	Negative voltage
3	2	NC	This pin must be left floating or connected to V-.
	4	NIC	No Internal Connection. A voltage or signal applied to this pin will have no effect.
	5	NIC	

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Unit
Reverse Current	20	mA
Forward Current	10	mA
Junction Temperature	150	°C
Power Dissipation	SOT-23-3	300
Power Dissipation	SC-70-5	240
		mW

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 3. RECOMMENDED OPERATING CONDITIONS

Parameter	Rating	Unit
I _{REVERSE}	0.06 – 15	mA
Ambient Temperature Range	-40 to +85	°C

Table 4. ESD SUSCEPTABILITY

Symbol	Parameter	Min	Units
ESD	Human Body Model	2000	V
	Machine Model	200	V

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Table 5. DC ELECTRICAL CHARACTERISTICS

($I_R = 100 \mu\text{A}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise noted. Typical values are at $T_A = +25^\circ\text{C}$.)

Symbol	Parameter	Test Conditions	Limits			Units	
			Min	Typ	Max		
1.225 V							
V_R	Reverse Breakdown Voltage	$T_A = +25^\circ\text{C}$	LM4041A (0.1%)	1.2238	1.225	1.2262	V
			LM4041B (0.2%)	1.2226	1.225	1.2274	
			LM4041C (0.5%)	1.219	1.225	1.231	
			LM4041D (1.0%)	1.213	1.225	1.237	
			LM4041E (2.0%)	1.200	1.225	1.250	
V_R	Reverse Breakdown Voltage Tolerance	LM4041A		± 1.2	± 9.2	mV	
		LM4041B		± 2.4	± 10.4		
		LM4041C		± 6	± 14		
		LM4041D		± 12	± 24		
		LM4041E		± 25	± 36		
I_{R_MIN}	Minimum Operating Current			45	65	μA	
$\Delta V_R/\Delta T$	Reverse Breakdown Voltage Temperature Coefficient	$I_R = 10 \text{ mA}$			± 20	ppm/ $^\circ\text{C}$	
		$I_R = 1 \text{ mA}$	LM4041A, B, C		± 15		± 100
			LM4041D, E		± 15		± 150
$I_R = 100 \mu\text{A}$			± 15				
$\Delta V_R/\Delta I_R$	Reverse Breakdown Voltage Change with Operating Current	$I_{R_MIN} \leq I_R \leq 1 \text{ mA}$	LM4041A, B, C		0.7	2.0	mV
			LM4041D, E		0.7	2.5	
		$1 \text{ mA} \leq I_R \leq 15 \text{ mA}$	LM4041A, B, C		2.5	8	
			LM4041D, E		2.5	10	
Z_R	Reverse Dynamic Impedance	$I_R = 1 \text{ mA}$, $f = 120 \text{ Hz}$, $I_{AC} = 0.1 I_R$	LM4041A, B		0.5	1.5	Ω
			LM4041C		0.5	1.5	
			LM4041D, E		0.5	2.0	
e_N	Wideband Noise	$I_R = 100 \mu\text{A}$, $10 \text{ Hz} \leq f \leq 10 \text{ KHz}$			200	μV_{RMS}	
ΔV_R	Reverse Breakdown Voltage Long Term Stability	$T = 1000 \text{ h}$			120	ppm	
V_{HYST}	Thermal Hysteresis (Note 2)	$\Delta T = -40^\circ\text{C}$ to $+125^\circ\text{C}$			0.08	%	

2.500 V

V_R	Reverse Breakdown Voltage	$T_A = +25^\circ\text{C}$	LM4040A (0.1%)	2.498	2.500	2.502	V
			LM4040B (0.2%)	2.496	2.500	2.504	
			LM4040C (0.5%)	2.490	2.500	2.510	
			LM4040D (1.0%)	2.475	2.500	2.525	
			LM4040E (2.0%)	2.450	2.500	2.550	
V_R	Reverse Breakdown Voltage Tolerance	LM4040A		± 2	± 19	mV	
		LM4040B		± 4	± 21		
		LM4040C		± 10	± 29		
		LM4040D		± 25	± 49		
		LM4040E		± 50	± 74		

1. Guaranteed by design.

2. Thermal hysteresis is defined as the difference in voltage measured at $+25^\circ\text{C}$ after cycling to temperature -40°C and the 25°C measurement after cycling to temperature $+125^\circ\text{C}$.

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Table 5. DC ELECTRICAL CHARACTERISTICS

 ($I_R = 100 \mu A$, $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted. Typical values are at $T_A = +25^\circ C$.)

Symbol	Parameter	Test Conditions	Limits			Units	
			Min	Typ	Max		
2.500 V							
I_{R_MIN}	Minimum Operating Current			45	65	μA	
$\Delta V_R/\Delta T$	Reverse Breakdown Voltage Temperature Coefficient	$I_R = 10 \text{ mA}$		± 20		ppm/ $^\circ C$	
		$I_R = 1 \text{ mA}$	LM4040A, B, C	± 15	± 100		
			LM4040D, E	± 15	± 150		
	$I_R = 100 \mu A$		± 15				
$\Delta V_R/\Delta I_R$	Reverse Breakdown Voltage Change with Operating Current	$I_{R_MIN} \leq I_R \leq 1 \text{ mA}$	LM4040A, B, C	0.3	1.0	mV	
			LM4040D, E	0.3	1.2		
		$1 \text{ mA} \leq I_R \leq 15 \text{ mA}$	LM4040A, B, C	2.5	8		
			LM4040D, E	2.5	10		
Z_R	Reverse Dynamic Impedance	$I_R = 1 \text{ mA}$, $f = 120 \text{ Hz}$, $I_{AC} = 0.1 I_R$	LM4040A, B	0.3	0.8	Ω	
			LM4040C	0.3	0.9		
			LM4040D, E	0.3	1.1		
e_N	Wideband Noise	$I_R = 100 \mu A$, $10 \text{ Hz} \leq f \leq 10 \text{ KHz}$		350		μV_{RMS}	
ΔV_R	Reverse Breakdown Voltage Long Term Stability	$T = 1000 \text{ h}$		120		ppm	
V_{HYST}	Thermal Hysteresis (Note 2)	$\Delta T = -40^\circ C$ to $+125^\circ C$		0.08		%	
3.000 V							
V_R	Reverse Breakdown Voltage	$T_A = +25^\circ C$	LM4040A (0.1%)	2.997	3.000	3.003	V
			LM4040B (0.2%)	2.994	3.000	3.006	
			LM4040C (0.5%)	2.985	3.000	3.015	
			LM4040D (1.0%)	2.970	3.000	3.030	
			LM4040E (2.0%)	2.940	3.000	3.060	
V_R	Reverse Breakdown Voltage Tolerance	LM4040A		± 3	± 22	mV	
		LM4040B		± 6	± 26		
		LM4040C		± 15	± 34		
		LM4040D		± 30	± 59		
		LM4040E		± 60	± 89		
I_{R_MIN}	Minimum Operating Current			45	65	μA	
$\Delta V_R/\Delta T$	Reverse Breakdown Voltage Temperature Coefficient	$I_R = 10 \text{ mA}$		± 20		ppm/ $^\circ C$	
		$I_R = 1 \text{ mA}$	LM4040A, B, C	± 15	± 100		
			LM4040D, E	± 15	± 150		
	$I_R = 100 \mu A$		± 15				
$\Delta V_R/\Delta I_R$	Reverse Breakdown Voltage Change with Operating Current	$I_{R_MIN} \leq I_R \leq 1 \text{ mA}$	LM4040A, B, C	0.4	1.1	mV	
			LM4040D, E	0.4	1.3		
		$1 \text{ mA} \leq I_R \leq 15 \text{ mA}$	LM4040A, B, C	2.7	9		
			LM4040D, E	2.7	11		

1. Guaranteed by design.

 2. Thermal hysteresis is defined as the difference in voltage measured at $+25^\circ C$ after cycling to temperature $-40^\circ C$ and the $25^\circ C$ measurement after cycling to temperature $+125^\circ C$.

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Table 5. DC ELECTRICAL CHARACTERISTICS

 ($I_R = 100 \mu\text{A}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise noted. Typical values are at $T_A = +25^\circ\text{C}$.)

Symbol	Parameter	Test Conditions	Limits			Units	
			Min	Typ	Max		
3.000 V							
Z_R	Reverse Dynamic Impedance	$I_R = 1 \text{ mA}$, $f = 120 \text{ Hz}$, $I_{AC} = 0.1 I_R$	LM4040A, B		0.4	0.9	Ω
			LM4040C		0.4	0.9	
			LM4040D, E		0.4	1.2	
e_N	Wideband Noise	$I_R = 100 \mu\text{A}$, $10 \text{ Hz} \leq f \leq 10 \text{ KHz}$		350		μV_{RMS}	
ΔV_R	Reverse Breakdown Voltage Long Term Stability	$T = 1000 \text{ h}$		120		ppm	
V_{HYST}	Thermal Hysteresis (Note 2)	$\Delta T = -40^\circ\text{C}$ to $+125^\circ\text{C}$		0.08		%	

3.300 V

V_R	Reverse Breakdown Voltage	$T_A = +25^\circ\text{C}$	LM4040A (0.1%)	3.297	3.300	3.303	V
			LM4040B (0.2%)	3.294	3.300	3.306	
V_R	Reverse Breakdown Voltage	$T_A = +25^\circ\text{C}$	LM4040C (0.5%)	3.285	3.300	3.315	V
			LM4040D (1.0%)	3.270	3.300	3.330	
V_R	Reverse Breakdown Voltage Tolerance	LM4040A			± 3	± 22	mV
		LM4040B			± 6	± 26	
		LM4040C			± 15	± 34	
		LM4040D			± 30	± 59	
I_{R_MIN}	Minimum Operating Current			45	65	μA	
$\Delta V_R/\Delta T$	Reverse Breakdown Voltage Temperature Coefficient	$I_R = 10 \text{ mA}$			± 20		ppm/ $^\circ\text{C}$
		$I_R = 1 \text{ mA}$	LM4040A, B, C		± 15	± 100	
			LM4040D		± 15	± 150	
$I_R = 100 \mu\text{A}$			± 15				
$\Delta V_R/\Delta I_R$	Reverse Breakdown Voltage Change with Operating Current	$I_{R_MIN} \leq I_R \leq 1 \text{ mA}$	LM4040A, B, C		0.3	1.0	mV
			LM4040D		0.3	1.2	
		$1 \text{ mA} \leq I_R \leq 15 \text{ mA}$	LM4040A, B, C		2.5	8	
			LM4040D		2.5	10	
Z_R	Reverse Dynamic Impedance	$I_R = 1 \text{ mA}$, $f = 120 \text{ Hz}$, $I_{AC} = 0.1 I_R$	LM4040A, B		0.3	0.8	Ω
			LM4040C		0.3	0.9	
			LM4040D		0.3	1.1	
e_N	Wideband Noise	$I_R = 100 \mu\text{A}$, $10 \text{ Hz} \leq f \leq 10 \text{ KHz}$		350		μV_{RMS}	
ΔV_R	Reverse Breakdown Voltage Long Term Stability	$T = 1000 \text{ h}$		120		ppm	
V_{HYST}	Thermal Hysteresis (Note 2)	$\Delta T = -40^\circ\text{C}$ to $+125^\circ\text{C}$		0.08		%	

4.096 V

V_R	Reverse Breakdown Voltage	$T_A = +25^\circ\text{C}$	LM4040A (0.1%)	4.092	4.096	4.100	V
			LM4040B (0.2%)	4.088	4.096	4.104	
			LM4040C (0.5%)	4.080	4.096	4.120	
			LM4040D (1.0%)	4.055	4.096	4.137	

1. Guaranteed by design.

 2. Thermal hysteresis is defined as the difference in voltage measured at $+25^\circ\text{C}$ after cycling to temperature -40°C and the 25°C measurement after cycling to temperature $+125^\circ\text{C}$.

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Table 5. DC ELECTRICAL CHARACTERISTICS

($I_R = 100 \mu\text{A}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise noted. Typical values are at $T_A = +25^\circ\text{C}$.)

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ	Max	
4.096 V						
V_R	Reverse Breakdown Voltage Tolerance	LM4040A		± 4	± 31	mV
		LM4040B		± 8	± 35	
		LM4040C		± 20	± 47	
		LM4040D		± 41	± 80	
I_{R_MIN}	Minimum Operating Current		45	65	μA	
$\Delta V_R/\Delta T$	Reverse Breakdown Voltage Temperature Coefficient	$I_R = 10 \text{ mA}$		± 30		ppm/ $^\circ\text{C}$
		$I_R = 1 \text{ mA}$	LM4040A, B, C	± 20	± 100	
			LM4040D	± 20	± 150	
$I_R = 100 \mu\text{A}$		± 15				
$\Delta V_R/\Delta I_R$	Reverse Breakdown Voltage Change with Operating Current	$I_{R_MIN} \leq I_R \leq 1 \text{ mA}$	LM4040A, B, C	0.5	1.2	mV
			LM4040D	0.5	1.5	
		$1 \text{ mA} \leq I_R \leq 15 \text{ mA}$	LM4040A, B, C	3.0	10	
			LM4040D	3.0	13	
Z_R	Reverse Dynamic Impedance	$I_R = 1 \text{ mA}$, $f = 120 \text{ Hz}$, $I_{AC} = 0.1 I_R$	LM4040A, B	0.5	1.0	Ω
			LM4040C	0.5	1.0	
			LM4040D	0.5	1.3	
e_N	Wideband Noise	$I_R = 100 \mu\text{A}$, $10 \text{ Hz} \leq f \leq 10 \text{ KHz}$		800		μV_{RMS}
ΔV_R	Reverse Breakdown Voltage Long Term Stability	$T = 1000 \text{ h}$		120		ppm
V_{HYST}	Thermal Hysteresis (Note 2)	$\Delta T = -40^\circ\text{C}$ to $+125^\circ\text{C}$		0.08		%

5.000 V

V_R	Reverse Breakdown Voltage	$T_A = +25^\circ\text{C}$	LM4040A (0.1%)	4.995	5.000	5.005	V
			LM4040B (0.2%)	4.990	5.000	5.010	
			LM4040C (0.5%)	4.975	5.000	5.025	
			LM4040D (1.0%)	4.950	5.000	5.050	
V_R	Reverse Breakdown Voltage Tolerance	LM4040A		± 5	± 38	mV	
		LM4040B		± 10	± 43		
		LM4040C		± 25	± 58		
		LM4040D		± 50	± 99		
I_{R_MIN}	Minimum Operating Current		45	65	μA		
$\Delta V_R/\Delta T$	Reverse Breakdown Voltage Temperature Coefficient	$I_R = 10 \text{ mA}$		± 30		ppm/ $^\circ\text{C}$	
		$I_R = 1 \text{ mA}$	LM4040A, B, C	± 20	± 100		
			LM4040D	± 20	± 150		
$I_R = 100 \mu\text{A}$		± 15					

1. Guaranteed by design.

2. Thermal hysteresis is defined as the difference in voltage measured at $+25^\circ\text{C}$ after cycling to temperature -40°C and the 25°C measurement after cycling to temperature $+125^\circ\text{C}$.

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Table 5. DC ELECTRICAL CHARACTERISTICS

($I_R = 100 \mu\text{A}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise noted. Typical values are at $T_A = +25^\circ\text{C}$.)

Symbol	Parameter	Test Conditions	Limits			Units	
			Min	Typ	Max		
5.000 V							
$\Delta V_R/\Delta I_R$	Reverse Breakdown Voltage Change with Operating Current	$I_{R_MIN} \leq I_R \leq 1 \text{ mA}$	LM4040A, B, C		0.5	1.4	mV
			LM4040D		05	1.8	
		$1 \text{ mA} \leq I_R \leq 15 \text{ mA}$	LM4040A, B, C		3.5	12	
			LM4040D		3.5	15	
Z_R	Reverse Dynamic Impedance	$I_R = 1 \text{ mA}$, $f = 120 \text{ Hz}$, $I_{AC} = 0.1 I_R$	LM4040A, B		0.5	1.1	Ω
			LM4040C		0.5	1.1	
			LM4040D		0.5	1.5	
e_N	Wideband Noise	$I_R = 100 \mu\text{A}$, $10 \text{ Hz} \leq f \leq 10 \text{ KHz}$		800		μV_{RMS}	
ΔV_R	Reverse Breakdown Voltage Long Term Stability	$T = 1000 \text{ h}$		120		ppm	
V_{HYST}	Thermal Hysteresis (Note 2)	$\Delta T = -40^\circ\text{C}$ to $+125^\circ\text{C}$		0.08		%	

1. Guaranteed by design.
2. Thermal hysteresis is defined as the difference in voltage measured at $+25^\circ\text{C}$ after cycling to temperature -40°C and the 25°C measurement after cycling to temperature $+125^\circ\text{C}$.

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TYPICAL PERFORMANCE CHARACTERISTICS

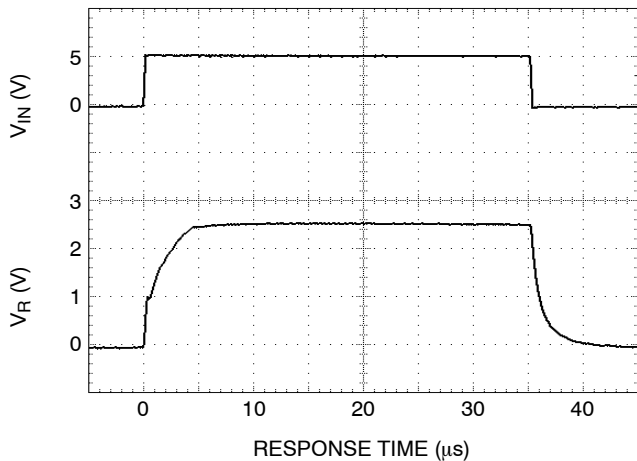


Figure 2. LM4040 – 2.5 V ($R_S = 30\text{ k}$)

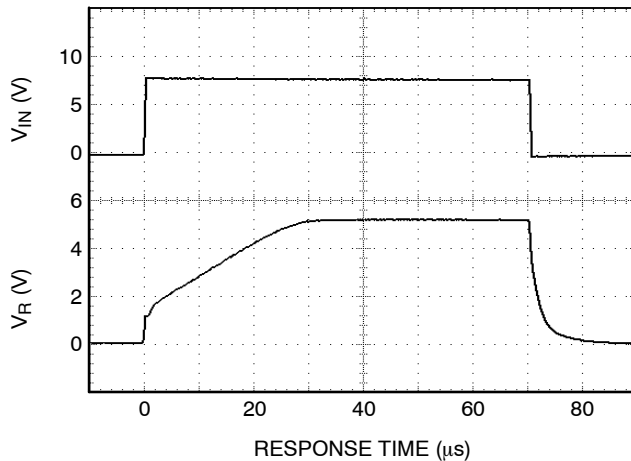


Figure 3. LM4040 – 5 V ($R_S = 30\text{ k}$)

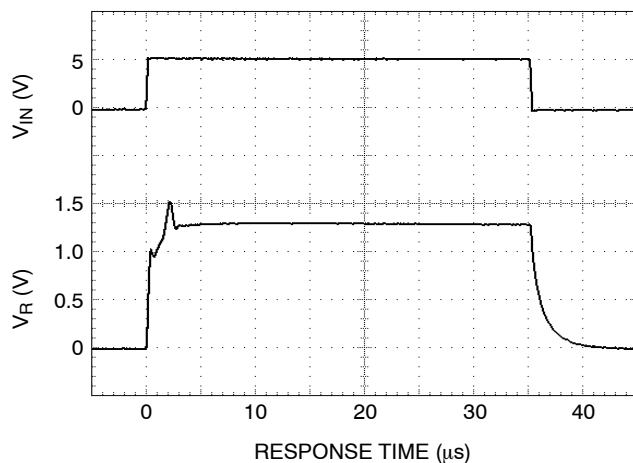


Figure 4. LM4041 – 1.225 V ($R_S = 30\text{ k}$)

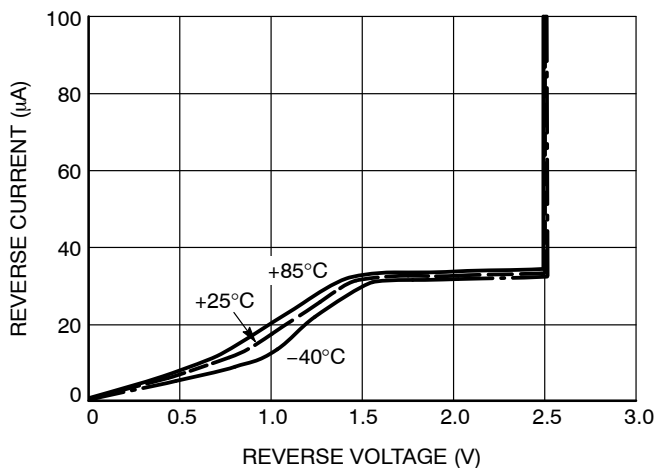


Figure 5. Reverse Characteristics (LM4040 – 2.5 V)

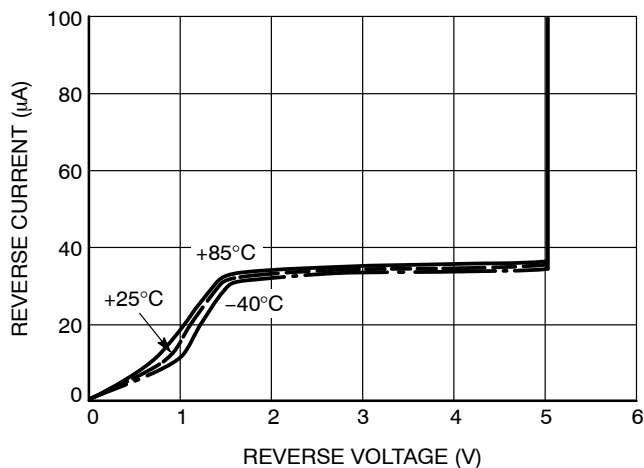


Figure 6. Reverse Characteristics (LM4040 – 5 V)

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TYPICAL PERFORMANCE CHARACTERISTICS

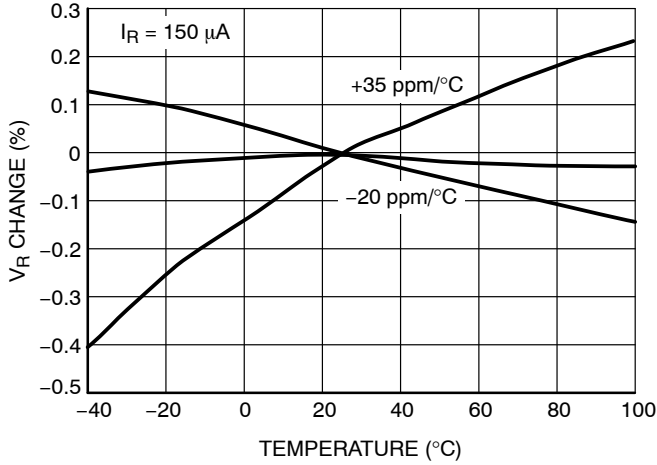


Figure 7. Temperature Drift - LM4040

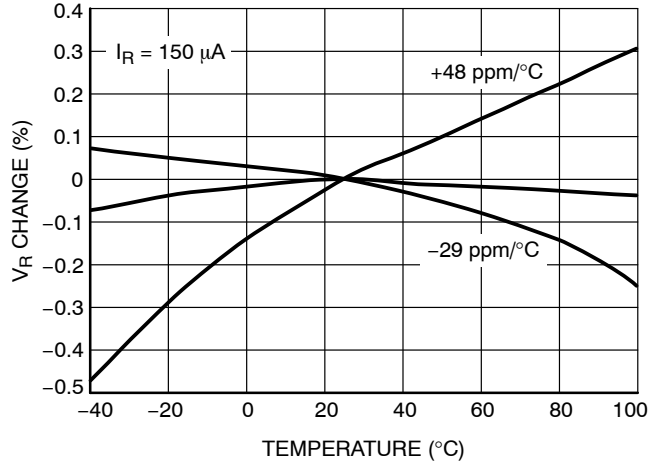


Figure 8. Temperature Drift - LM4041

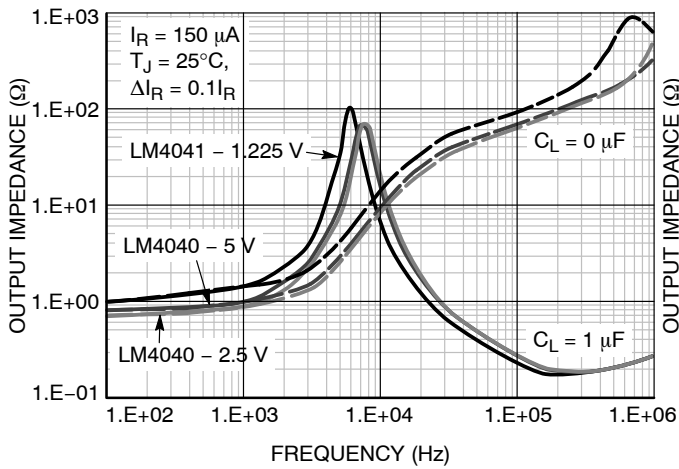


Figure 9. Output Impedance vs. Frequency

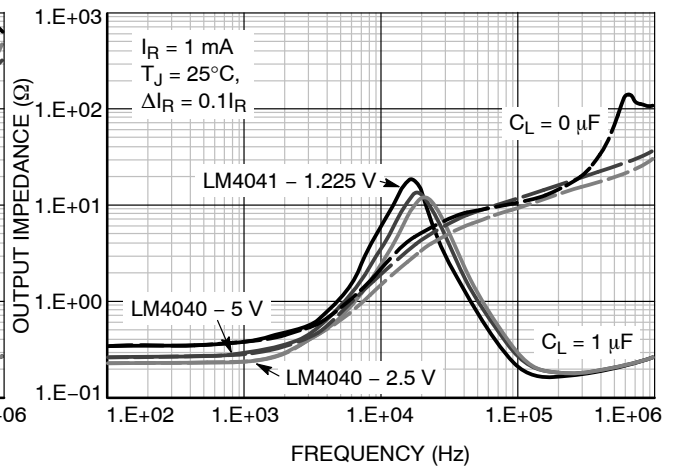


Figure 10. Output Impedance vs. Frequency

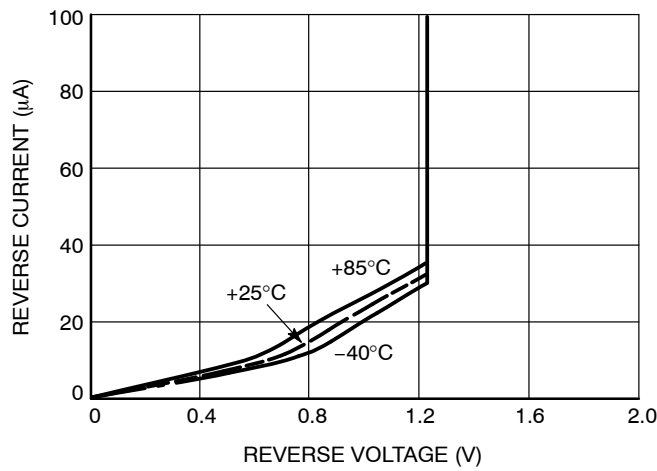


Figure 11. Reverse Characteristics - LM4041

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Device Description

The LM404x shunt references use ON Semiconductor's floating gate (EEPROM) technology to produce a capacitor which stores an accurate and stable voltage that is used as the reference voltage for a control amplifier and shunt N-channel FET.

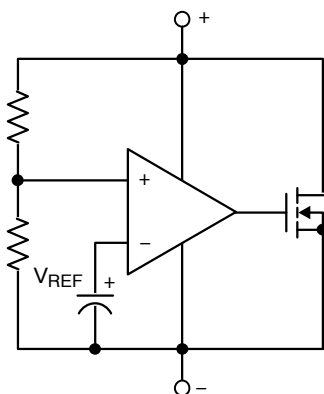


Figure 12. Functional Block Diagram

The device operates like a zener diode; maintaining a fixed voltage across its output terminals when biased with 60 μA to 15 mA of reverse current. The LM404x will also act like a silicon diode when forward biased with currents up to 10 mA.

Applications Information

The LM404x's internal pass transistor maintains a constant output voltage by sinking the necessary amount of current across a source resistor. The source resistance (R_S) is set by the load current range (I_{LOAD}), supply voltage (V_S) variations, LM404x's terminal voltage (V_R), and desired quiescent current.

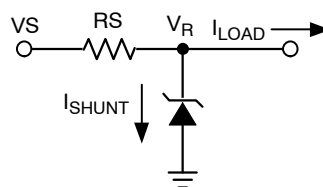


Figure 13. Typical Operating Circuit

To select a value of R_S , set V_S at its minimum value and I_{LOAD} at its maximum. Be sure to maintain a minimum operating current of 60 μA through LM404x at all times, as LM404x uses this current to power its internal circuitry. The R_S value should be large enough to keep I_{SHUNT} less than 15 mA for proper regulation when V_S is maximum and I_{LOAD} is at a minimum. Therefore, the value of R_S is bounded by the following equation:

$$\frac{(V_{S(\min)} - V_R)}{(60 \mu\text{A} + I_{LOAD(\max)})} > R_S$$

and

$$R_S > \frac{(V_{S(\max)} - V_R)}{(15 \text{ mA} + I_{LOAD(\min)})}$$

Choosing a larger resistance minimizes the power dissipated in the circuit by reducing the shunt current.

Output Capacitance

The LM404x does not require an external capacitor for frequency stability and is stable for any output capacitance.

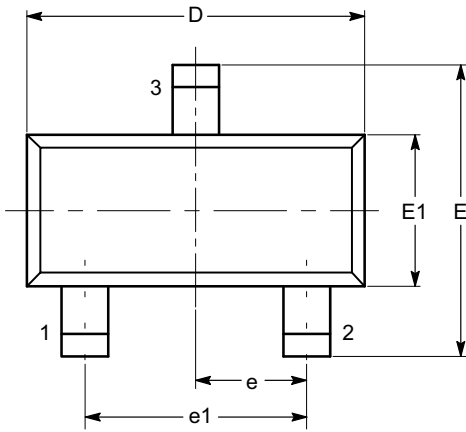
Effect of Temperature

LM404x has an output voltage temperature coefficient of typically ± 15 to ± 30 ppm/ $^{\circ}\text{C}$ meaning the LM404x's output voltage will change by 50 – 100 $\mu\text{V}/^{\circ}\text{C}$ for a 3.300 V regulator. The polarity of this temperature induced voltage shift can vary from device to device, some moving in the positive direction and others in the negative direction.

LM4040, LM4041

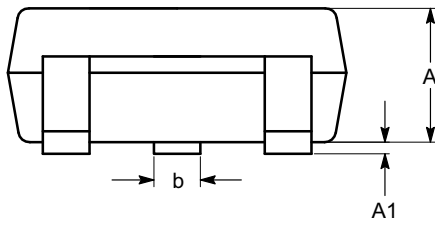
PACKAGE DIMENSIONS

SOT-23, 3 Lead
CASE 527AG-01
ISSUE O

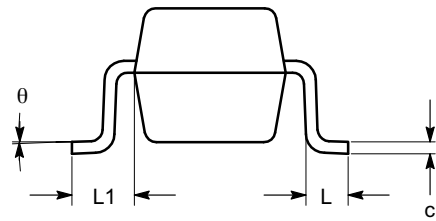


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	0.89		1.12
A1	0.013		0.10
b	0.37		0.50
c	0.085		0.18
D	2.80		3.04
E	2.10		2.64
E1	1.20		1.40
e	0.95 BSC		
e1	1.90 BSC		
L	0.40 REF		
L1	0.54 REF		
θ	0°		8°



SIDE VIEW



END VIEW

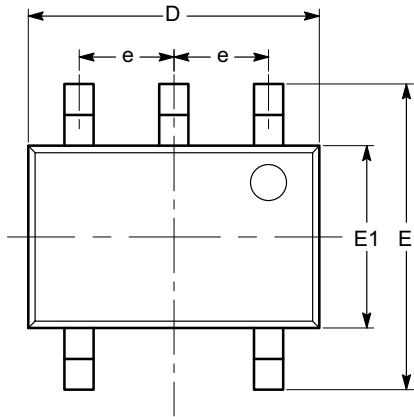
Notes:

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC TO-236.

LM4040, LM4041

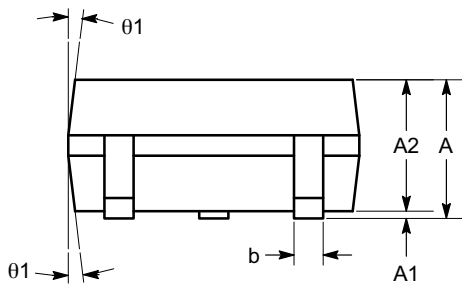
PACKAGE DIMENSIONS

SC-88A (SC-70 5 Lead), 1.25x2
CASE 419AC-01
ISSUE A

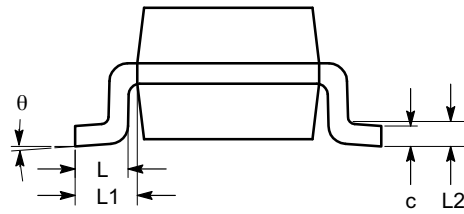


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	0.80		1.10
A1	0.00		0.10
A2	0.80		1.00
b	0.15		0.30
c	0.10		0.18
D	1.80	2.00	2.20
E	1.80	2.10	2.40
E1	1.15	1.25	1.35
e	0.65 BSC		
L	0.26	0.36	0.46
L1	0.42 REF		
L2	0.15 BSC		
θ	0°		8°
θ_1	4°		10°



SIDE VIEW



END VIEW

Notes:

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MO-203.

LM4040, LM4041

Table 6. ORDERING INFORMATION

Part Number	Specific Device Marking	Voltage	Accuracy	Max Drift	Temperature Range	Package (Note 3)	
LM4041ATB-122GT3	4M	1.225 V	±0.1%	100 ppm/°C	-40°C to 85°C	SOT-23-3	
LM4041BTB-122GT3			±0.2%				
LM4041CTB-122GT3			±0.5%				
LM4041DTB-122GT3			±1.0%,	150 ppm/°C			
LM4041ETB-122GT3			±2.0%,				
LM4040ATB-250GT3	4L	2.500 V	±0.1%	100 ppm/°C			
LM4040BTB-250GT3			±0.2%				
LM4040CTB-250GT3			±0.5%				
LM4040DTB-250GT3			±1.0%,	150 ppm/°C			
LM4040ETB-250GT3			±2.0%,				
LM4040ATB-300GT3		3.000 V	3.000 V	±0.1%			100 ppm/°C
LM4040BTB-300GT3				±0.2%			
LM4040CTB-300GT3				±0.5%			
LM4040DTB-300GT3				±1.0%,			150 ppm/°C
LM4040ETB-300GT3				±2.0%,			
LM4040ATB-330GT3		3.300 V	3.300 V	±0.1%	100 ppm/°C		
LM4040BTB-330GT3				±0.2%			
LM4040CTB-330GT3				±0.5%			
LM4040DTB-330GT3				±1.0%,	150 ppm/°C		
LM4040ETB-330GT3				±2.0%,			
LM4040ATB-409GT3	4.096 V	4.096 V	±0.1%	100 ppm/°C			
LM4040BTB-409GT3			±0.2%				
LM4040CTB-409GT3			±0.5%				
LM4040DTB-409GT3			±1.0%,	150 ppm/°C			
LM4040ETB-409GT3			±2.0%,				
LM4040ATB-500GT3	5.000 V	5.000 V	±0.1%	100 ppm/°C			
LM4040BTB-500GT3			±0.2%				
LM4040CTB-500GT3			±0.5%				
LM4040DTB-500GT3			±1.0%,	150 ppm/°C			
LM4040ETB-500GT3			±2.0%,				

3. Tape & Reel, 3,000 Units / Reel
4. All packages are RoHS-compliant (Lead-free, Halogen-free).
5. The standard lead finish is NiPdAu.
6. For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
7. For detailed information and a breakdown of device nomenclature and numbering systems, please see the ON Semiconductor Device Nomenclature document, TND310/D, available at www.onsemi.com


LM4040, LM4041

Table 6. ORDERING INFORMATION

Part Number	Specific Device Marking	Voltage	Accuracy	Max Drift	Temperature Range	Package (Note 3)	
LM4041 ASD -122GT3	4M	1.225 V	±0.1%	100 ppm/°C	-40°C to 85°C	SC-70-5	
LM4041 BSD -122GT3			±0.2%				
LM4041 CSD -122GT3			±0.5%				
LM4041 DSD -122GT3			±1.0%,	150 ppm/°C			
LM4041 ESD -122GT3			±2.0%,				
LM4040 ASD -250GT3	4L	2.500 V	±0.1%	100 ppm/°C			
LM4040 BSD -250GT3			±0.2%				
LM4040 CSD -250GT3			±0.5%				
LM4040 DSD -250GT3			±1.0%,	150 ppm/°C			
LM4040 ESD -250GT3			±2.0%,				
LM4040 ASD -300GT3		3.000 V	3.000 V	±0.1%			100 ppm/°C
LM4040 BSD -300GT3				±0.2%			
LM4040 CSD -300GT3				±0.5%			
LM4040 DSD -300GT3				±1.0%,			150 ppm/°C
LM4040 ESD -300GT3				±2.0%,			
LM4040 ASD -330GT3		3.300 V	3.300 V	±0.1%	100 ppm/°C		
LM4040 BSD -330GT3				±0.2%			
LM4040 CSD -330GT3				±0.5%			
LM4040 DSD -330GT3				±1.0%,	150 ppm/°C		
LM4040 ESD -330GT3				±2.0%,			
LM4040 ASD -409GT3	4.096 V	4.096 V	±0.1%	100 ppm/°C			
LM4040 BSD -409GT3			±0.2%				
LM4040 CSD -409GT3			±0.5%				
LM4040 DSD -409GT3			±1.0%,	150 ppm/°C			
LM4040 ESD -409GT3			±2.0%,				
LM4040 ASD -500GT3	5.000 V	5.000 V	±0.1%	100 ppm/°C			
LM4040 BSD -500GT3			±0.2%				
LM4040 CSD -500GT3			±0.5%				
LM4040 DSD -500GT3			±1.0%,	150 ppm/°C			
LM4040 ESD -500GT3			±2.0%,				

3. Tape & Reel, 3,000 Units / Reel
4. All packages are RoHS-compliant (Lead-free, Halogen-free).
5. The standard lead finish is NiPdAu.
6. For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
7. For detailed information and a breakdown of device nomenclature and numbering systems, please see the ON Semiconductor Device Nomenclature document, TND310/D, available at www.onsemi.com

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