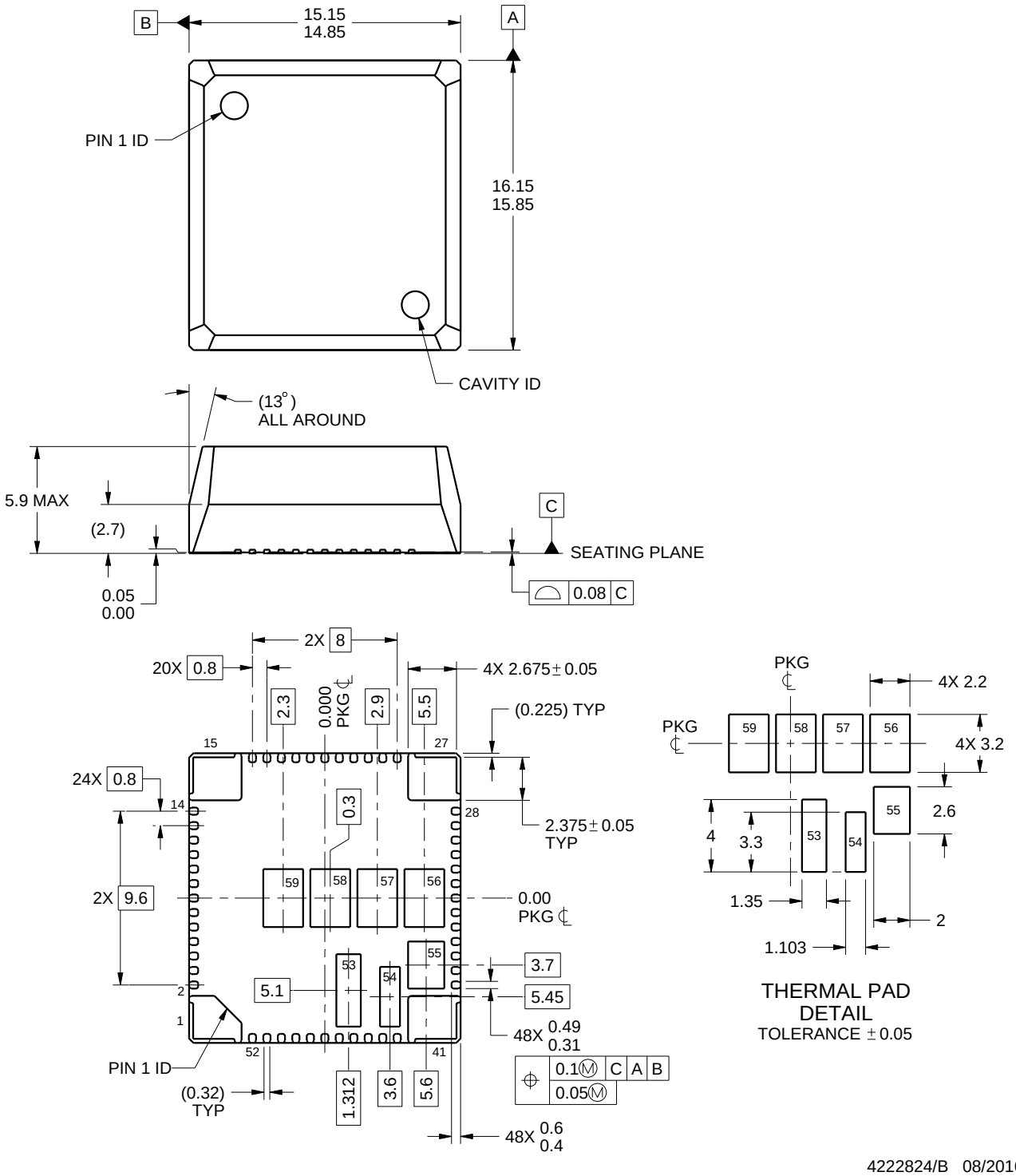
PACKAGE OUTLINE

RLG0059A

B4QFN - 5.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



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NOTES:

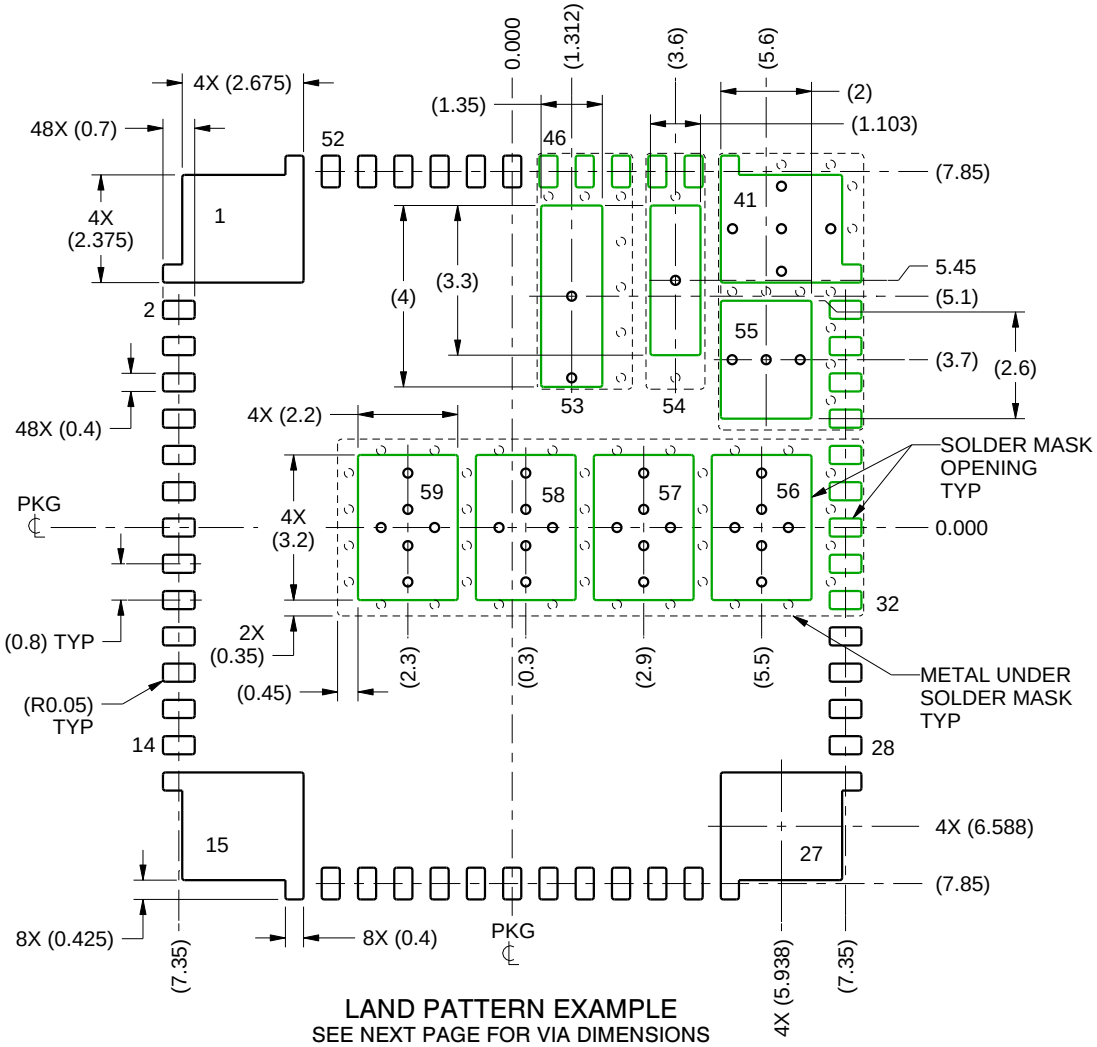
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pads must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

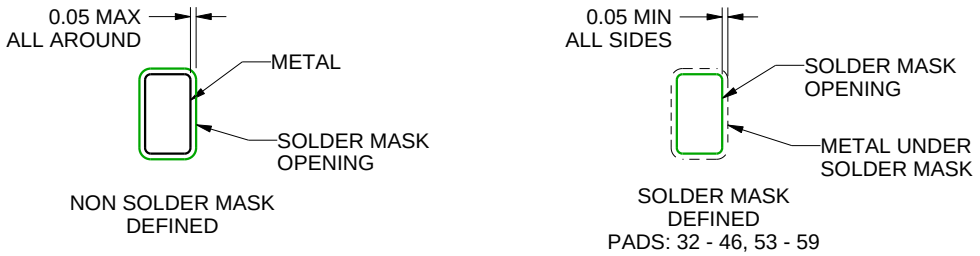
RLG0059A

B4QFN - 5.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SEE NEXT PAGE FOR VIA DIMENSIONS
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

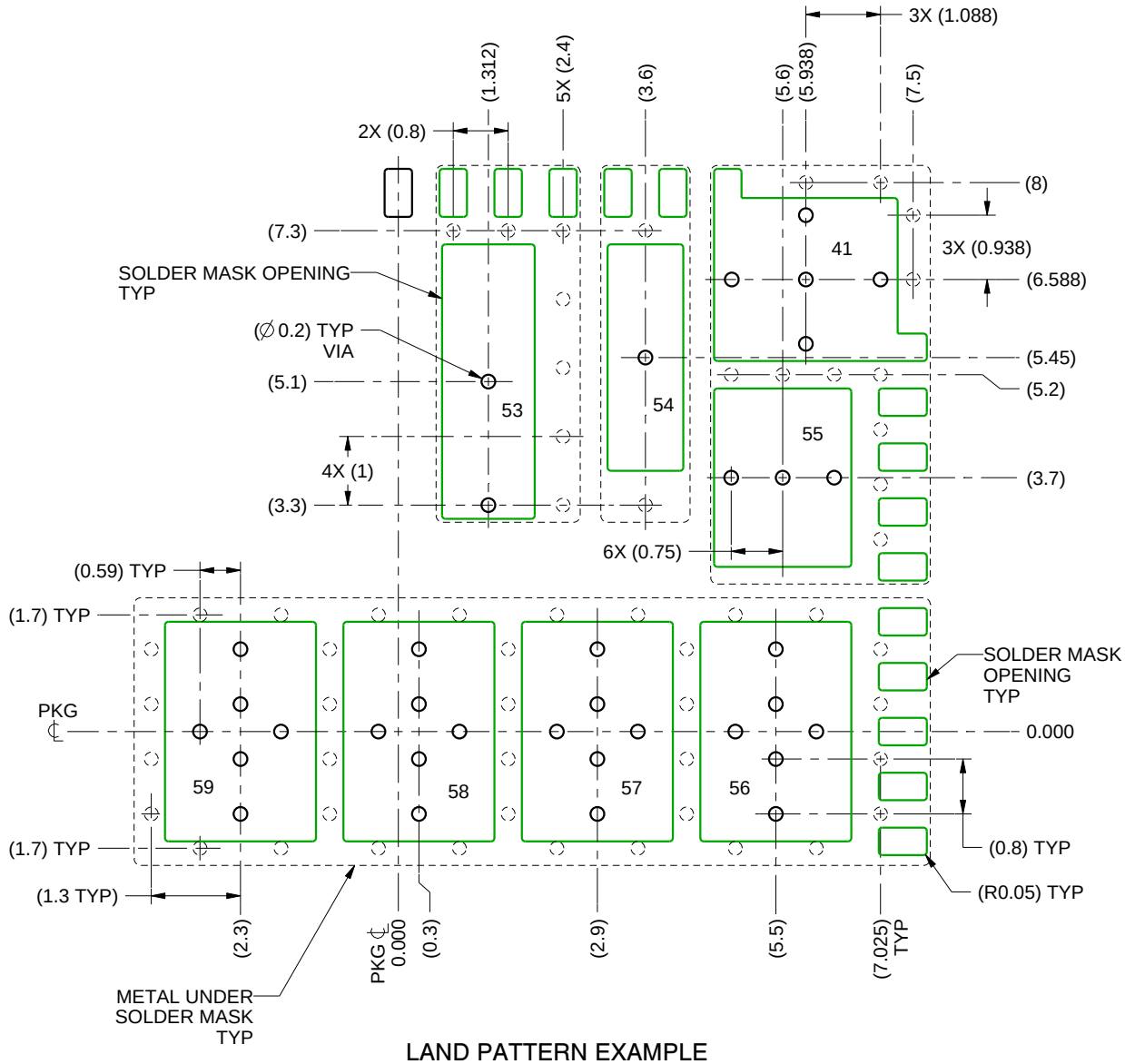
4. This package is designed to be soldered to the thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE BOARD LAYOUT

RLG0059A

B4QFN - 5.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
VIA DETAIL
SCALE:10X

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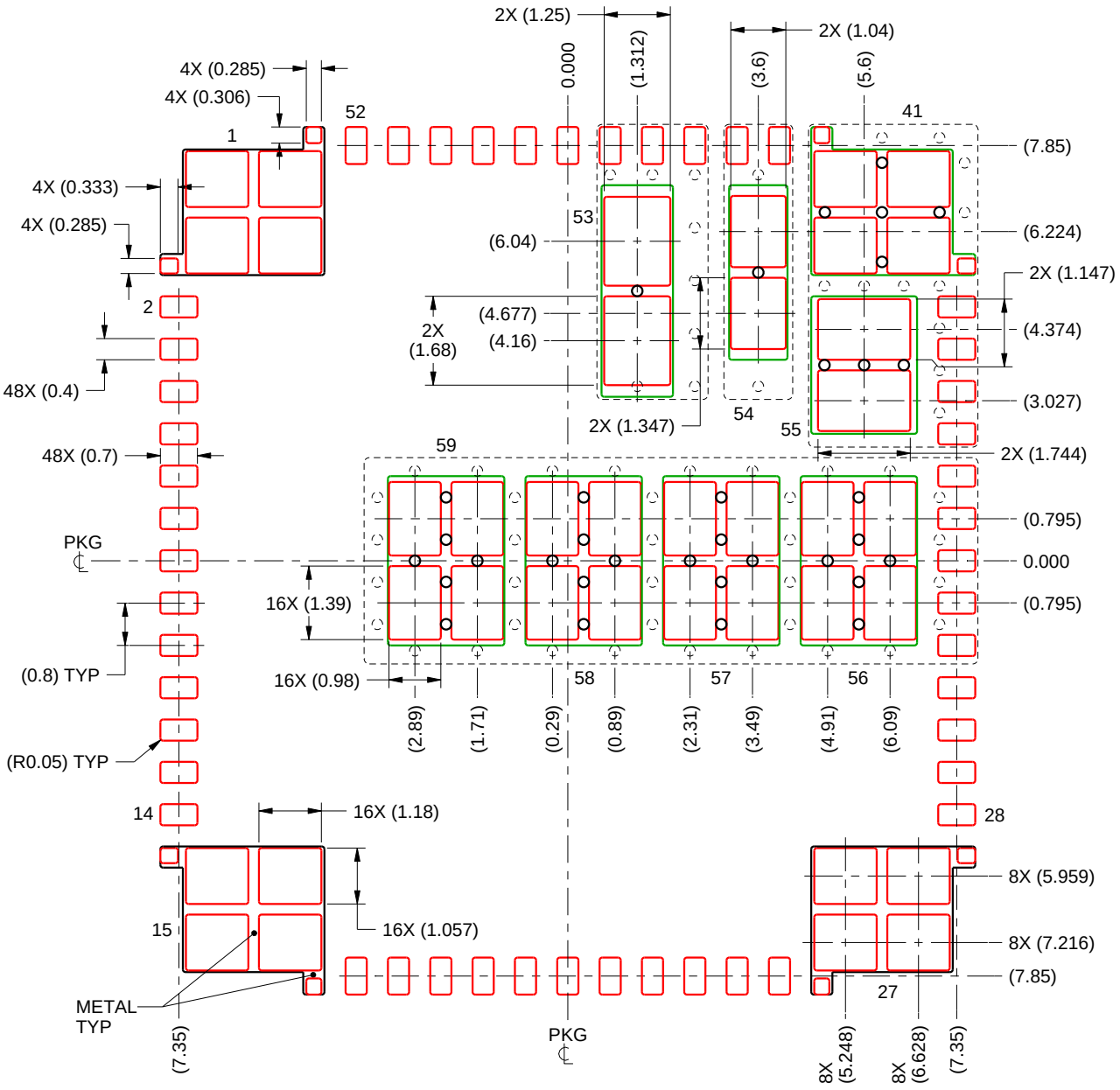
EXAMPLE STENCIL DESIGN

RLG0059A

B4QFN - 5.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS 1,15,27 & 41: 78.5%
PAD 53: 77.8%
PADS 54 & 55: 77%
PADS 56 - 59: 77.4%
SCALE:8X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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