

# p-channel JFETs designed for . . .

- Analog Switches
- Choppers
- Commutators
- Amplifiers

Performance Curves PE  
 See Section 5

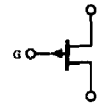
**BENEFITS**

- Low Insertion Loss  
 $R_{DS(on)} < 150 \Omega$  (2N3386)

**\*ABSOLUTE MAXIMUM RATINGS (25°C)**

Gate-Drain Voltage (Note 1)	30 V
Gate-Source Voltage (Note 1)	30 V
Gate Current	50 mA
Storage Temperature Range	-65 to +200°C
Total Dissipation at 25°C T <sub>A</sub> (Note 2)	300 mW

TO-72  
 See Section 7



**\*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

Characteristic	2N3382		2N3384		2N3386		Unit	Test Conditions
	Min	Max	Min	Max	Min	Max		
1   S T A T I C   IGSS   Gate Reverse Current		15		15		15	nA	VGS = 30 V VDS = 0
2   IGSS   Gate Reverse Current		15		15		15	μA	VGS = 5 V VDS = 0 TA = 150°C
3   BVGSS   Gate-Source Breakdown Voltage	30		30		30		V	IG = 1 μA VDS = 0
4   VGS(off)   Gate-Source Cutoff Voltage (Note 3)	1.0	5.0	4.0	5.0	4.0	9.5		VDS = -5 V ID = -1 μA
5   IDSS   Saturation Drain Current (Note 3)	-3.0	-30.0	-15.0	-30.0	-15.0	-50.0	mA	VDS = -10 V VGS = 0
6   ID(off)   Drain Cutoff Current		-2 (8)		-2 (8)		-2.5 (10)	nA (V)	VDS = -5 V VGS = ( )
7   rds(on)   Drain-Source ON Resistance		300		180		150	Ω	VGS = 0 VDS = 0
8   gfs   Common-Source Forward Transconductance (Note 3)	4500	12,500	7500	12,500	7500	15,000	μmho	VDS = -10 V VGS = 0 f = 1 kHz
9   Csgs + Cdgs   Source-Gate Capacitance Plus Drain-Gate Capacitance		6.0		6.0		6.0	pF	VDS = 0 VGS = 10 V f = 140 kHz
10   Ciss   Common-Source Input Capacitance	18 Typ							VDS = -5 V VGS = 1 V

\*JEDEC registered data.

**NOTE:**

1. Due to symmetrical geometry, units may be operated with source and drain leads interchanged.
2. Derate linearly to +175°C at 2 mW/°C
3. Pulsewidth = 2 ms, duty cycle ≤ 3%.

PE

