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2N5022
 2N5023

PNP SILICON TRANSISTOR

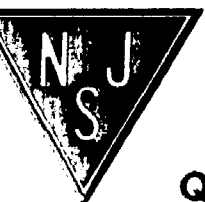
JEDEC TO-39 CASE

MAXIMUM RATINGS ($T_A=25^\circ\text{C}$ unless otherwise noted)

	SYMBOL	2N5022	2N5023	UNIT
Collector-Base Voltage	V_{CB0}	50	30	V
Collector-Emitter Voltage	V_{CE0}	50	30	V
Emitter-Base Voltage	V_{EB0}	5.0	5.0	V
Collector-Current-continuous	I_C	1.0	1.0	A
Power Dissipation, $T_A=25^\circ\text{C}$	P_D	1.0	1.0	W
Power Dissipation, $T_C=25^\circ\text{C}$	P_D	4.0	4.0	W
Operating and Storage Junction Temperature	T_J, T_{STG}	-65 TO +200		$^\circ\text{C}$
Thermal Resistance	θ_{JC}	43.8		$^\circ\text{C/W}$
Thermal Resistance	θ_{JA}	175		$^\circ\text{C/W}$

ELECTRICAL CHARACTERISTICS ($T_A=25^\circ\text{C}$ unless otherwise noted)

SYMBOL	TEST CONDITIONS	2N5022		2N5023		UNIT
		MIN	MAX	MIN	MAX	
I_{CES}	$V_{CE}=30\text{V}$		100		-	nA
I_{CES}	$V_{CE}=20\text{V}$		-		100	nA
I_{CES}	$V_{CE}=30\text{V}, T_A=100^\circ\text{C}$		15		-	μA
I_{CES}	$V_{CE}=20\text{V}, T_A=100^\circ\text{C}$		-		15	μA
BV_{CB0}	$I_C=100\mu\text{A}$	50		30		V
BV_{CES}	$I_C=100\mu\text{A}$	50		30		V
BV_{CE0}	$I_C=10\text{mA}$	50		30		V
BV_{EB0}	$I_E=100\mu\text{A}$	5		5		V
$V_{CE(SAT)}$	$I_C=100\text{mA}, I_B=10\text{mA}$		0.20		0.17	V
$V_{CE(SAT)}$	$I_C=500\text{mA}, I_B=50\text{mA}$		0.40		0.35	V
$V_{CE(SAT)}$	$I_C=1.0\text{A}, I_B=100\text{mA}$		0.80		0.70	V
$V_{BE(SAT)}$	$I_C=100\text{mA}, I_B=10\text{mA}$		1.0		1.0	V
$V_{BE(SAT)}$	$I_C=500\text{mA}, I_B=50\text{mA}$	0.8	1.4	0.8	1.4	V
$V_{BE(SAT)}$	$I_C=1.0\text{A}, I_B=100\text{mA}$		1.75		1.75	V
h_{FE}	$V_{CE}=1.0\text{V}, I_C=100\text{mA}$	15		30		
h_{FE}	$V_{CE}=1.0\text{V}, I_C=50\text{mA}$	25	100	40	100	
h_{FE}	$V_{CE}=5.0\text{V}, I_C=1.0\text{A}$	25		40		
h_{FE}	$V_{CE}=1.0\text{V}, I_C=500\text{mA}, T_A=-55^\circ\text{C}$	10		20		
f_T	$V_{CE}=10\text{V}, I_C=50\text{mA}, f=100\text{MHz}$	170		200		MHz
C_{ob}	$V_{BE}=10\text{V}, f=100\text{kHz}$		25		25	pF
C_{ib}	$V_{BE}=0.5\text{V}, f=100\text{kHz}$		100		100	pF
t_{on}	$V_{CE}=-30\text{V}, I_C=500\text{mA}, I_B=50\text{mA}$		40		40	ns
t_{off}	$V_{CE}=30\text{V}, I_C=500\text{mA}, I_{B1}=I_{B2}=50\text{mA}$		90		90	ns



NJ Semi-Conductors reserves the right to change test conditions, parameters limits and package dimensions without notice information furnished by NJ Semi-Conductors is believed to be both accurate and reliable at the time of going to press. However NJ Semi-Conductors assumes no responsibility for any errors or omissions discovered in its use. NJ Semi-Conductors encourages customers to verify that datasheets are current before placing orders.

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