

2SB1193

Silicon PNP epitaxial planar type darlington

For midium-speed power switching

Complementary to 2SD1773

■ Features

- High forward current transfer ratio h_{FE}
- High-speed switching
- Full-pack package which can be installed to the heat sink with one screw

■ Absolute Maximum Ratings $T_C = 25^\circ\text{C}$

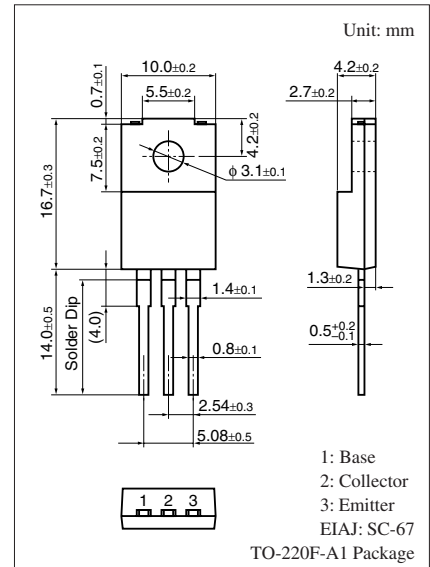
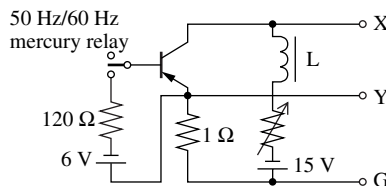
Parameter	Symbol	Rating	Unit
Collector-base voltage (Emitter open)	V_{CBO}	-120	V
Collector-emitter voltage (Base open)	V_{CEO}	-120	V
Emitter-base voltage (Collector open)	V_{EBO}	-7	V
Collector current	I_C	-8	A
Peak collector current	I_{CP}	-12	A
Collector power dissipation	P_C	50	W
		2	
Junction temperature	T_j	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 ~ +150	$^\circ\text{C}$

■ Electrical Characteristics $T_C = 25^\circ\text{C} \pm 3^\circ\text{C}$

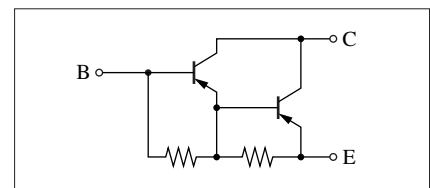
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Collector-emitter sustaining voltage *	$V_{CEO(SUS)}$	$I_C = -2\text{ A}$, $L = 10\text{ mH}$	-120			V
Emitter-base voltage (Collector open)	V_{EBO}	$I_E = -50\text{ mA}$, $I_C = 0$	-7			V
Collector-base cutoff current (Emitter open)	I_{CBO}	$V_{CB} = -120\text{ V}$, $I_E = 0$			-100	μA
Collector-emitter cutoff current (Base open)	I_{CEO}	$V_{CE} = -100\text{ V}$, $I_B = 0$			-10	μA
Forward current transfer ratio	h_{FE}	$V_{CE} = -3\text{ V}$, $I_C = -4\text{ A}$	1 000	20 000		—
Collector-emitter saturation voltage	$V_{CE(sat)1}$	$I_C = -4\text{ A}$, $I_B = -8\text{ mA}$			-1.5	V
	$V_{CE(sat)2}$	$I_C = -8\text{ A}$, $I_B = -80\text{ mA}$			-3.0	
Base-emitter saturation voltage	$V_{BE(sat)1}$	$I_C = -4\text{ A}$, $I_B = -8\text{ mA}$			-2.0	V
	$V_{BE(sat)2}$	$I_C = -8\text{ A}$, $I_B = -80\text{ mA}$			-3.5	
Transition frequency	f_T	$V_{CE} = -10\text{ V}$, $I_C = -0.5\text{ A}$, $f = 1\text{ MHz}$		15		MHz
Turn-on time	t_{on}	$I_C = -4\text{ A}$, $I_{B1} = -8\text{ mA}$, $I_{B2} = 8\text{ mA}$		0.7		μs
Storage time	t_{stg}	$V_{CC} = -50\text{ V}$		3.5		μs
Fall time	t_f			2.0		μs

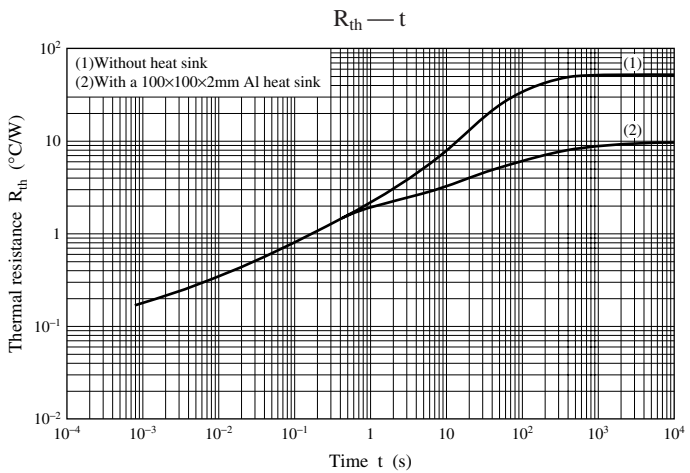
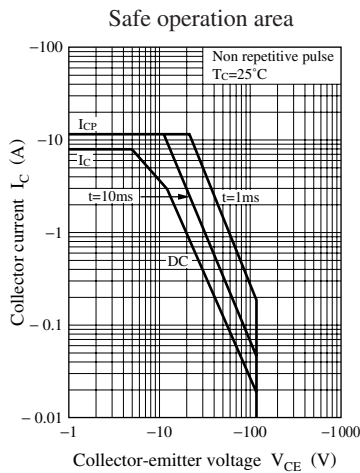
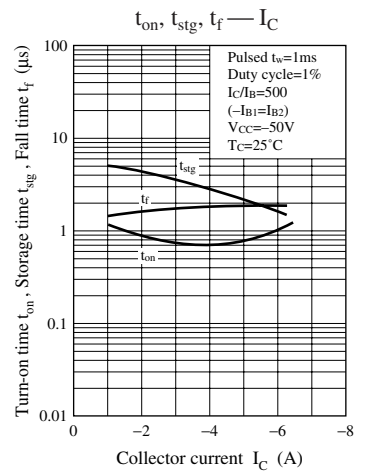
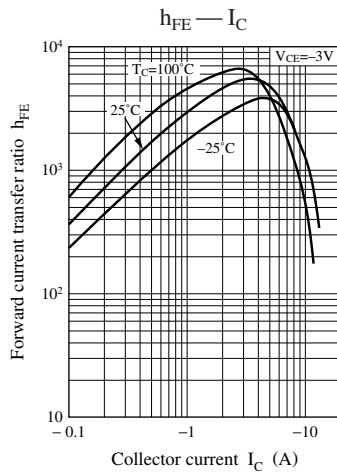
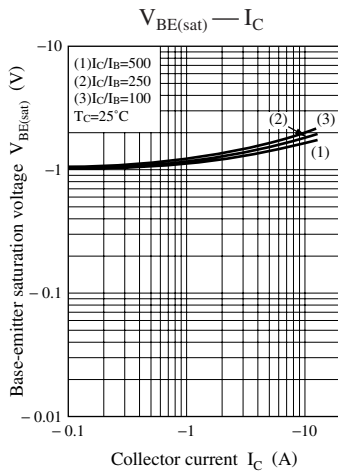
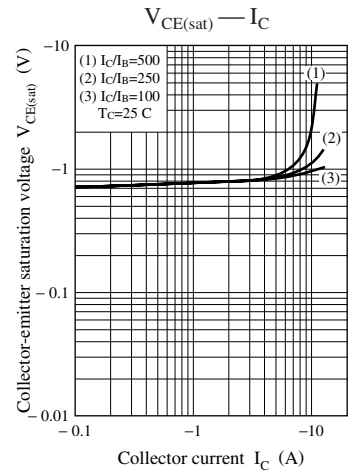
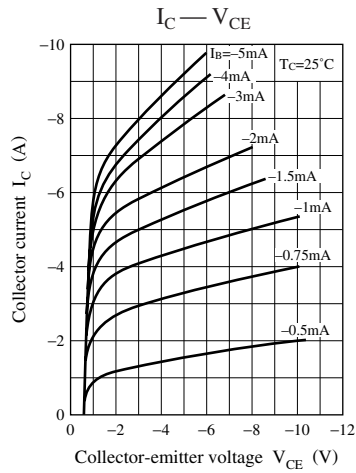
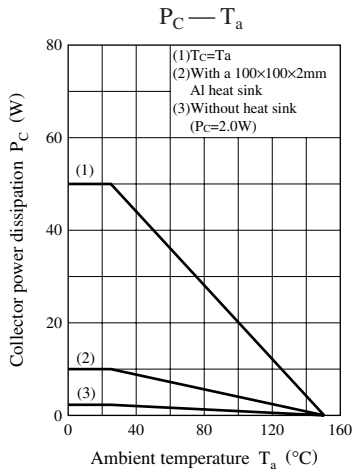
Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

2. *: $V_{CEO(SUS)}$ test circuit



Internal Connection





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