

# 2SD1747, 2SD1747A

## Silicon NPN epitaxial planar type

For power switching

### ■ Features

- Low collector-emitter saturation voltage  $V_{CE(sat)}$
- Satisfactory linearity of forward current transfer ratio  $h_{FE}$
- Large collector current  $I_C$
- I type package enabling direct soldering of the radiating fin to the printed circuit board, etc. of small electronic equipment

### ■ Absolute Maximum Ratings $T_C = 25^\circ\text{C}$

Parameter	Symbol	Rating	Unit	
Collector-base voltage (Emitter open)	2SD1747	$V_{CBO}$	130	V
	2SD1747A		150	
Collector-emitter voltage (Base open)	2SD1747	$V_{CEO}$	80	V
	2SD1747A		100	
Emitter-base voltage (Collector open)	$V_{EBO}$	7	V	
Collector current	$I_C$	7	A	
Peak collector current	$I_{CP}$	15	A	
Collector power dissipation	$P_C$		15	W
		$T_a = 25^\circ\text{C}$	1.3	
Junction temperature	$T_j$	150	$^\circ\text{C}$	
Storage temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$	

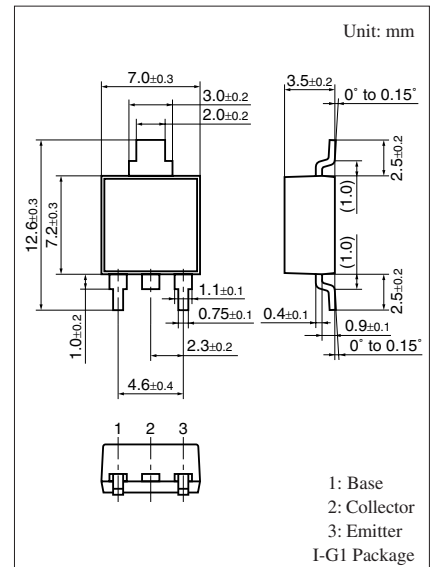
### ■ Electrical Characteristics $T_C = 25^\circ\text{C} \pm 3^\circ\text{C}$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Collector-emitter voltage (Base open)	2SD1747	$I_C = 10\text{ mA}, I_B = 0$	80			V
	2SD1747A		100			
Collector-base cutoff current (Emitter open)	$I_{CBO}$	$V_{CB} = 100\text{ V}, I_E = 0$			10	$\mu\text{A}$
Emitter-base cutoff current (Collector open)	$I_{EBO}$	$V_{EB} = 5\text{ V}, I_C = 0$			50	$\mu\text{A}$
Forward current transfer ratio	$h_{FE1}$	$V_{CE} = 2\text{ V}, I_C = 0.1\text{ A}$	45			—
	$h_{FE2}^*$	$V_{CE} = 2\text{ V}, I_C = 3\text{ A}$	90	260		
Collector-emitter saturation voltage	$V_{CE(sat)}$	$I_C = 5\text{ A}, I_B = 0.25\text{ A}$			0.5	V
Base-emitter saturation voltage	$V_{BE(sat)}$	$I_C = 5\text{ A}, I_B = 0.25\text{ A}$			1.5	V
Transition frequency	$f_T$	$V_{CE} = 10\text{ V}, I_C = 0.5\text{ A}, f = 10\text{ MHz}$		30		MHz
Turn-on time	$t_{on}$	$I_C = 3\text{ A}, I_{B1} = 0.3\text{ A}, I_{B2} = -0.3\text{ A}$		0.5		$\mu\text{s}$
Storage time	$t_{stg}$	$V_{CC} = 50\text{ V}$		1.5		$\mu\text{s}$
Fall time	$t_f$			0.2		$\mu\text{s}$

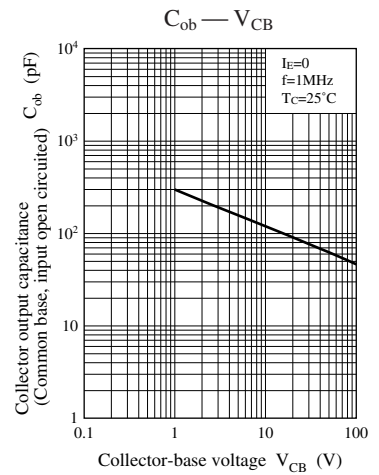
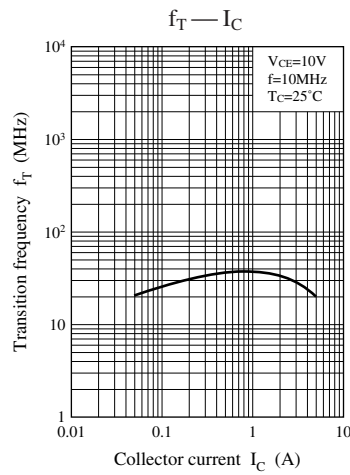
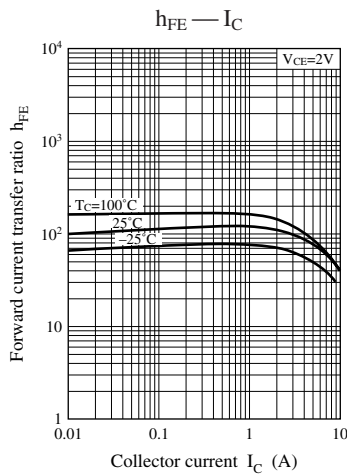
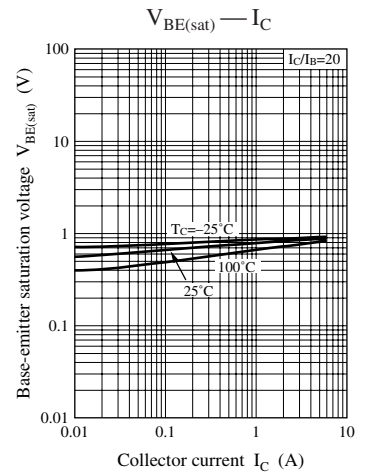
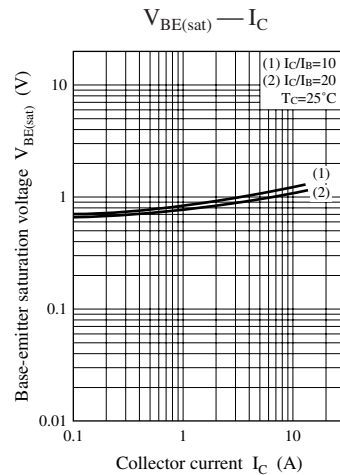
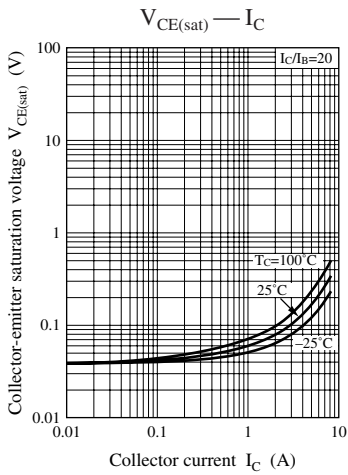
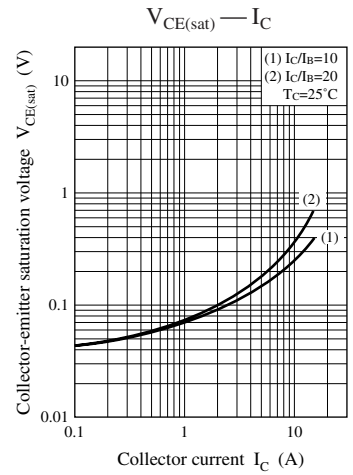
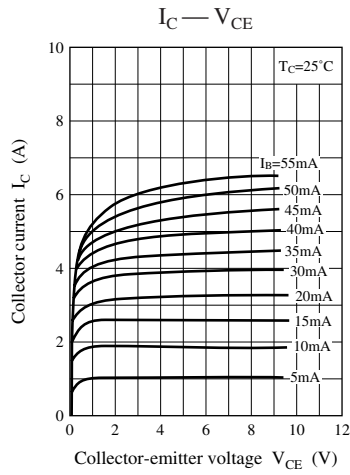
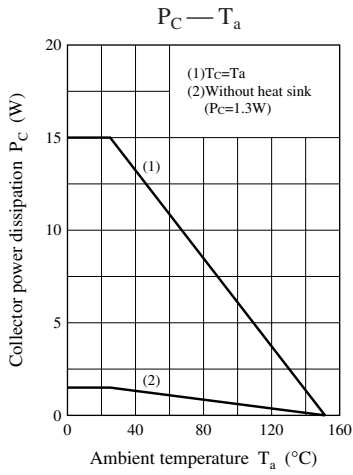
Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

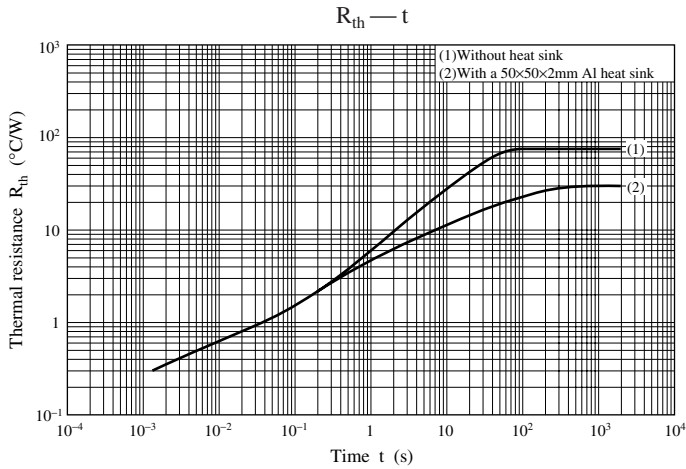
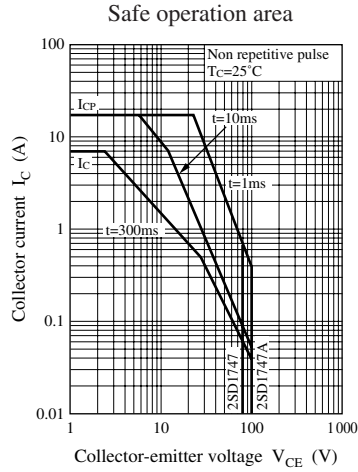
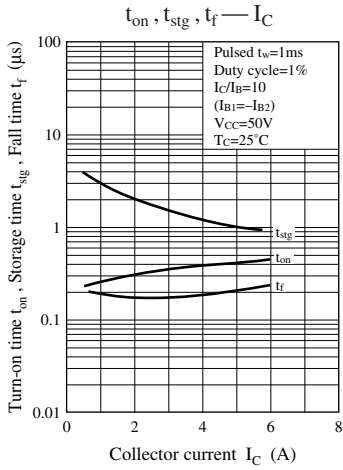
2. \*: Rank classification

Rank	Q	P
$h_{FE1}$	90 to 180	130 to 260



Note) Self-supported type package is also prepared.





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