

**2SK1065**

## High-Frequency General-Purpose Amplifier Applications

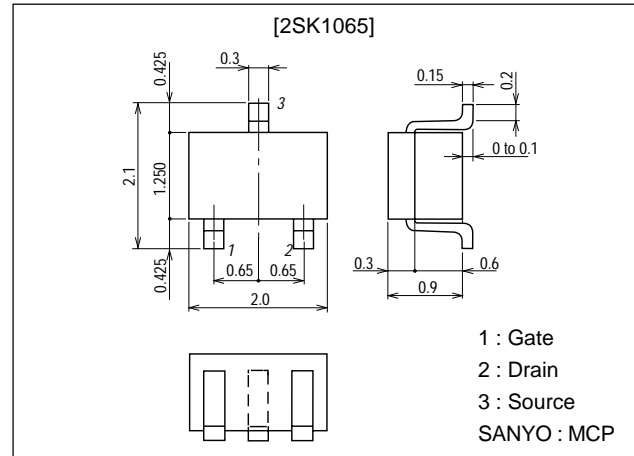
### Features

- Ultrasmall package facilitates miniaturization in end products.
- Small Crss (Crss=0.04pF typ).

### Package Dimensions

unit:mm

2057A



### Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Gate-to-Drain Voltage	V <sub>GDO</sub>		-20	V
Gate Current	I <sub>G</sub>		10	mA
Drain Current	I <sub>D</sub>		20	mA
Allowable Power Dissipation	P <sub>D</sub>		150	mW
Junction Temperature	T <sub>J</sub>		150	°C
Storage Temperature	T <sub>stg</sub>		-55 to +150	°C

Electrical Characteristics at Ta = 25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Gate-to-Drain Breakdown Voltage	V <sub>(BR)GDO</sub>	I <sub>G</sub> =-10μA	-20			V
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =-0.5V, V <sub>DS</sub> =0			-10	nA
Zero-Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =5V, V <sub>GS</sub> =0	1.2*		12.0*	mA
Cutoff Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> =5V, I <sub>D</sub> =10μA	-0.4	-1.3	-2.5	V
Forward Transfer Admittance	y <sub>fs</sub>   <sub>1</sub>	V <sub>DS</sub> =5V, V <sub>GS</sub> =0, f=1kHz	2.4	6.0		mS
	y <sub>fs</sub>   <sub>2</sub>	V <sub>DS</sub> =5V, V <sub>GS</sub> =0, f=100MHz	2.4	6.0		mS

\* : The 2SK1065 is classified by I<sub>DSS</sub> as follows (unit : mA) :

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I <sub>DSS</sub> rank	3	4	5
I <sub>DSS</sub>	1.2 to 3.0	2.5 to 6.0	5.0 to 12.0

(Note) Marking : T

- For CP package version, use the 2SK242.

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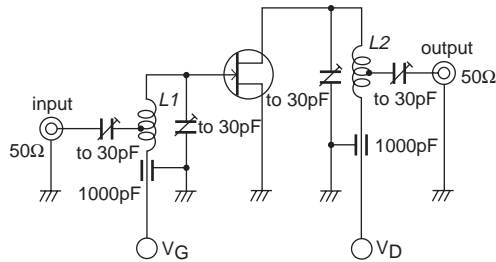
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

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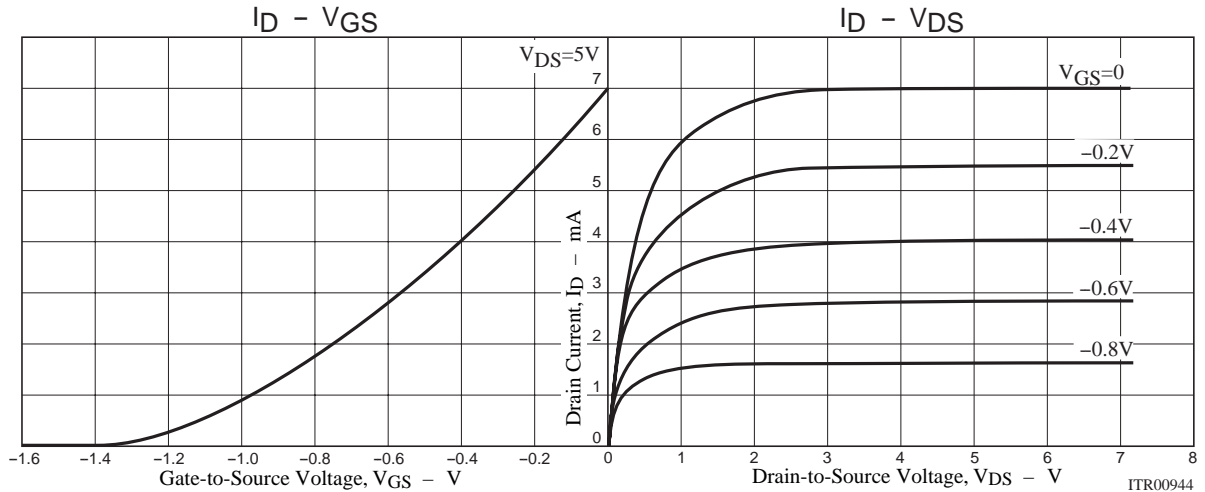
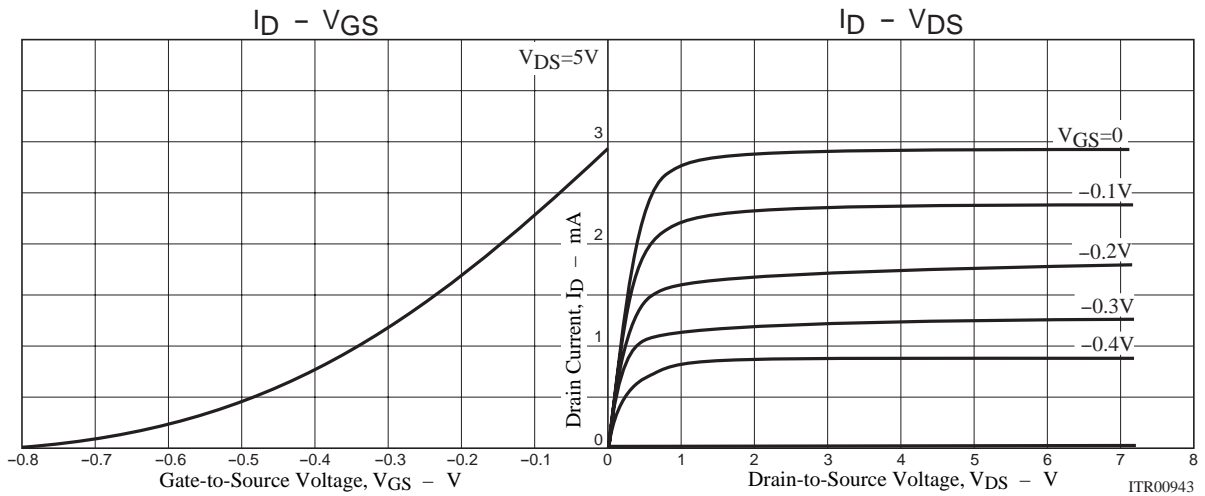
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Parameter	Symbol	Conditions	Ratings		Unit
Input Capacitance	Ciss	$V_{DS}=5V, V_{GS}=0, f=1MHz$	4.0		pF
Reverse Transfer Capacitance	Crss	$V_{DS}=5V, V_{GS}=0, f=1MHz$	0.04	0.15	pF
Output Capacitance	Coss	$V_{DS}=5V, V_{GS}=0, f=1MHz$	4.0		pF
Power Gain	PG	$V_{DS}=5V, V_{GS}=0, f=100MHz$ , See specified Test Circuit	24		dB
Noise Figure	NF	See specified Test Circuit	3.5	6.0	dB

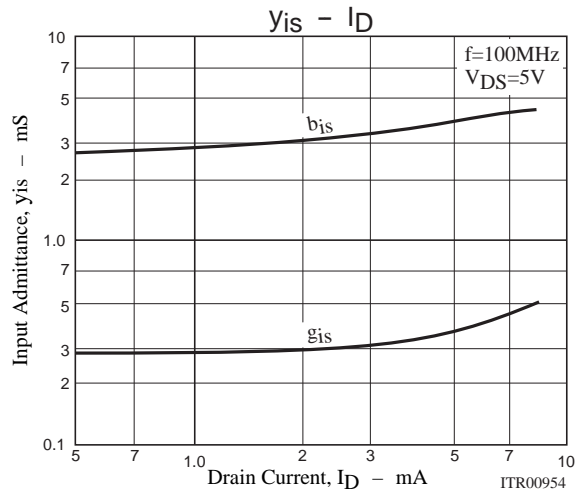
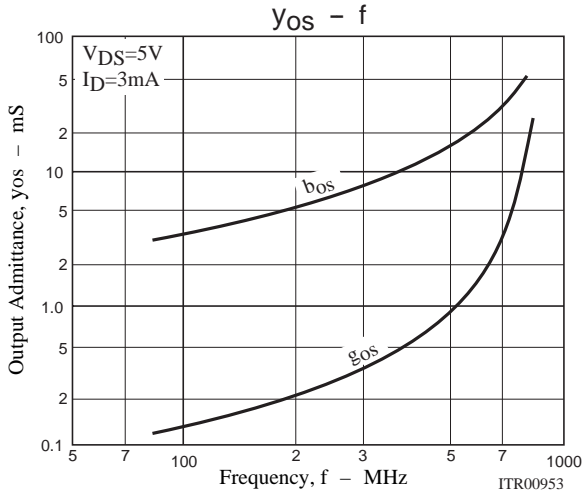
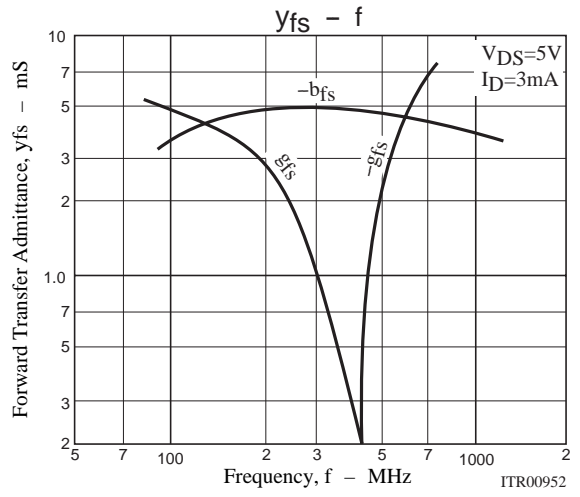
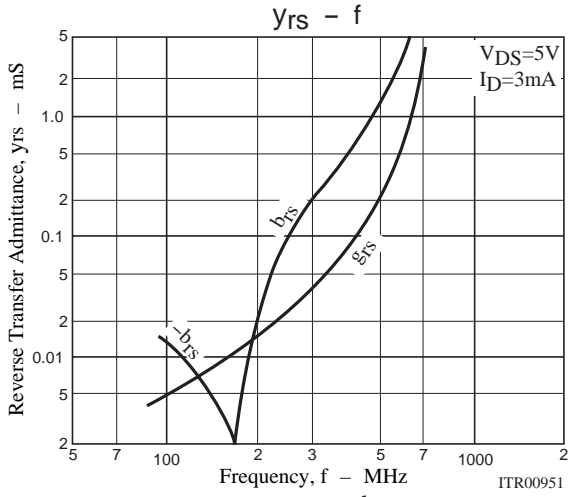
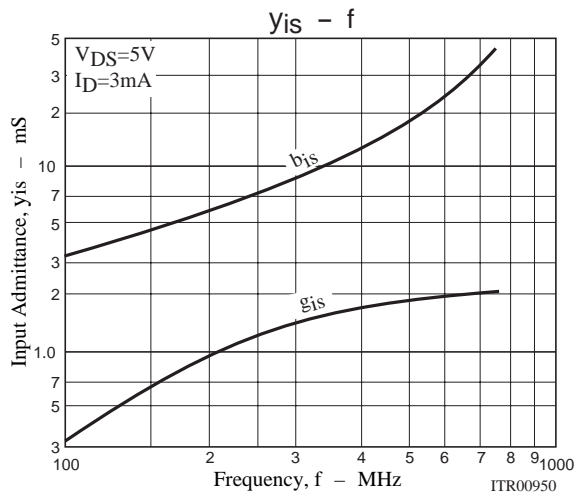
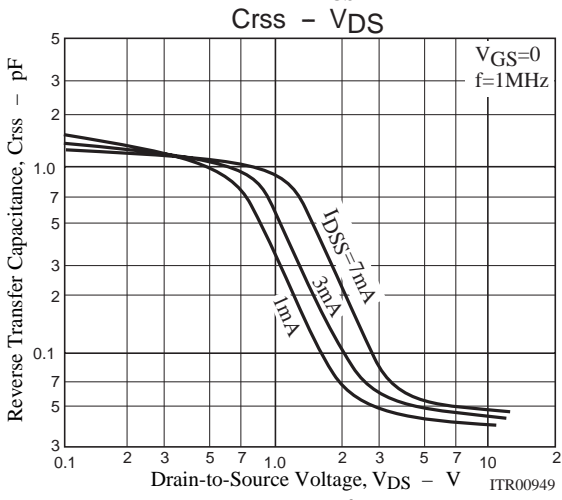
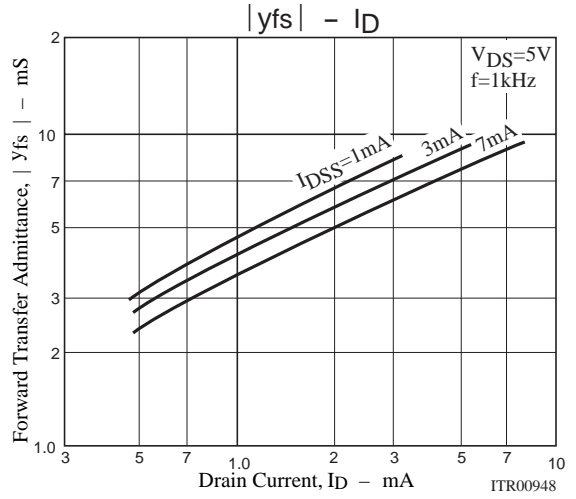
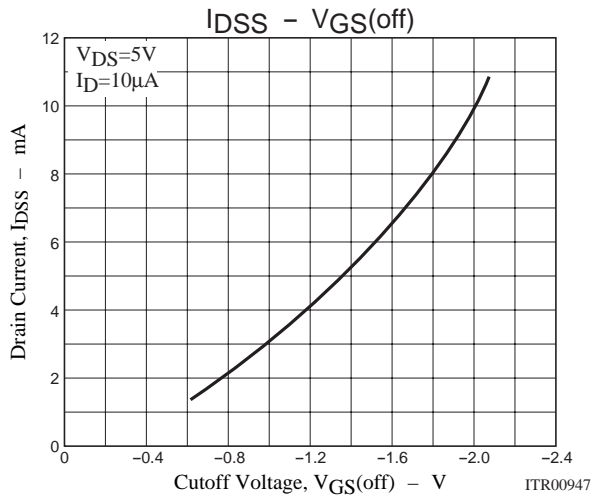
## PG and NF Test Circuit



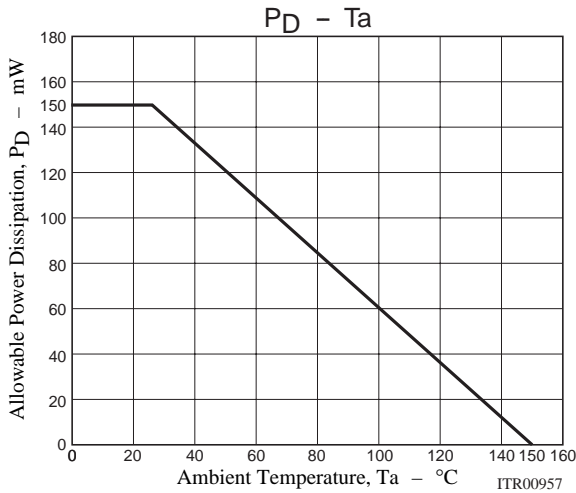
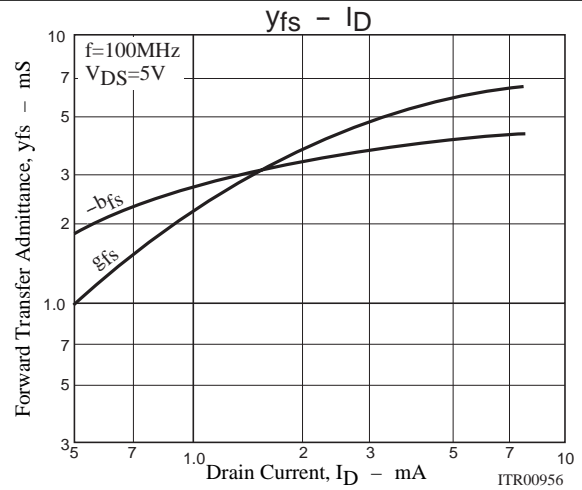
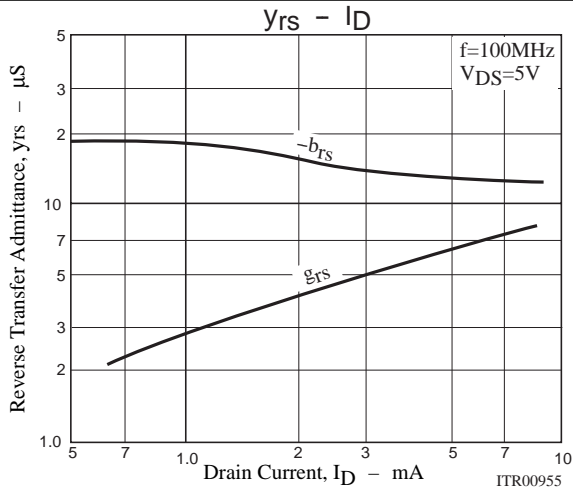
- L1 : 1mm  $\phi$  plated wire, 10mm  $\phi$  4T 18mm pitch, tapped at 1T from gate side
- L2 : 1mm  $\phi$  plated wire, 10mm  $\phi$  6T 10mm pitch, tapped at 1T from gate side



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