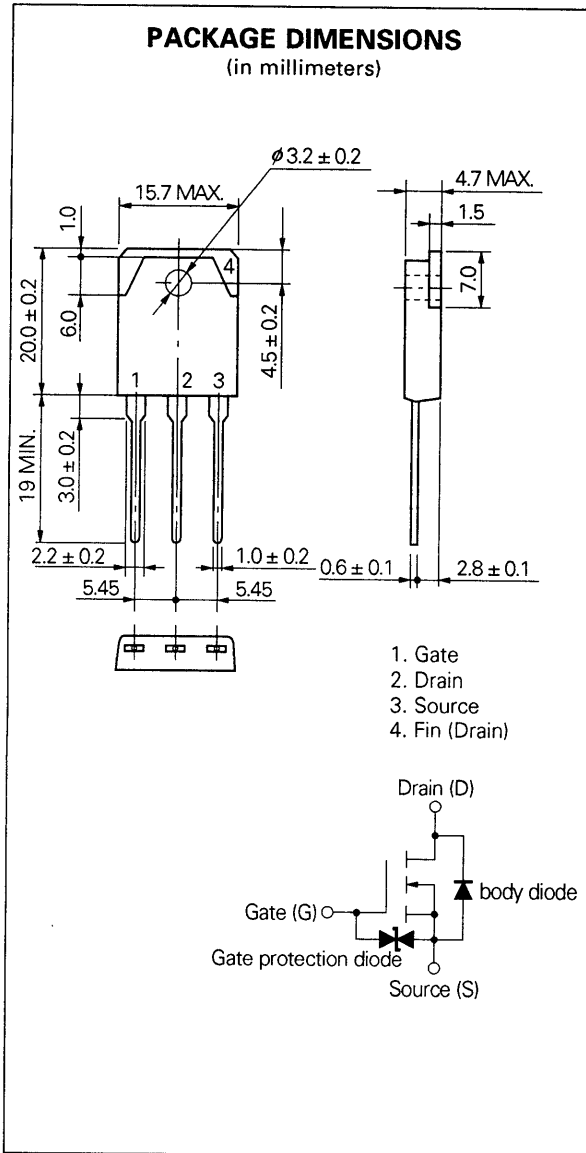


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P1 98.2

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE



DESCRIPTION

The 2SK1123 is N-channel MOS Field Effect Transistor designed for solenoid, motor and lamp driver.

FEATURES

- Low On-state Resistance
 $R_{DS(on)} \leq 27 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 20 \text{ A)}$
 $R_{DS(on)} \leq 50 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4 \text{ V, } I_D = 20 \text{ A)}$
- Low C_{iss} $C_{iss} = 3250 \text{ pF TYP.}$
- Built-in G-S Gate Protection Diodes

QUALITY GRADE

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature	-55 to +150	°C
Channel Temperature	150	°C MAX.

Maximum Power Dissipation

Total Power Dissipation ($T_c = 25 \text{ }^\circ\text{C}$)	100	W
Total Power Dissipation ($T_a = 25 \text{ }^\circ\text{C}$)	3.0	W

Maximum Voltages and Currents ($T_a = 25 \text{ }^\circ\text{C}$)

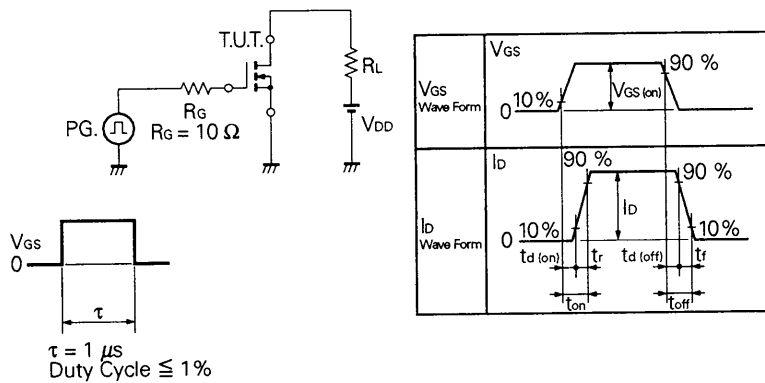
V_{DSS}	Drain to Source Voltage	60	V
$V_{GSS(AC)}$	Gate to Source Voltage	± 20	V
$I_{D(DC)}$	Drain Current (DC)	± 40	A
$I_{D(pulse)*}$	Drain Current (pulse)	± 160	A

* $PW \leq 10 \text{ } \mu\text{s}$, Duty Cycle $\leq 1 \%$

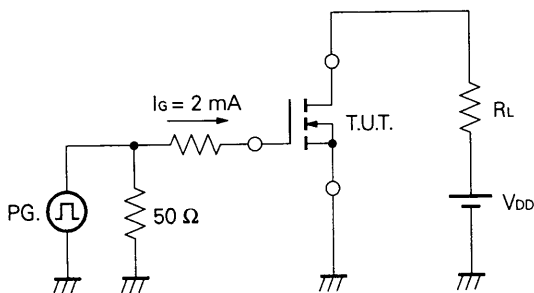
ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	R _{DS(on)}		22	70	mΩ	V _{GS} = 10 V, I _D = 20 A
Drain to Source On-state Resistance	R _{DS(on)}		30	95	mΩ	V _{GS} = 4.0 V, I _D = 20 A
Gate to Source Cutoff Voltage	V _{GS(off)}	1.0		2.5	V	V _{DS} = 10 V, I _D = 1 mA
Forward Transfer Admittance	y _{fs}	7.0			S	V _{DS} = 10 V, I _D = 20 A
Drain Leakage Current	I _{DSS}			10	μA	V _{DS} = 60 V, V _{GS} = 0
Gate to Source Leakage Current	I _{GSS}			±10	μA	V _{GS} = ±20 V, V _{DS} = 0
Input Capacitance	C _{iss}		3 250		pF	V _{DS} = 10 V V _{GS} = 0 f = 1 MHz
Output Capacitance	C _{oss}		1 200		pF	
Reverse Transfer Capacitance	C _{rss}		380		pF	
Turn-On Delay Time	t _{d(on)}		60		ns	V _{GS(on)} = 10 V V _{DD} = 30 V I _D = 20 A, R _G = 10 Ω R _L = 1.5 Ω
Rise Time	t _r		500		ns	
Turn-Off Delay Time	t _{d(off)}		250		ns	
Fall Time	t _f		160		ns	
Total Gate Charge	Q _G		85		nC	V _{GS} = 10 V I _D = 40 A V _{DD} = 48 V
Gate to Source Charge	Q _{GS}		10		nC	
Gate to Drain Charge	Q _{GD}		35		nC	
Diode Forward Voltage	V _{SD}		1.2		V	I _{SD} = 40 A, V _{GS} = 0
Reverse Recovery Time	t _{rr}		130		ns	I _F = 40 A, V _{GS} = 0
Reverse Recovery Charge	Q _{rr}		200		nC	di/dt = 50 A/μs

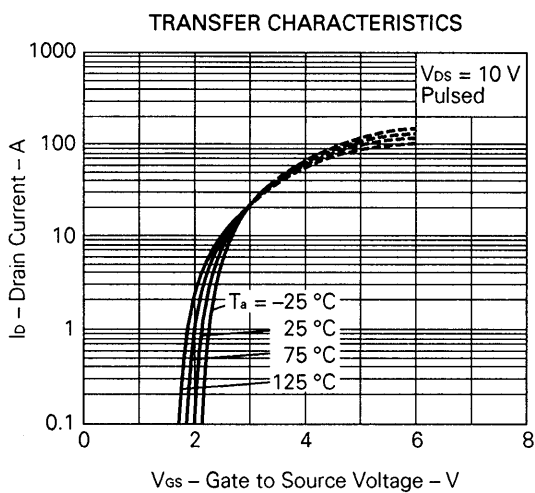
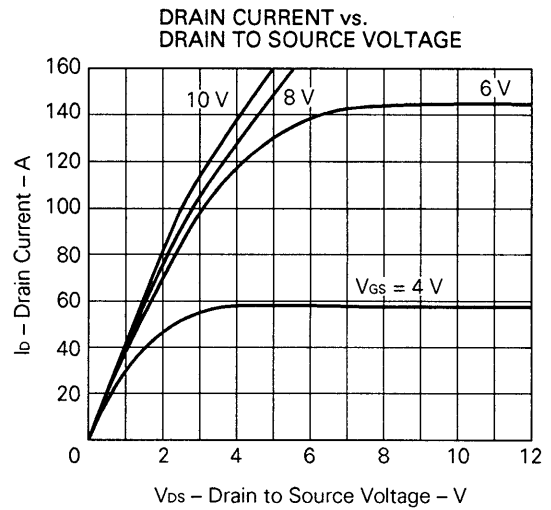
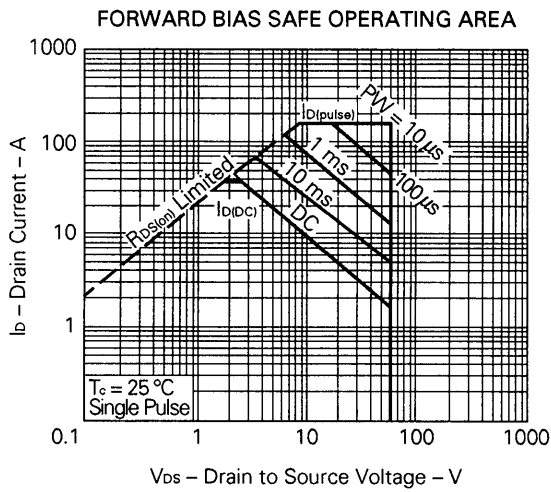
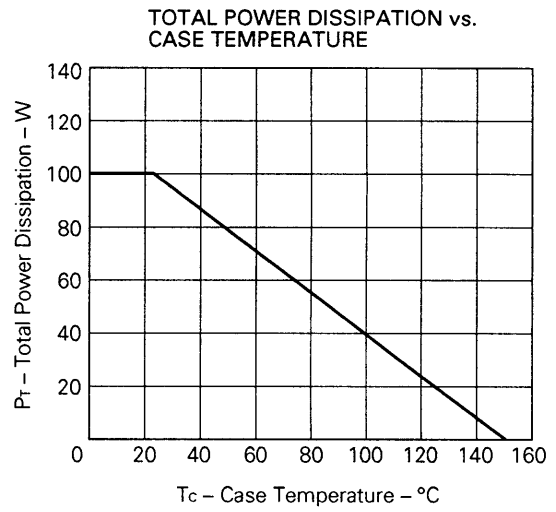
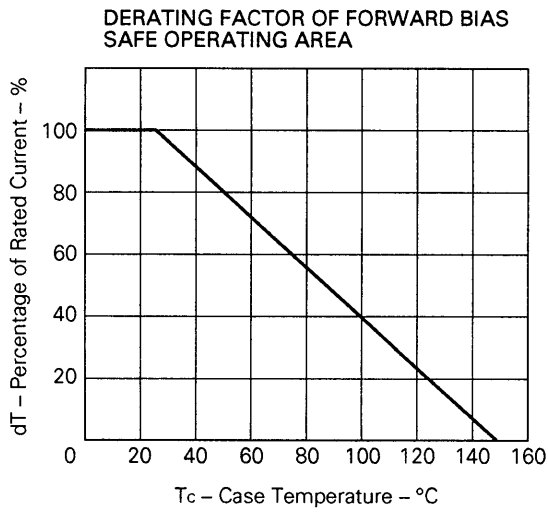
Test Circuit 1: Switching Time

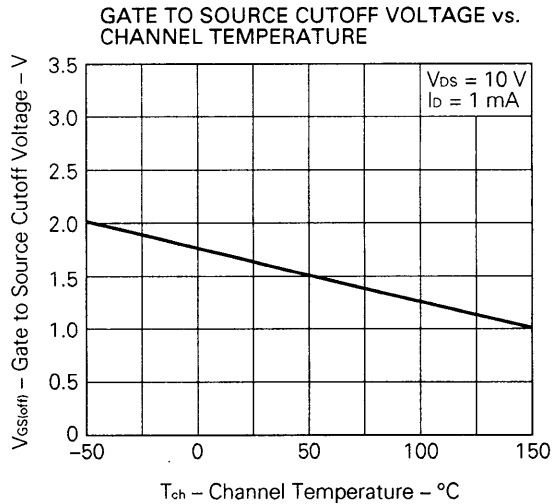
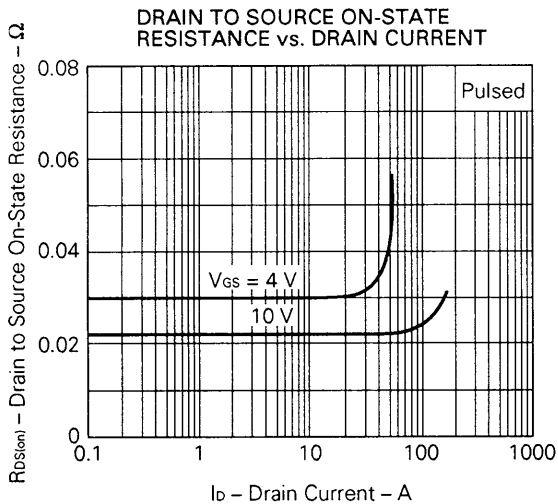
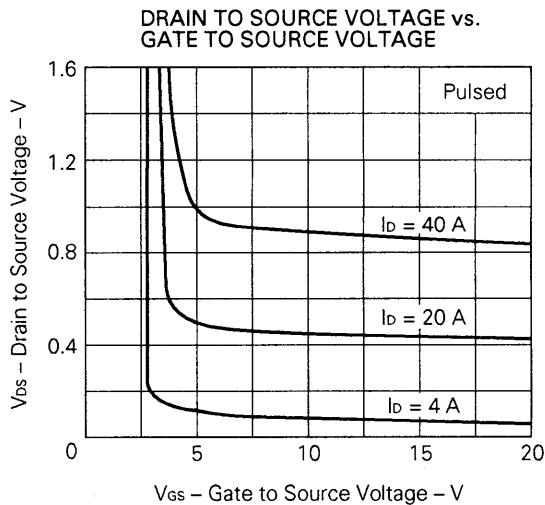
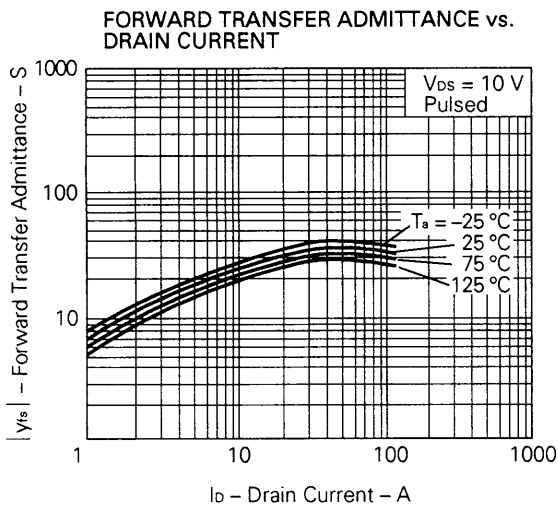
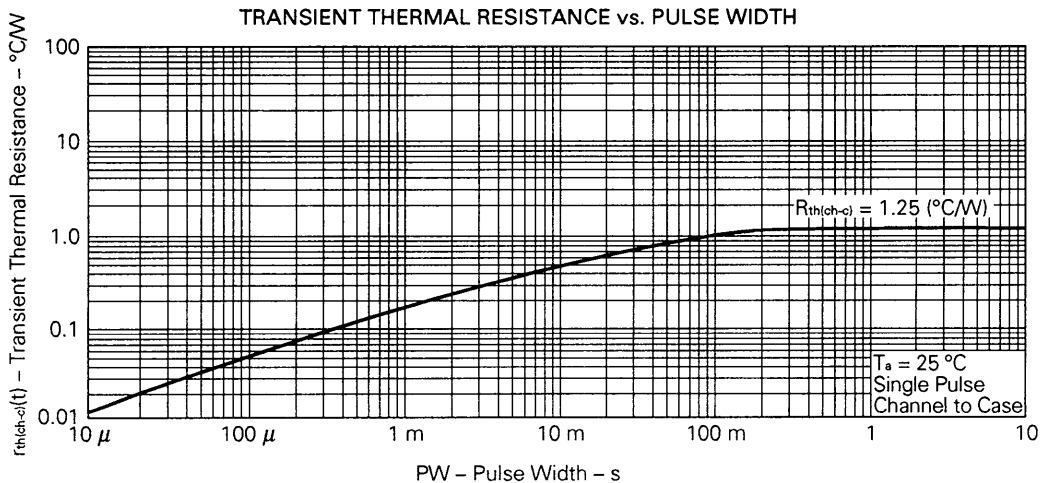


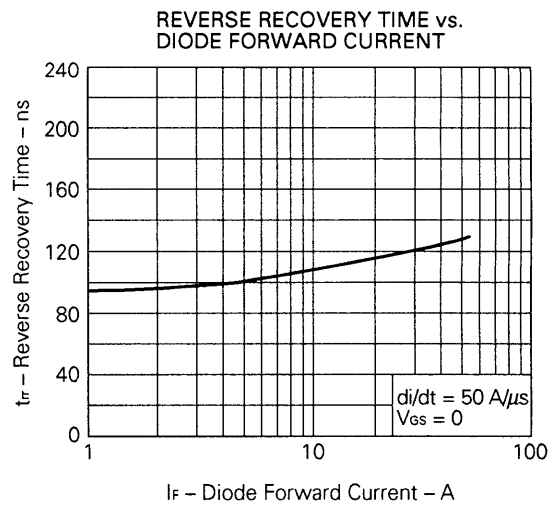
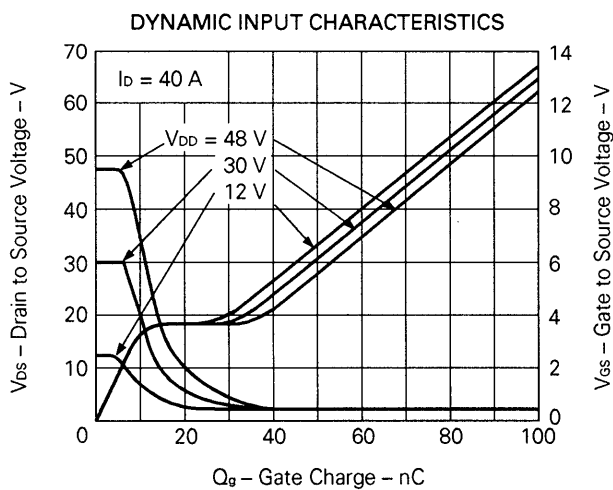
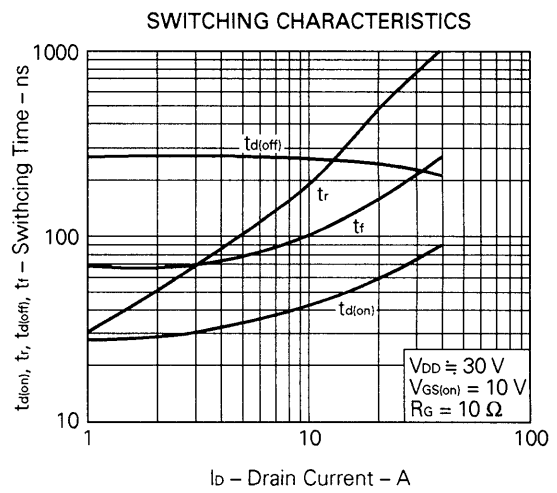
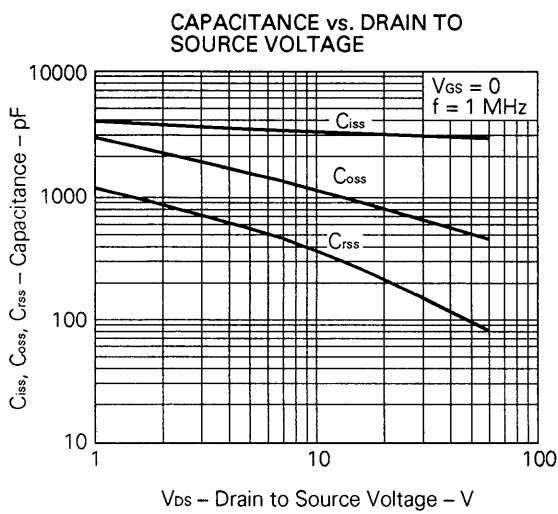
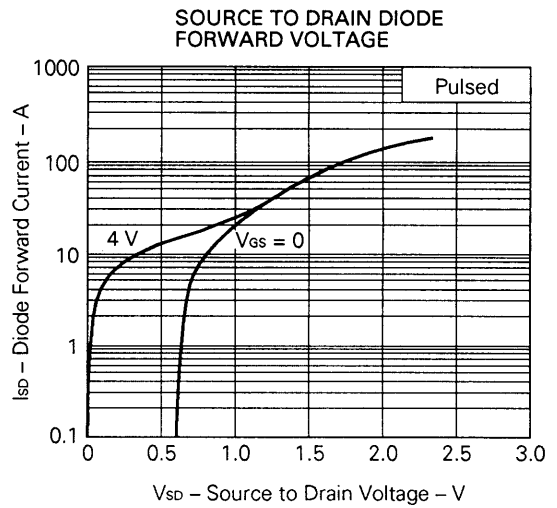
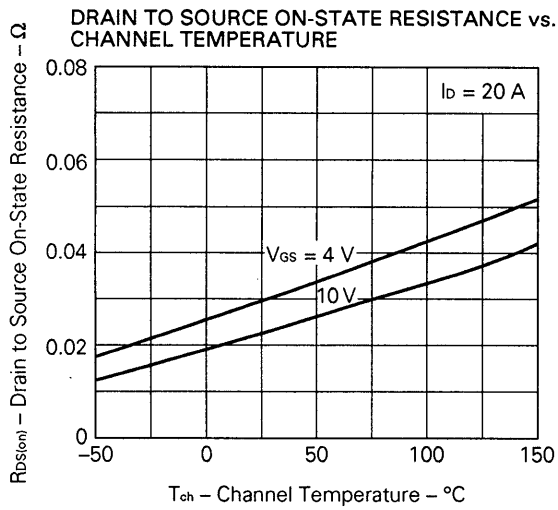
Test Circuit 2: Gate Charge



TYPICAL CHARACTERISTICS (T_a = 25 °C)







Reference

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207

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