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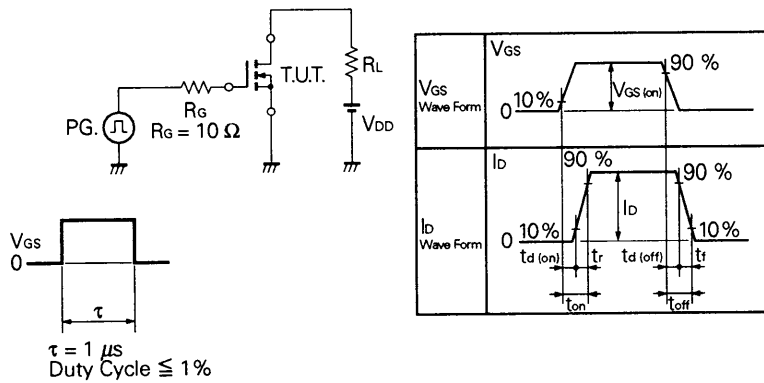
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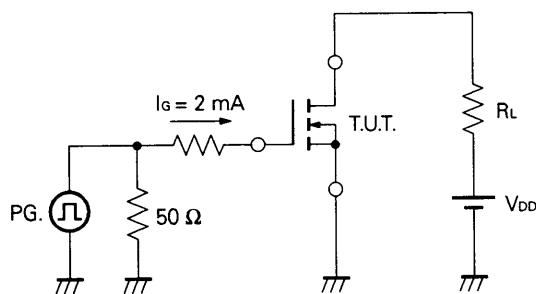
**ELECTRICAL CHARACTERISTICS (T<sub>a</sub> = 25 °C)**

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	R <sub>DS(on)</sub>		0.12	0.15	Ω	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 8 A
Drain to Source On-state Resistance	R <sub>DS(on)</sub>		0.15	0.2	Ω	V <sub>GS</sub> = 4.0 V, I <sub>D</sub> = 8 A
Gate to Source Cutoff Voltage	V <sub>GS(off)</sub>	1.0		2.5	V	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA
Forward Transfer Admittance	y <sub>fs</sub>	7.0	14		S	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 8 A
Drain Leakage Current	I <sub>DSS</sub>			10	μA	V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0
Gate to Source Leakage Current	I <sub>GSS</sub>			±10	μA	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0
Input Capacitance	C <sub>iss</sub>		1 400		pF	V <sub>DS</sub> = 10 V V <sub>GS</sub> = 0 f = 1 MHz
Output Capacitance	C <sub>oss</sub>		350		pF	
Reverse Transfer Capacitance	C <sub>rss</sub>		50		pF	
Turn-On Delay Time	t <sub>d(on)</sub>		25		ns	V <sub>GS(on)</sub> = 10 V V <sub>DD</sub> = 50 V I <sub>D</sub> = 10 A, R <sub>G</sub> = 10 Ω R <sub>L</sub> = 5.0 Ω
Rise Time	t <sub>r</sub>		110		ns	
Turn-Off Delay Time	t <sub>d(off)</sub>		100		ns	
Fall Time	t <sub>f</sub>		65		ns	
Total Gate Charge	Q <sub>G</sub>		30		nC	V <sub>GS</sub> = 10 V I <sub>D</sub> = 20 A V <sub>DD</sub> = 80 V
Gate to Source Charge	Q <sub>GS</sub>		5		nC	
Gate to Drain Charge	Q <sub>GD</sub>		10		nC	
Diode Forward Voltage	V <sub>SD</sub>		1.1		V	I <sub>SD</sub> = 15 A, V <sub>GS</sub> = 0
Reverse Recovery Time	t <sub>rr</sub>		200		ns	I <sub>F</sub> = 20 A, V <sub>GS</sub> = 0 di/dt = 50 A/μs
Reverse Recovery Charge	Q <sub>rr</sub>		500		nC	

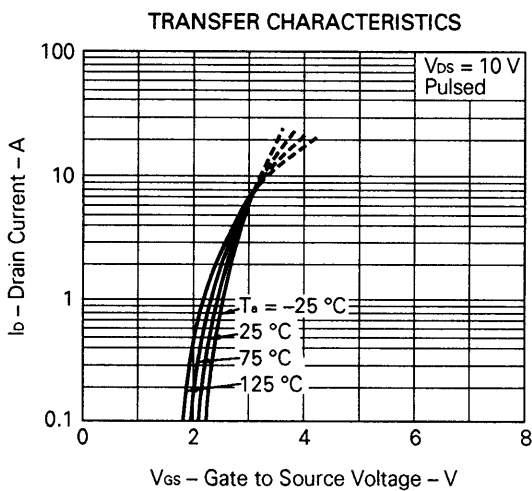
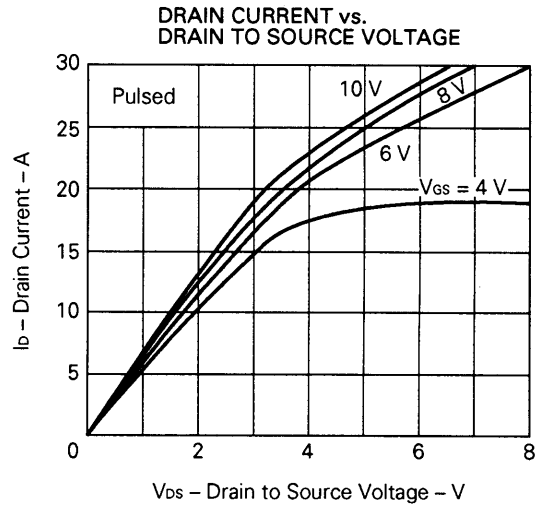
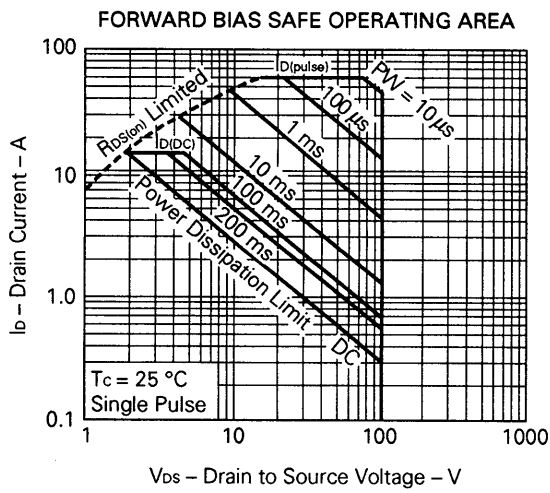
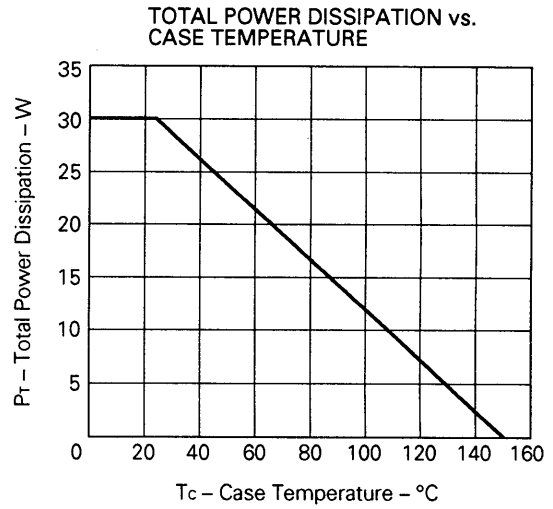
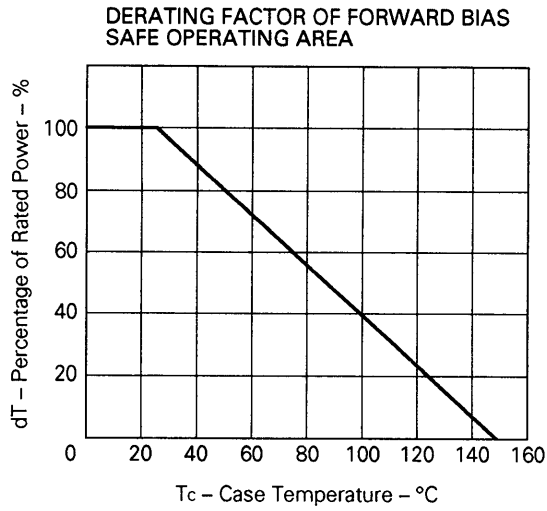
**Test Circuit 1: Switching Time**



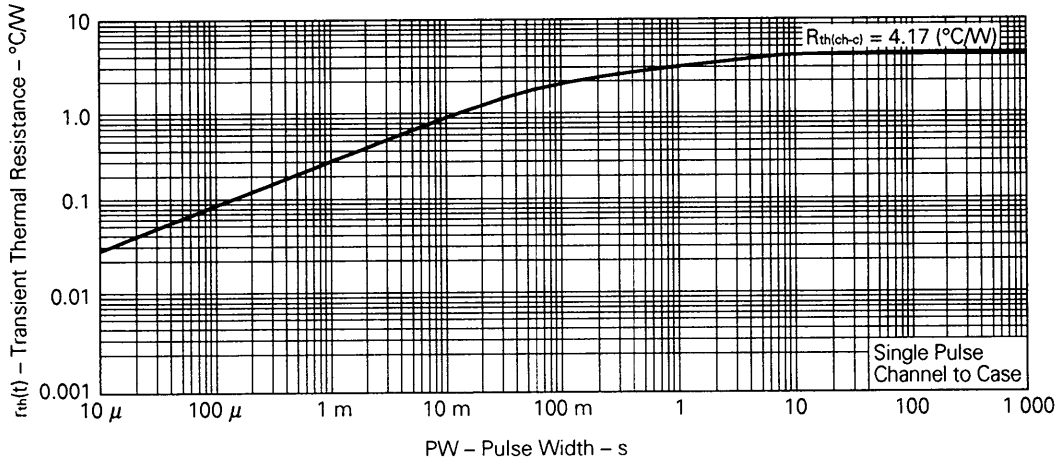
**Test Circuit 2: Gate Charge**



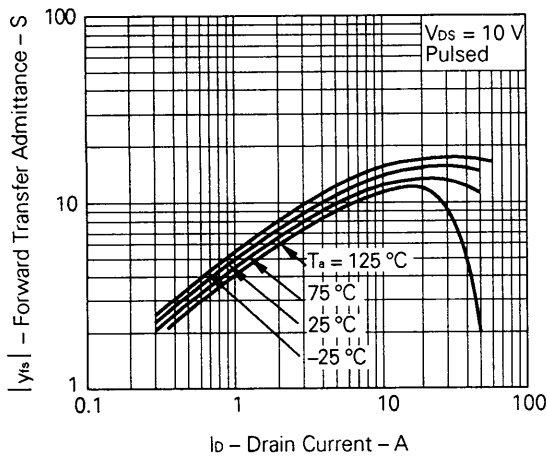
TYPICAL CHARACTERISTICS (T<sub>a</sub> = 25 °C)



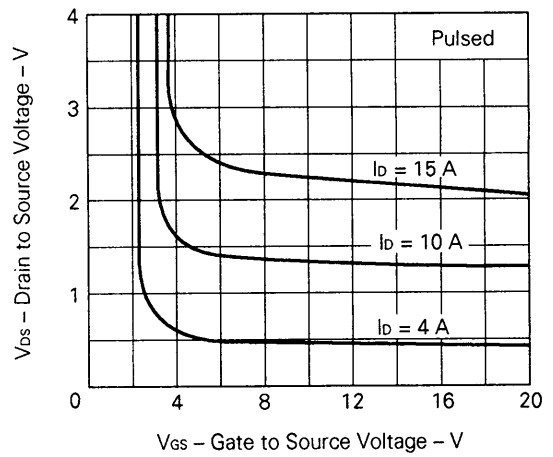
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



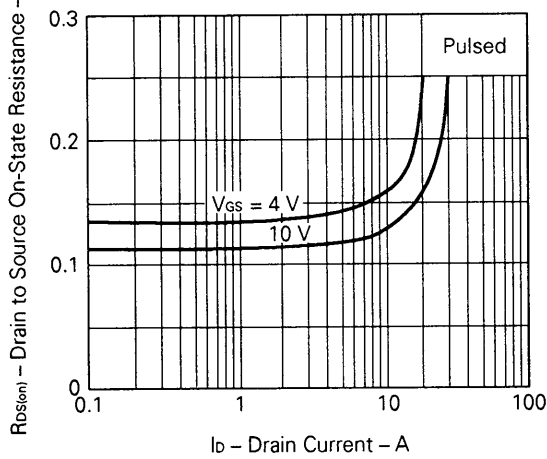
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



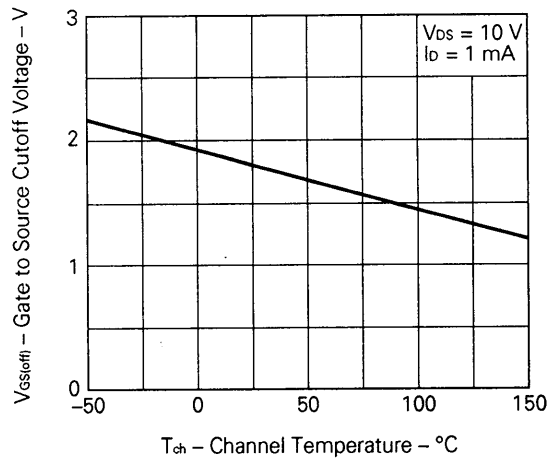
DRAIN TO SOURCE VOLTAGE vs. GATE TO SOURCE VOLTAGE



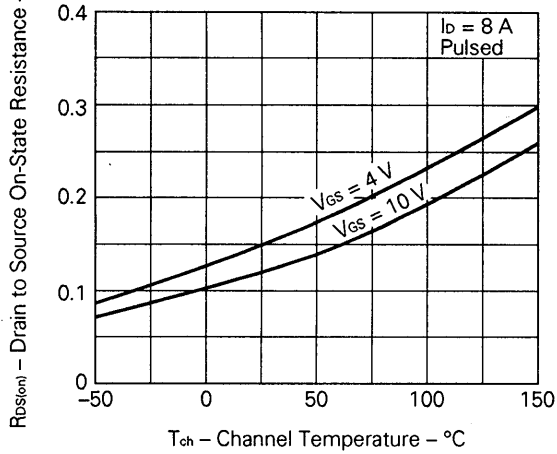
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



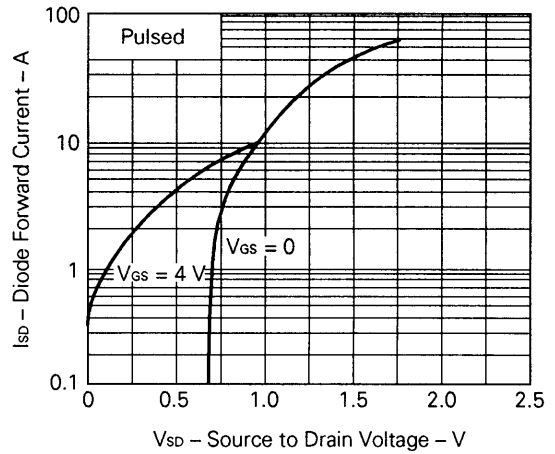
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE



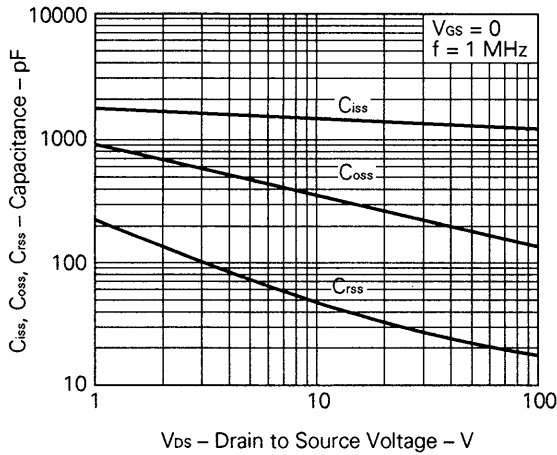
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



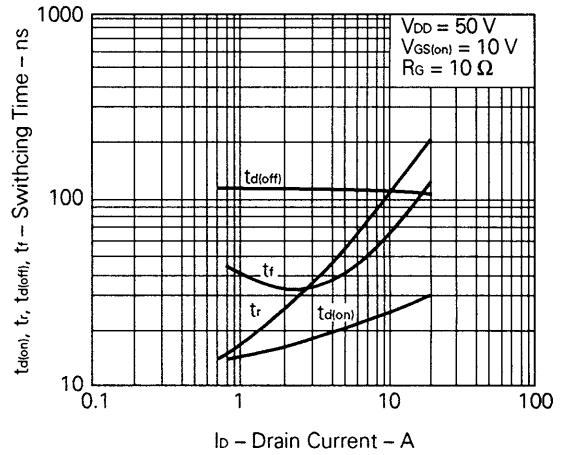
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



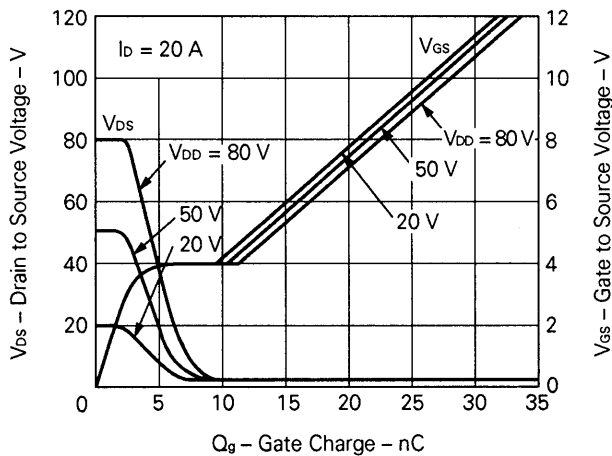
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



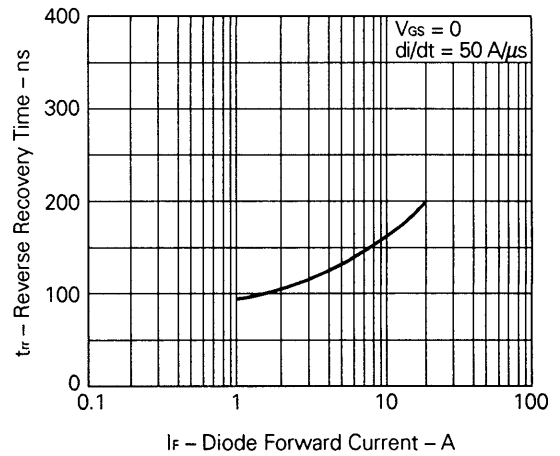
SWITCHING CHARACTERISTICS



DYNAMIC INPUT CHARACTERISTICS



REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



**Reference**

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207

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