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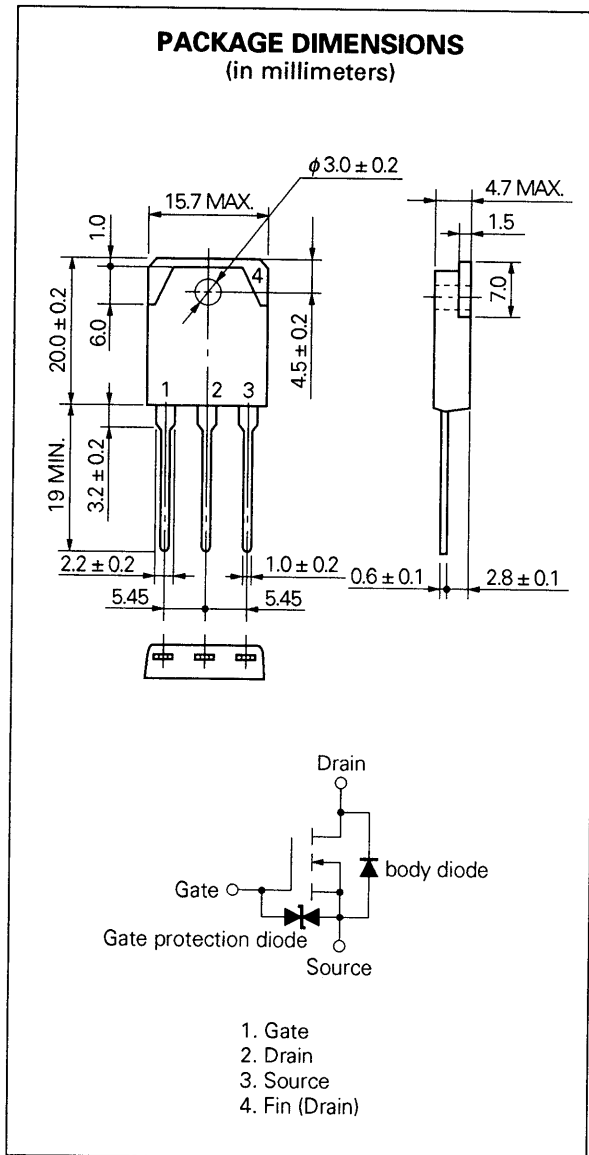
N-CHANNEL MOS FIELD EFFECT POWER TRANSISTOR

2SK1492

SWITCHING

N-CHANNEL POWER MOS FET

INDUSTRIAL USE



DESCRIPTION

The 2SK1492 is N-channel MOS Field Effect Transistor designed for high voltage switching applications.

FEATURES

- Low On-state Resistance
 $R_{DS(on)} = 0.12 \Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 18 \text{ A)}$
- Low C_{iss} $C_{iss} = 3\ 000 \text{ pF TYP.}$
- Built-in G-S Gate Protection Diodes
- High Avalanche Capability Ratings

QUALITY GRADE

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature	-55 to +150 °C
Channel Temperature	150 MAX. °C

Maximum Power Dissipation

Total Power Dissipation ($T_a = 25 \text{ °C}$)	140	W
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Maximum Voltages and Currents ($T_a = 25 \text{ °C}$)

V_{DSS}	Drain to Source Voltage	250	V
V_{GSS}	Gate to Source Voltage	±30	V
$I_{D(DC)}$	Drain Current (DC)	±35	A
$I_{D(pulse)*}$	Drain Current (pulse)	±140	A

* $PW \leq 10 \mu s$, Duty Cycle $\leq 1 \%$

Maximum Avalanche Capability Ratings**

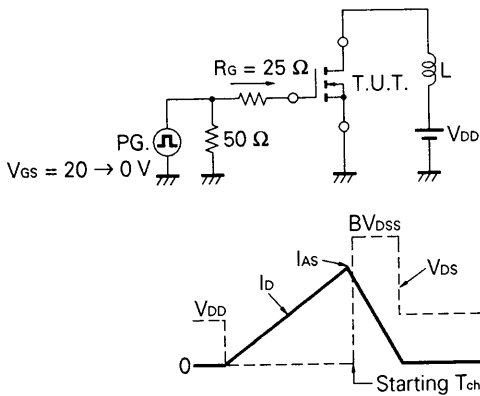
I_{AS}	Single Avalanche Current	52.5	A
E_{AS}	Single Avalanche Energy	2 500	mJ

**Starting $T_{ch} = 25 \text{ °C}$, $R_G = 25 \Omega$, $V_{GS} = 20 \text{ V} \rightarrow 0$

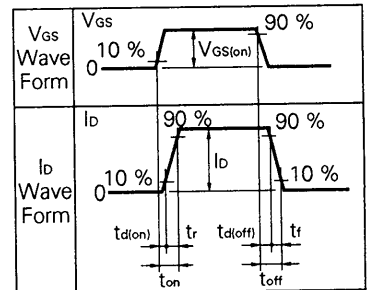
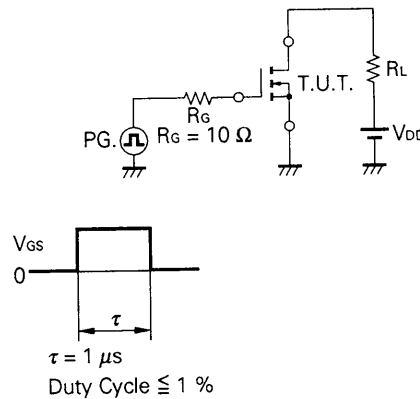
ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	R _{DS(on)}		0.08	0.12	Ω	V _{GS} = 10 V, I _D = 18 A
Gate to Source Cutoff Voltage	V _{GS(off)}	2.5		3.5	V	V _{DS} = 10 V, I _D = 1 mA
Forward Transfer Admittance	y _{fs}	7.0			S	V _{DS} = 10 V, I _D = 18 A
Drain Leakage Current	I _{DSS}			100	μA	V _{DS} = 250 V, V _{GS} = 0
Gate to Source Leakage Current	I _{GSS}			±10	μA	V _{GS} = ±30 V, V _{DS} = 0
Input Capacitance	C _{iss}		3 000		pF	V _{DS} = 10 V
Output Capacitance	C _{oss}		1 500		pF	V _{GS} = 0
Reverse Transfer Capacitance	C _{rss}		620		pF	f = 1 MHz
Turn-On Delay Time	t _{d(on)}		50		ns	V _{GS} = 10 V
Rise Time	t _r		240		ns	V _{DD} = 150 V
Turn-Off Delay Time	t _{d(off)}		140		ns	I _D = 18 A, R _G = 10 Ω
Fall Time	t _f		100		ns	R _L = 8.3 Ω
Total Gate Charge	Q _G		80		nC	V _{GS} = 10 V
Gate to Source Charge	Q _{GS}		17		nC	I _D = 35 A
Gate to Drain Charge	Q _{GD}		50		nC	V _{DD} = 200 V
Diode Forward Voltage	V _{F(S-D)}		1.0		V	I _F = 35 A, V _{GS} = 0
Reverse Recovery Time	t _{rr}		370		ns	I _F = 35 A
Reverse Recovery Charge	Q _{rr}		2.8		μC	di/dt = 50 A/μs

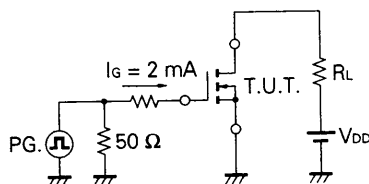
Test Circuit 1: Avalanche Time



Test Circuit 2: Switching Time

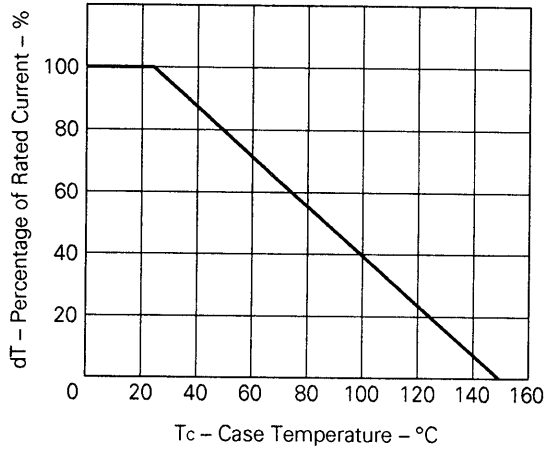


Test Circuit 3: Gate Charge

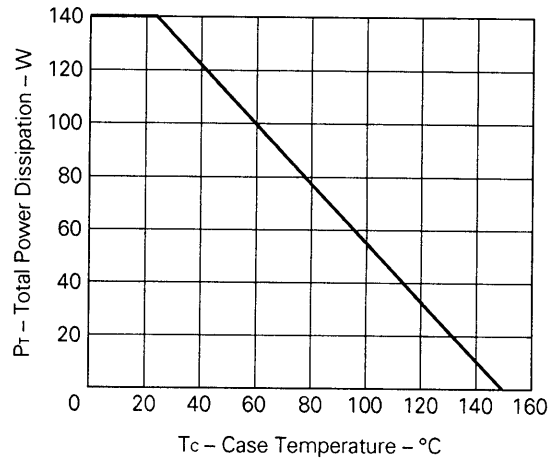


TYPICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$)

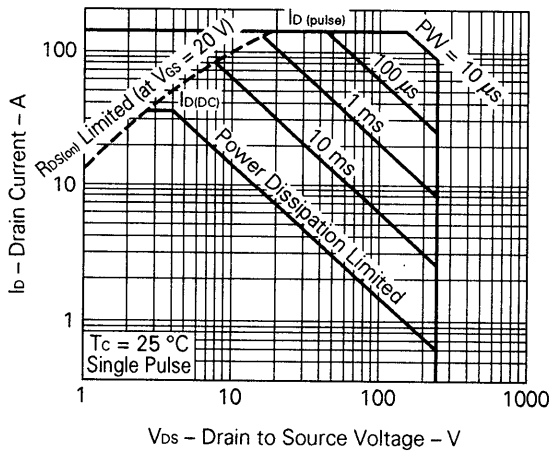
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



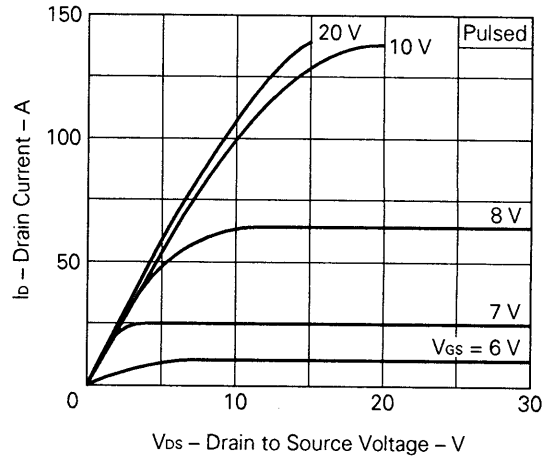
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



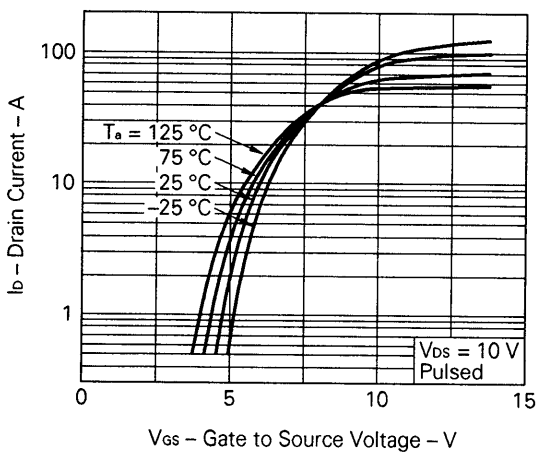
FORWARD BIAS SAFE OPERATING AREA



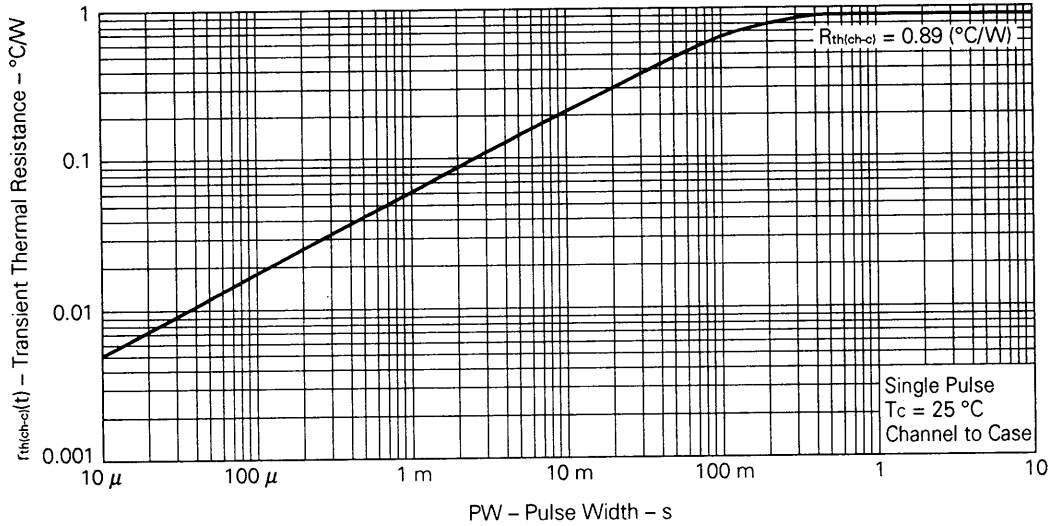
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



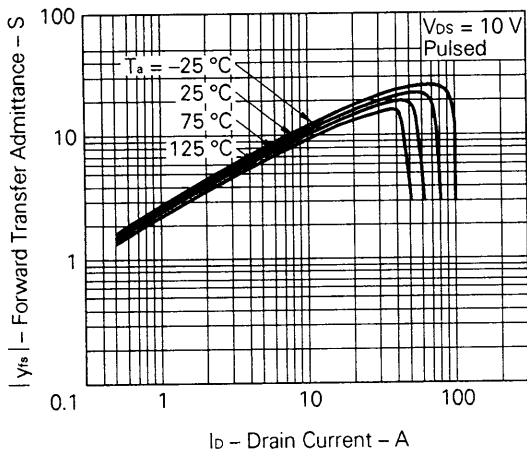
TRANSFER CHARACTERISTICS



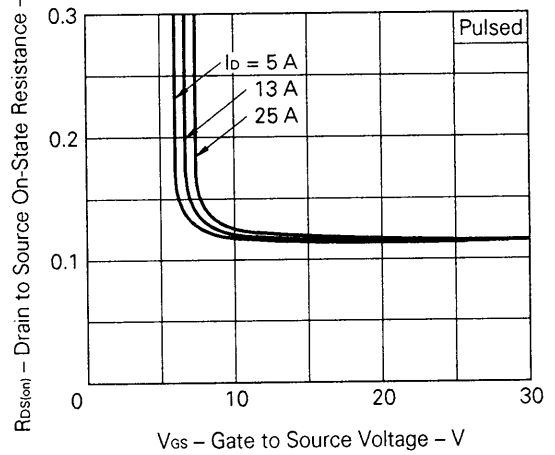
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



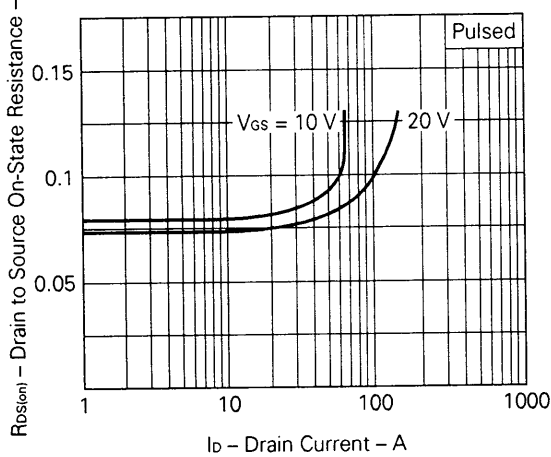
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



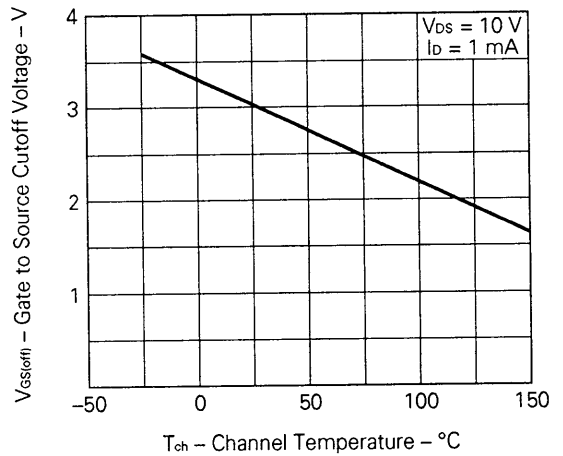
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

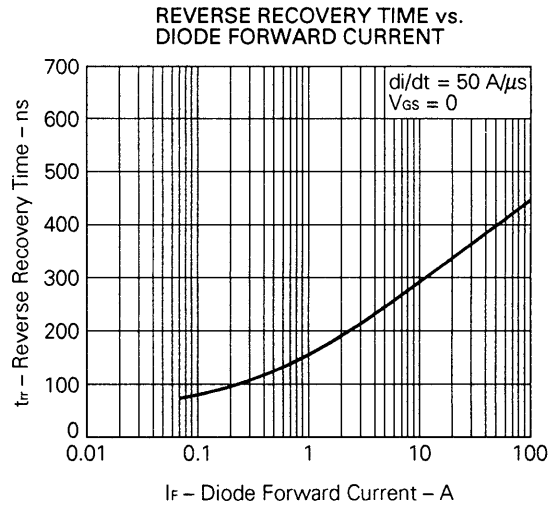
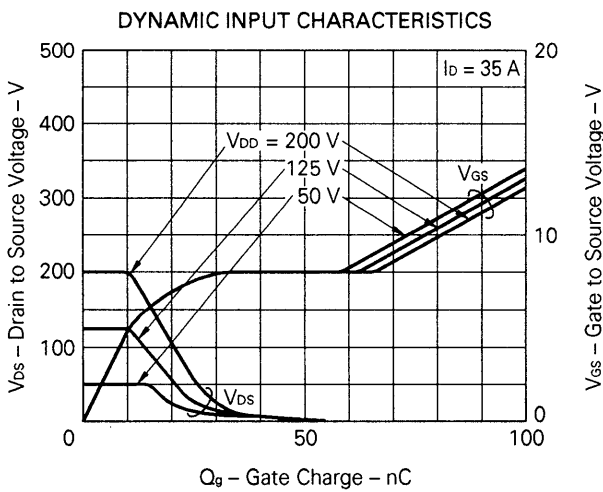
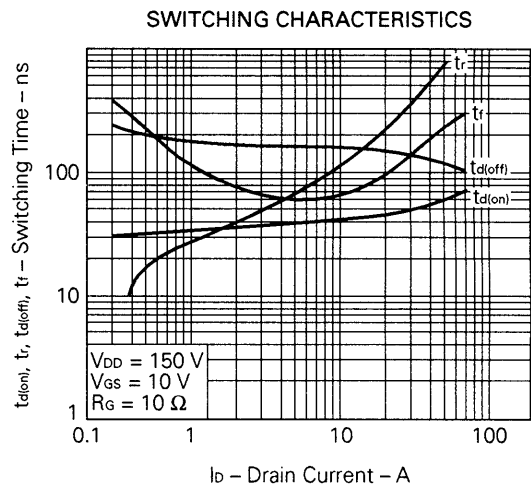
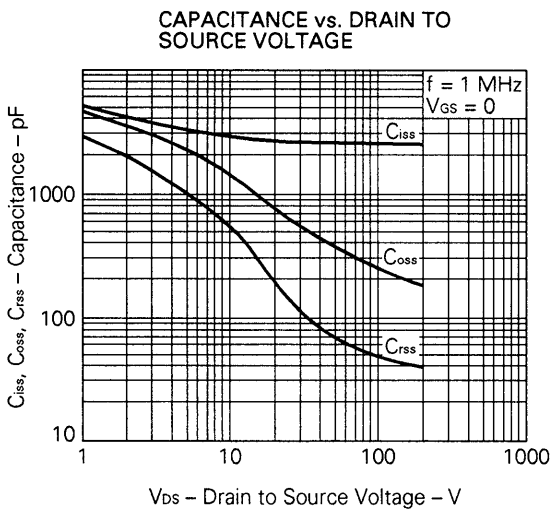
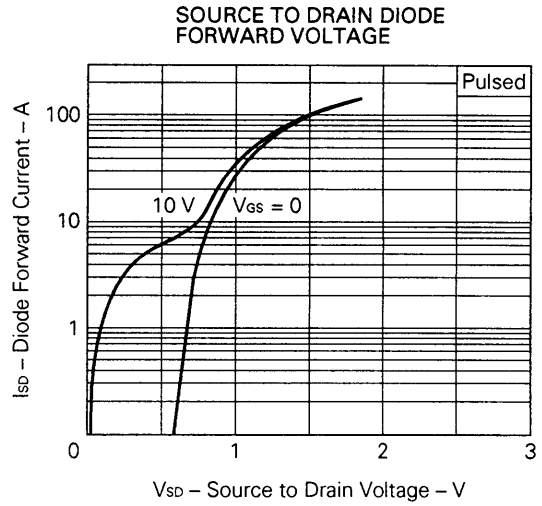
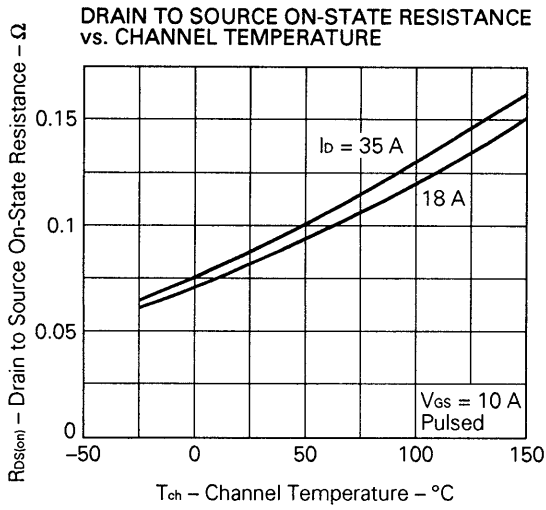


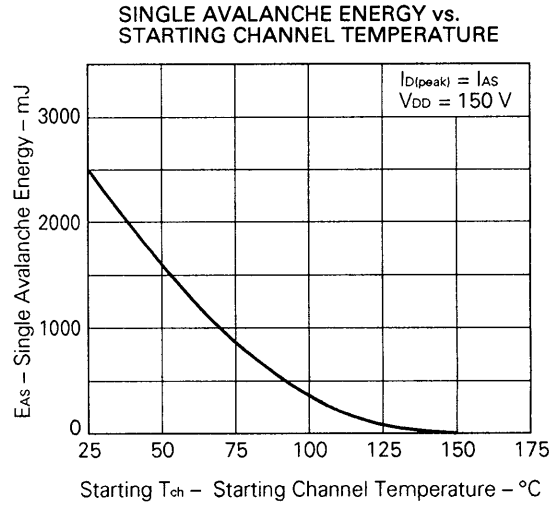
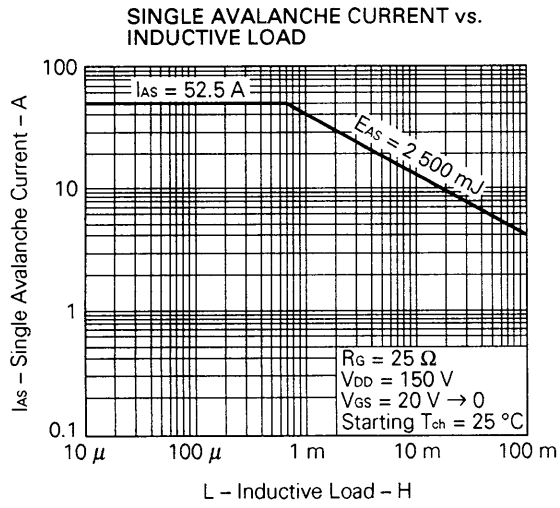
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE







Reference

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207

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