

Notice: You cannot copy or search for text in this PDF file, because this PDF file is converted from the scanned image of printed materials.

P1 98.2

MOS FIELD EFFECT POWER TRANSISTOR  
**2SK1497/2SK1498**

**SWITCHING**  
**N-CHANNEL POWER MOS FET**  
**INDUSTRIAL USE**

**DESCRIPTION**

The 2SK1497/2SK1498 is N-channel MOS Field Effect Transistor designed for high voltage switching applications.

**FEATURES**

- Low On-state Resistance  
 $R_{DS(on)} \leq 0.35 \Omega / 0.40 \Omega$  ( $V_{GS} = 10 \text{ V}$ ,  $I_D = 10 \text{ A}$ )
- Low  $C_{iss}$   $C_{iss} = 2460 \text{ pF TYP.}$
- Built-in G-S Gate Protection Diode
- High Avalanche Capability Ratings

**QUALITY GRADE**

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

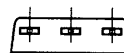
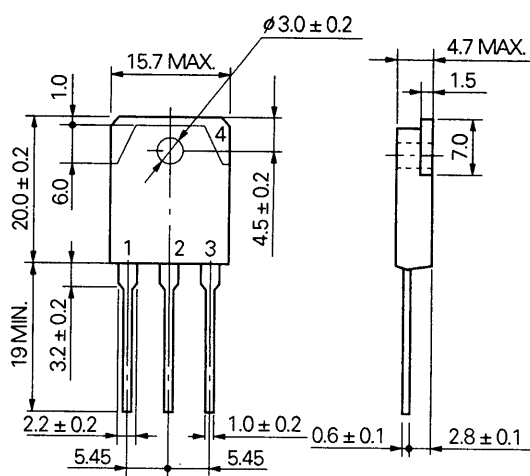
**ABSOLUTE MAXIMUM RATINGS ( $T_a = 25 \text{ }^\circ\text{C}$ )**

Drain to Source Voltage	$V_{DSS}$	450/500	V
(2SK1497/2SK1498)			
Gate to Source Voltage	$V_{GSS}$	$\pm 30$	V
Drain Current (DC)	$I_{D(DC)}$	$\pm 20$	A
Drain Current (pulse)	$I_{D(pulse)^*}$	$\pm 80$	A
Single Avalanche Current	$I_{AS}^{**}$	30	A
Single Avalanche Energy	$E_{AS}^{**}$	560	mJ
Total Power Dissipation ( $T_c = 25 \text{ }^\circ\text{C}$ )	$P_T$	120	W
Channel Temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$

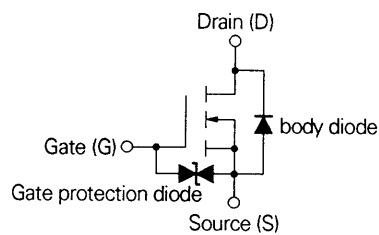
\*  $PW \leq 10 \mu\text{s}$ , Duty Cycle  $\leq 2 \%$

\*\* Starting  $T_{ch} = 25 \text{ }^\circ\text{C}$ ,  $R_G = 25 \Omega$ ,  $V_{GS} = 20 \text{ V} \rightarrow 0$

**PACKAGE DIMENSIONS**  
 (in millimeters)



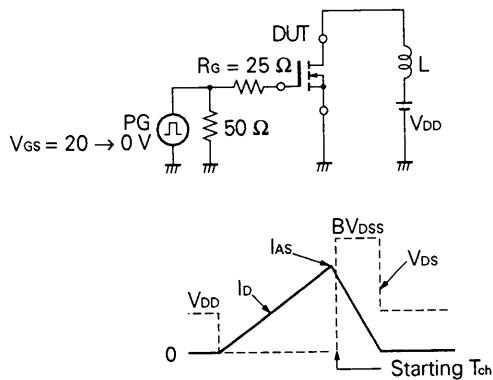
1. Gate
2. Drain
3. Source
4. Fin (Drain)



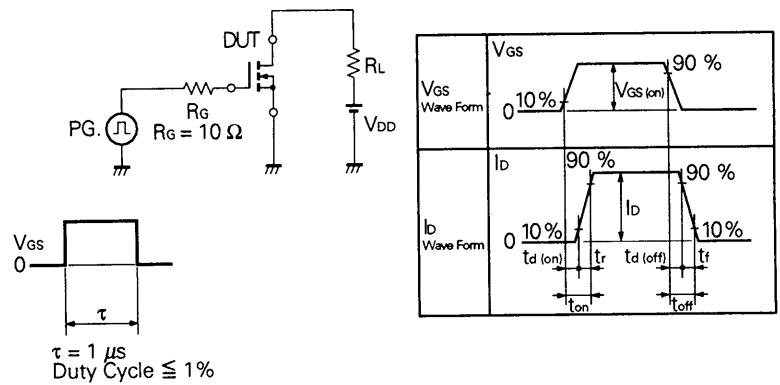
**ELECTRICAL CHARACTERISTICS (T<sub>a</sub> = 25 °C)**

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	2SK1497		0.28	0.35	Ω	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A
	2SK1498		0.32	0.40	Ω	
Gate to Source Cutoff Voltage	V <sub>GS(off)</sub>	2.5		3.5	V	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA
Forward Transfer Admittance	y <sub>fs</sub>	7.5			S	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 10 A
Drain Leakage Current (2SK1497)	I <sub>DSS</sub>			100	μA	V <sub>DS</sub> = 450 V, V <sub>GS</sub> = 0
Drain Leakage Current (2SK1498)	I <sub>DSS</sub>			100	μA	V <sub>DS</sub> = 500 V, V <sub>GS</sub> = 0
Gate to Source Leakage Current	I <sub>GSS</sub>			±10	μA	V <sub>GS</sub> = ±30 V, V <sub>DS</sub> = 0
Input Capacitance	C <sub>iss</sub>		2 460		pF	V <sub>DS</sub> = 10 V V <sub>GS</sub> = 0 f = 1 MHz
Output Capacitance	C <sub>oss</sub>		700		pF	
Reverse Transfer Capacitance	C <sub>rss</sub>		290		pF	
Turn-On Delay Time	t <sub>d(on)</sub>		30		ns	V <sub>GS</sub> = 10 V V <sub>DD</sub> = 150 V I <sub>D</sub> = 10 A, R <sub>G</sub> = 10 Ω R <sub>L</sub> = 15 Ω
Rise Time	t <sub>r</sub>		115		ns	
Turn-Off Delay Time	t <sub>d(off)</sub>		140		ns	
Fall Time	t <sub>f</sub>		50		ns	
Total Gate Charge	Q <sub>G</sub>		85		nC	
Gate to Source Charge	Q <sub>GS</sub>		15		nC	V <sub>GS</sub> = 10 V I <sub>D</sub> = 20 A V <sub>DD</sub> = 400 V
Gate to Drain Charge	Q <sub>GD</sub>		50		nC	
Diode Forward Voltage	V <sub>F(S-D)</sub>		1.0		V	
Reverse Recovery Time	t <sub>rr</sub>		630		ns	I <sub>F</sub> = 20 A, V <sub>GS</sub> = 0 di/dt = 50 A/μs
Reverse Recovery Charge	Q <sub>rr</sub>		6.0		μC	

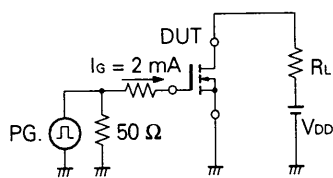
**Test Circuit 1: Avalanche Capability**



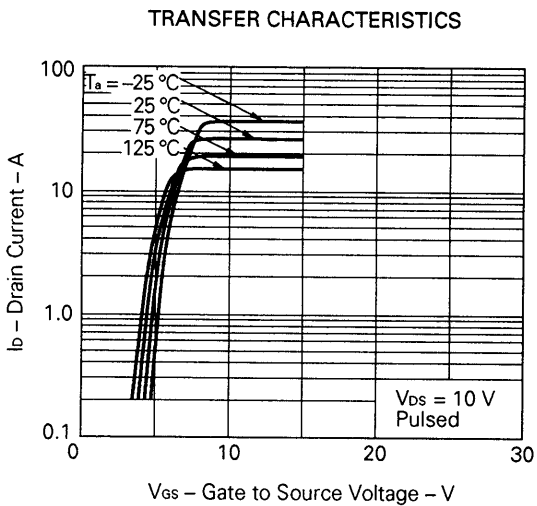
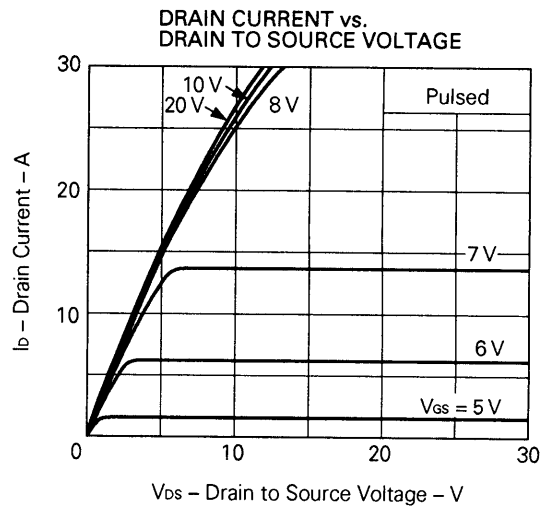
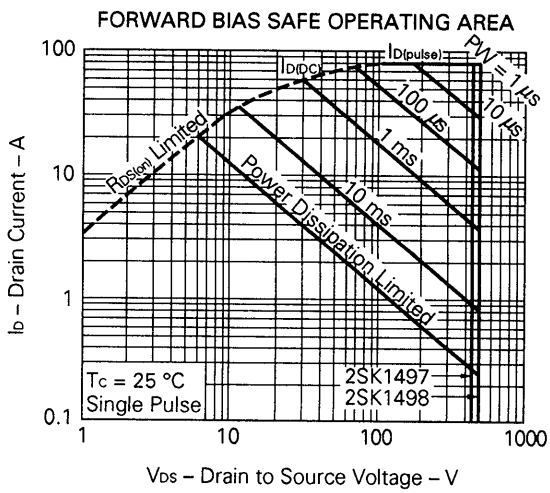
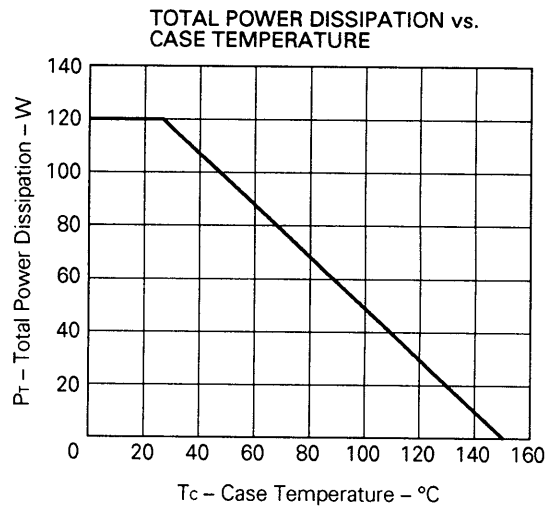
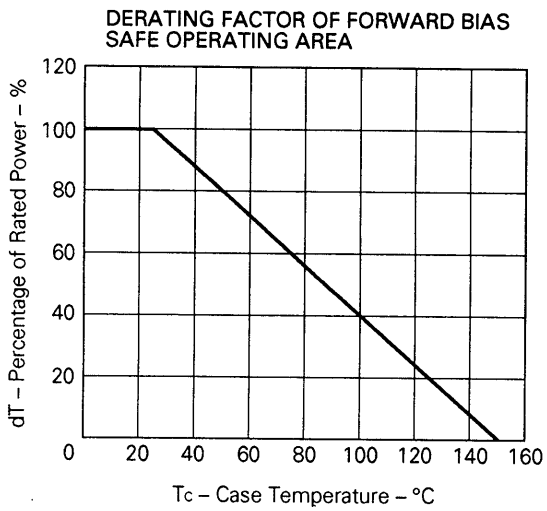
**Test Circuit 2: Switching Time**



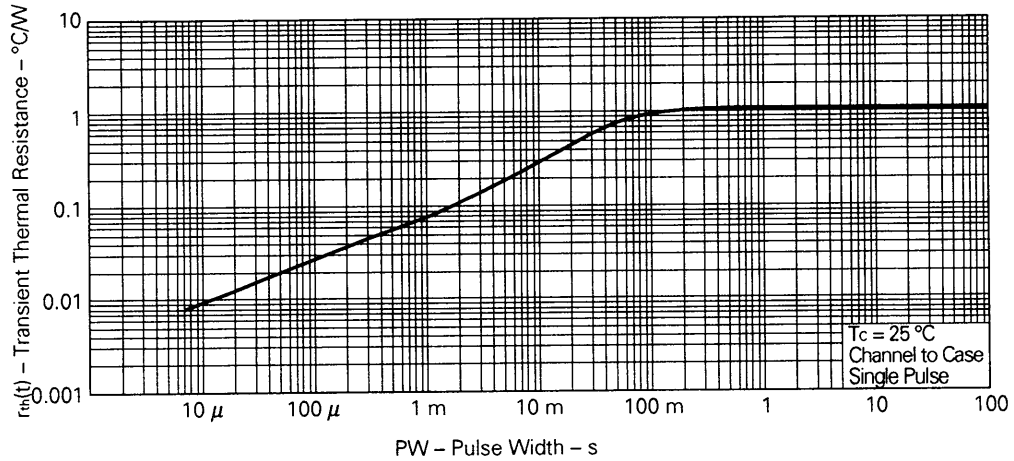
**Test Circuit 3: Gate Charge**



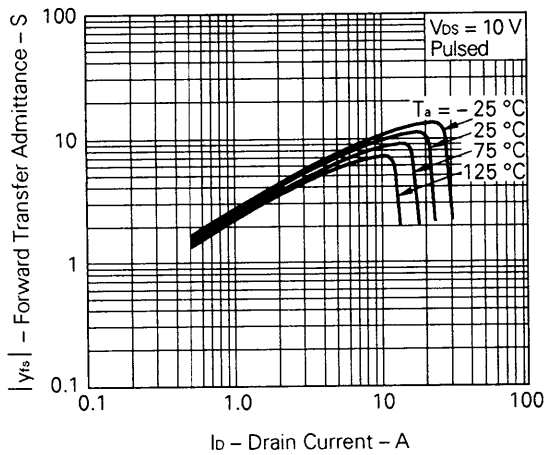
TYPICAL CHARACTERISTICS (T<sub>a</sub> = 25 °C)



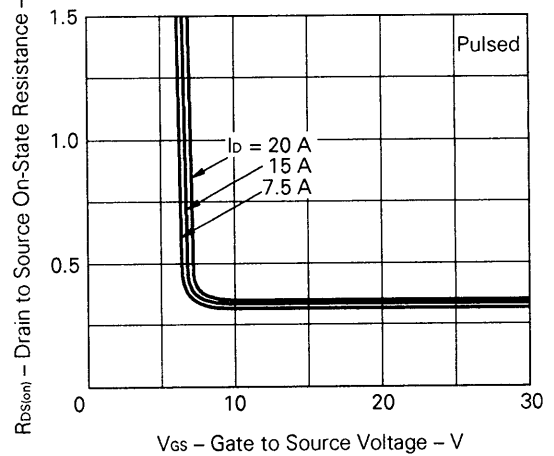
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



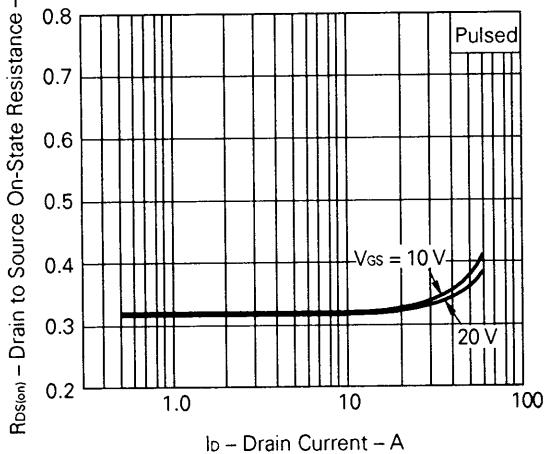
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



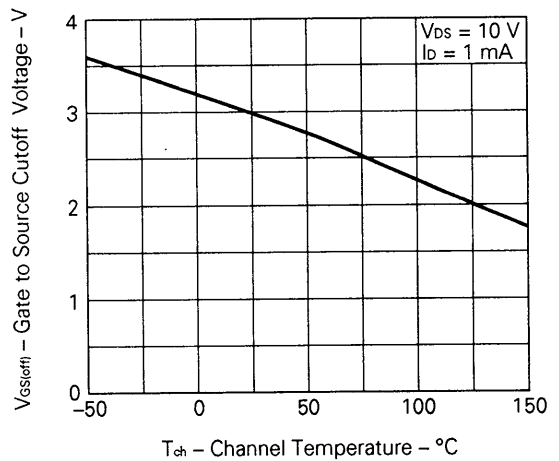
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

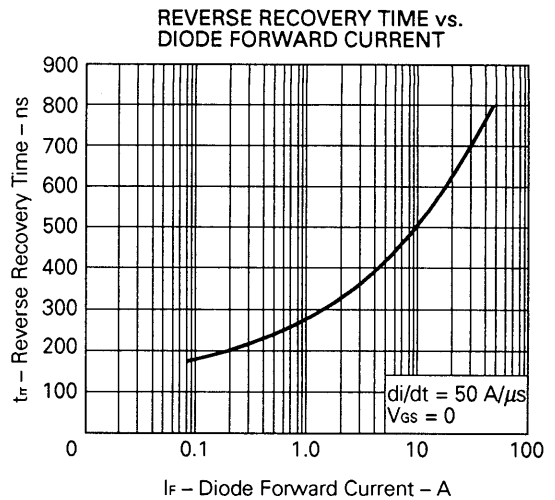
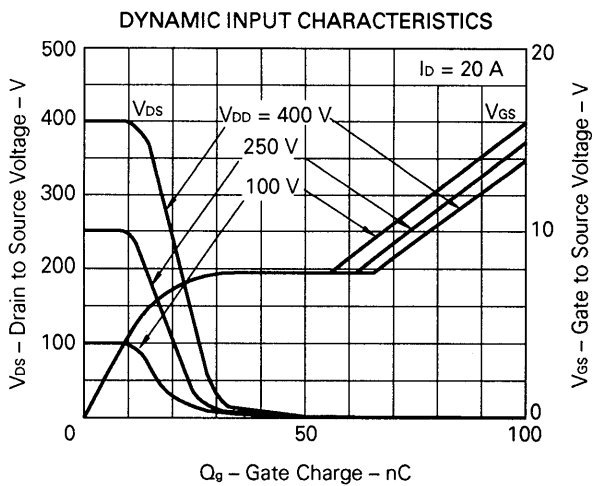
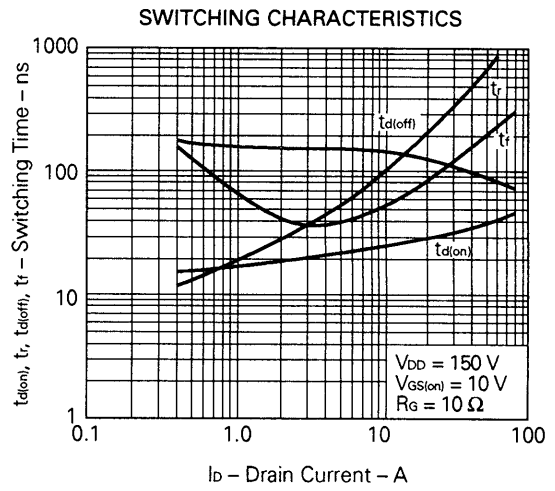
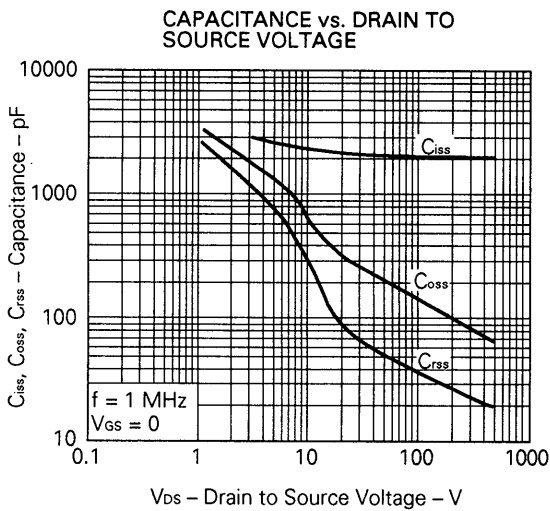
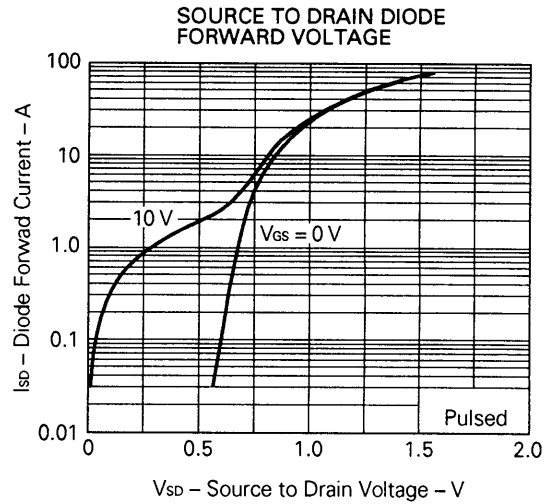
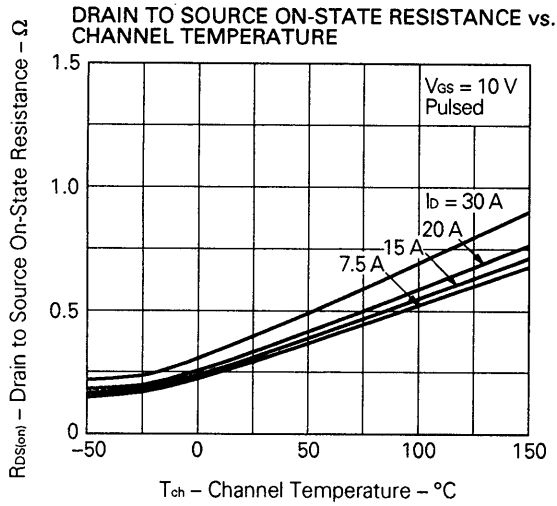


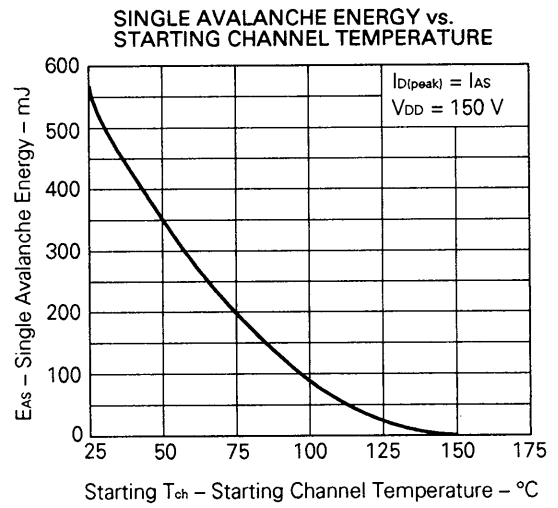
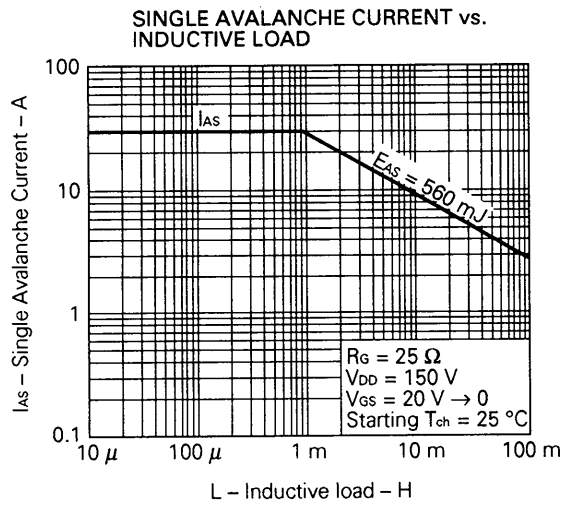
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE







**Reference**

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207



[MEMO]

No part of this document may be copied or reproduced in any form or by any means without the prior written consent of NEC Corporation. NEC Corporation assumes no responsibility for any errors which may appear in this document.

NEC Corporation does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from use of a device described herein or any other liability arising from use of such device. No license, either express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC Corporation or others.

The devices listed in this document are not suitable for use in aerospace equipment, submarine cables, nuclear reactor control systems and life support systems. If customers intend to use NEC devices for above applications or they intend to use "Standard" quality grade NEC devices for applications not intended by NEC, please contact our sales people in advance.

Application examples recommended by NEC Corporation.

Standard: Computer, Office equipment, Communication equipment, Test and Measurement equipment, Machine tools, Industrial robots, Audio and Visual equipment, Other consumer products, etc.

Special: Automotive and Transportation equipment, Traffic control systems, Antidisaster systems, Anticrime systems, etc.