

SWITCHING N-CANNEL POWER MOS FET

DESCRIPTION

The 2SK3430 is N-channel MOS Field Effect Transistor designed for high current switching applications.

FEATURES

- Super low on-state resistance:
 $R_{DS(on)1} = 7.3 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 40 \text{ A)}$
 $R_{DS(on)2} = 15 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4 \text{ V, } I_D = 40 \text{ A)}$
- Low C_{iss} : $C_{iss} = 2800 \text{ pF TYP.}$
- Built-in gate protection diode

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	40	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	± 20	V
Drain Current (DC) ($T_C = 25^\circ\text{C}$)	$I_{D(DC)}$	± 80	A
Drain Current (pulse) ^{Note1}	$I_{D(pulse)}$	± 200	A
Total Power Dissipation ($T_C = 25^\circ\text{C}$)	P_T	84	W
Total Power Dissipation ($T_A = 25^\circ\text{C}$)	P_T	1.5	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	$-55 \text{ to } +150$	$^\circ\text{C}$
Single Avalanche Current ^{Note2}	I_{AS}	37	A
Single Avalanche Energy ^{Note2}	E_{AS}	137	mJ

Notes 1. $PW \leq 10 \mu\text{s}$, Duty cycle $\leq 1\%$

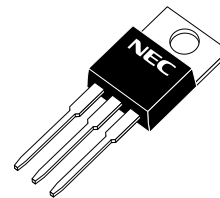
2. Starting $T_{ch} = 25^\circ\text{C}$, $V_{DD} = 20 \text{ V}$, $R_G = 25 \Omega$, $V_{GS} = 20 \rightarrow 0 \text{ V}$

ORDERING INFORMATION

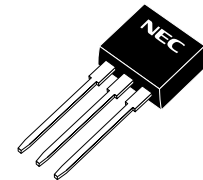
PART NUMBER	PACKAGE
2SK3430	TO-220AB
2SK3430-S	TO-262
2SK3430-ZJ	TO-263
2SK3430-Z	TO--220SMD ^{Note}

Note TO-220SMD package is produced only in Japan.

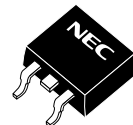
(TO-220AB)



(TO-262)



(TO-263 ,TO-220SMD)

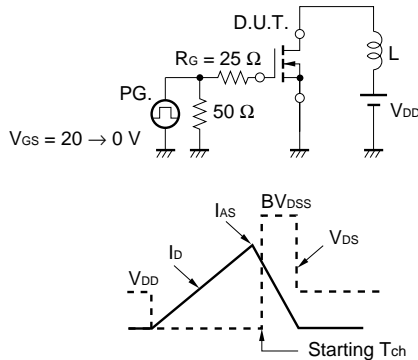


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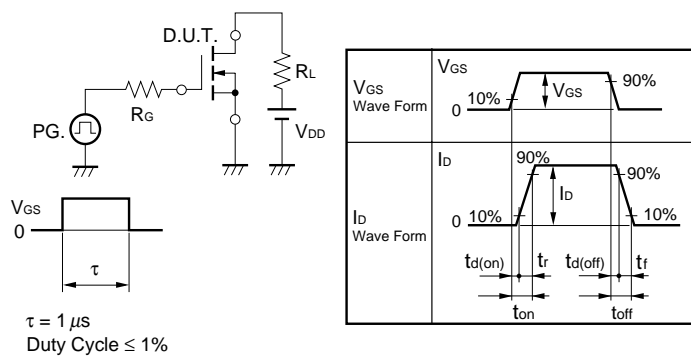
ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 40 V, V _{GS} = 0 V			10	μA
Gate Leakage Current	I _{GSS}	V _{GS} = ±20 V, V _{DS} = 0V			±10	μA
Gate Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance	y _{fs}	V _{DS} = 10 V, I _D = 40 A	20	40		S
Drain to Source On-state Resistance	R _{DS(on)1}	V _{GS} = 10 V, I _D = 40 A		5.9	7.3	mΩ
	R _{DS(on)2}	V _{GS} = 4 V, I _D = 40 A		10.5	15	mΩ
Input Capacitance	C _{iss}	V _{DS} = 10 V,		2800		pF
Output Capacitance	C _{oss}	V _{GS} = 0 V,		730		pF
Reverse Transfer Capacitance	C _{rss}	f = 1 MHz		320		pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 20 V, I _D = 40 A		110		ns
Rise Time	t _r	V _{GS} = 10 V		1800		ns
Turn-off Delay Time	t _{d(off)}	R _G = 10 Ω		170		ns
Fall Time	t _f			350		ns
Total Gate Charge	Q _G	V _{DD} = 32 V		50		nC
Gate to Source Charge	Q _{GS}	V _{GS} = 10 V		10		nC
Gate to Drain Charge	Q _{GD}	I _D = 80 A		14		nC
Body Diode Forward Voltage	V _{F(S-D)}	I _F = 80 A, V _{GS} = 0 V		1.0		V
Reverse Recovery Time	t _{rr}	I _F = 80 A, V _{GS} = 0 V		50		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 100 A/μs		77		nC

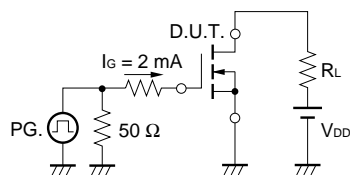
TEST CIRCUIT 1 AVALANCHE CAPABILITY



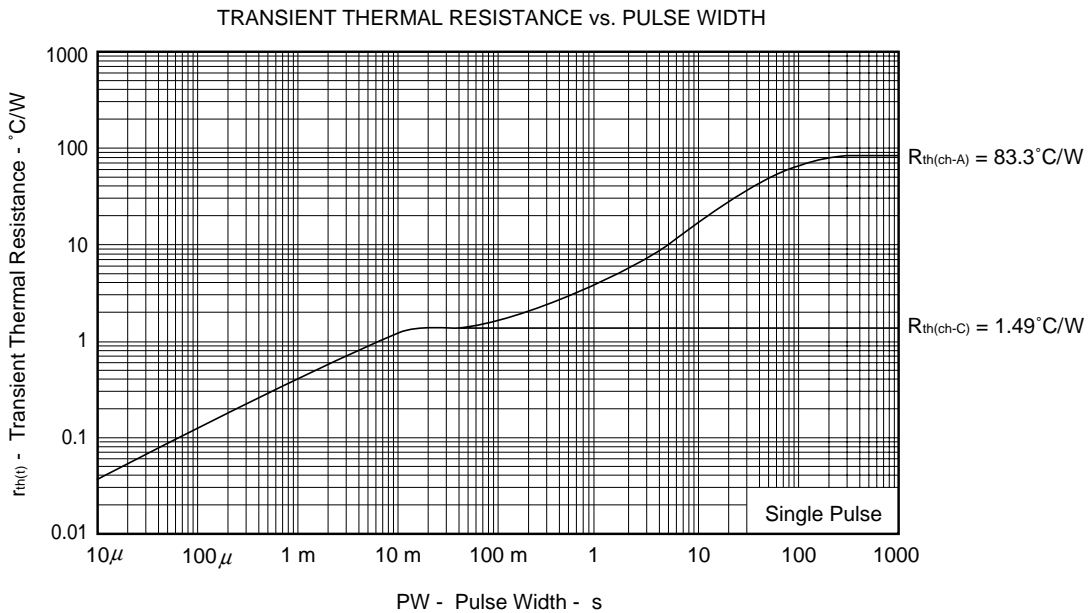
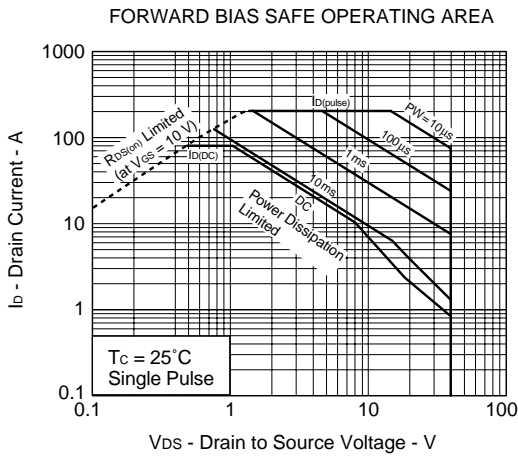
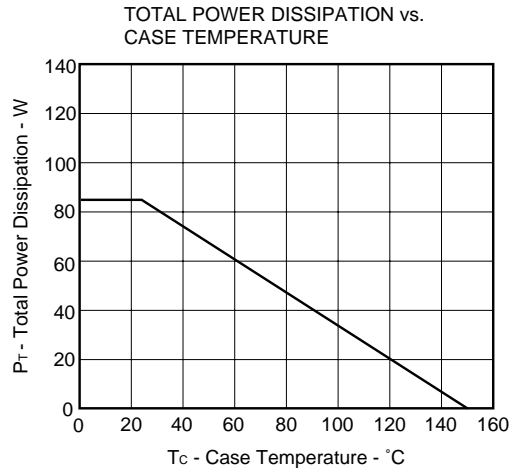
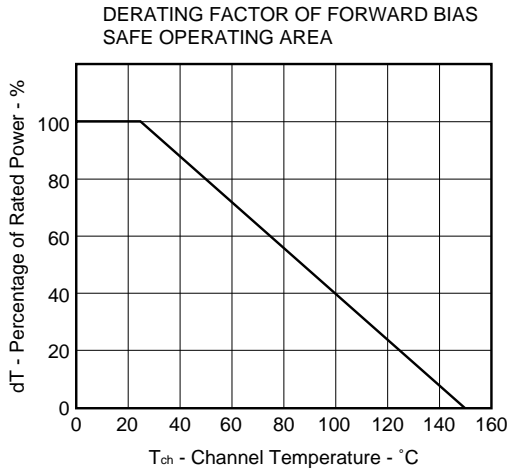
TEST CIRCUIT 2 SWITCHING TIME



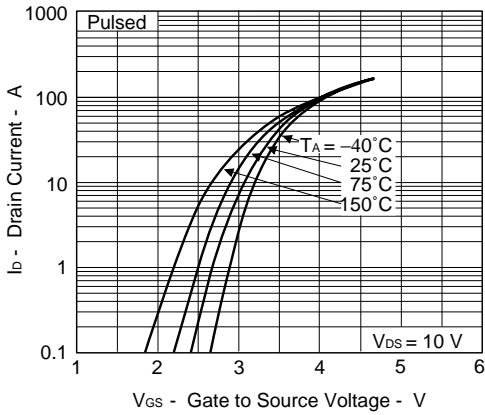
TEST CIRCUIT 3 GATE CHARGE



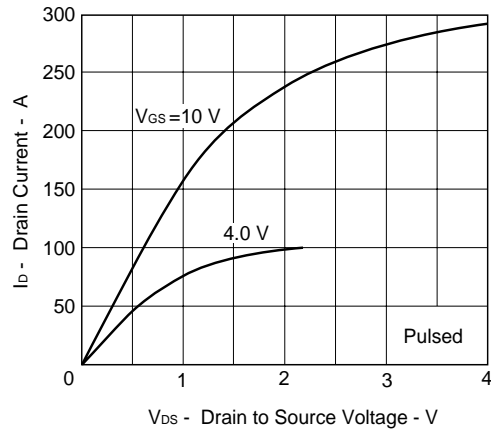
TYPICAL CHARACTERISTICS (T_A = 25 °C)



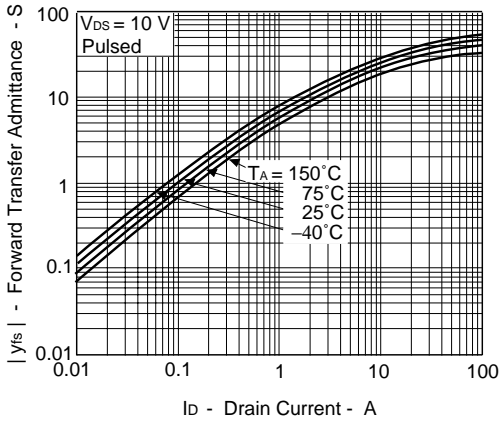
FORWARD TRANSFER CHARACTERISTICS



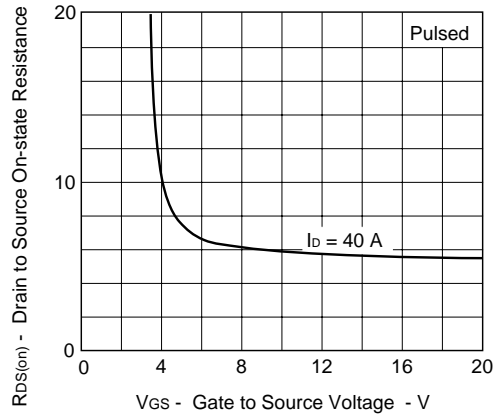
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



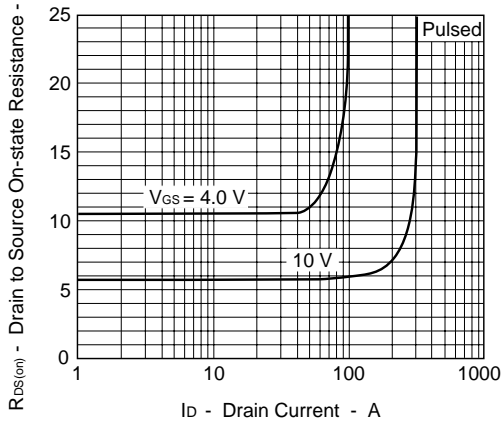
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



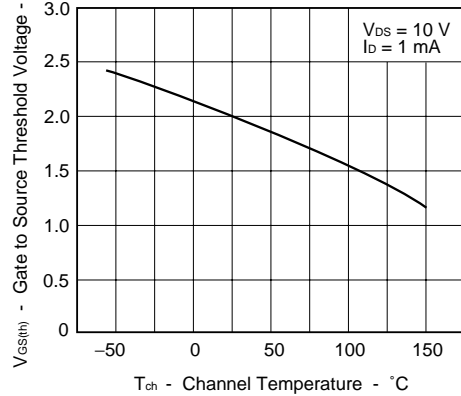
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



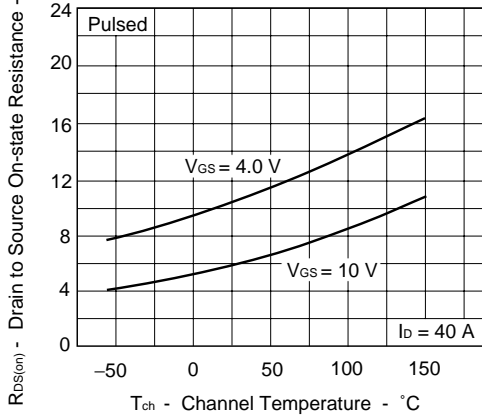
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



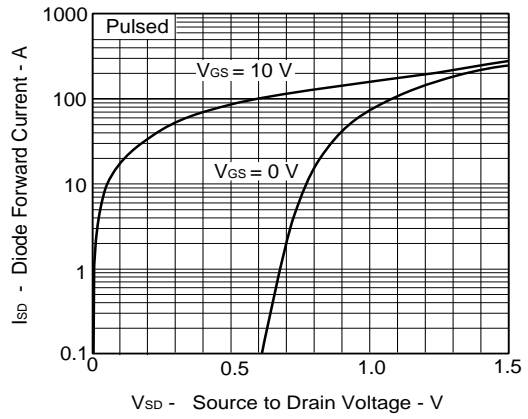
GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE



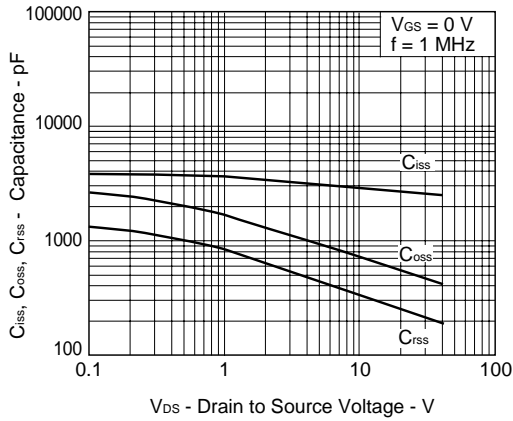
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



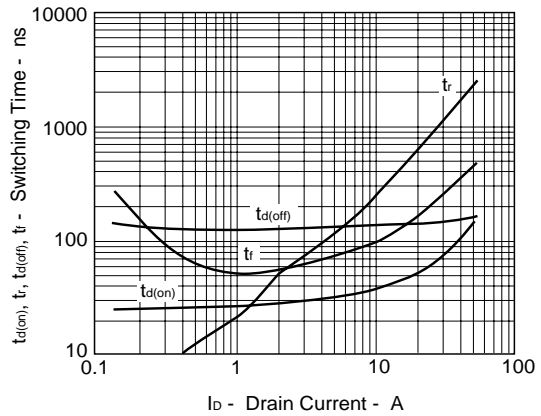
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



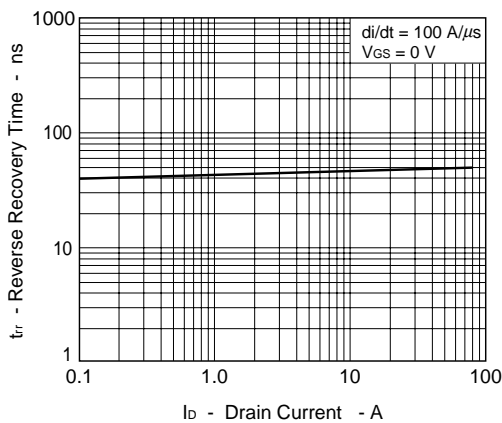
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



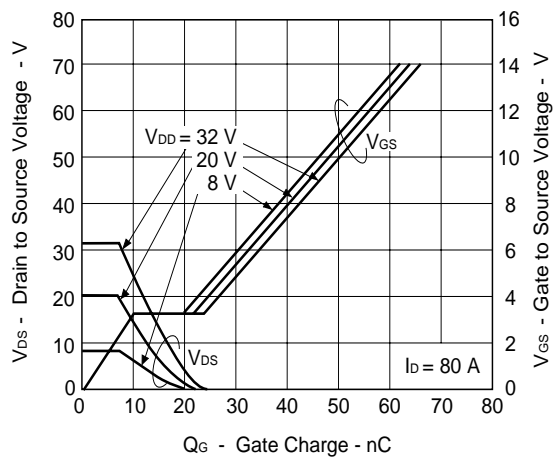
SWITCHING CHARACTERISTICS

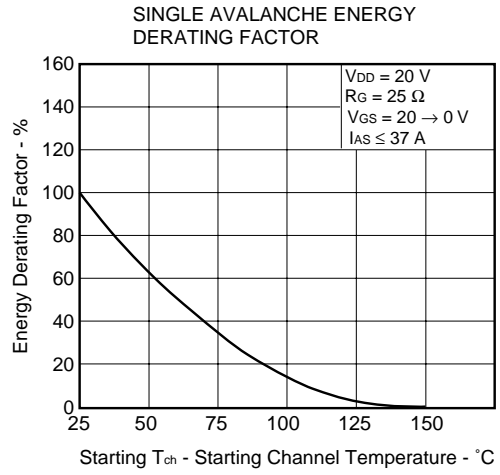
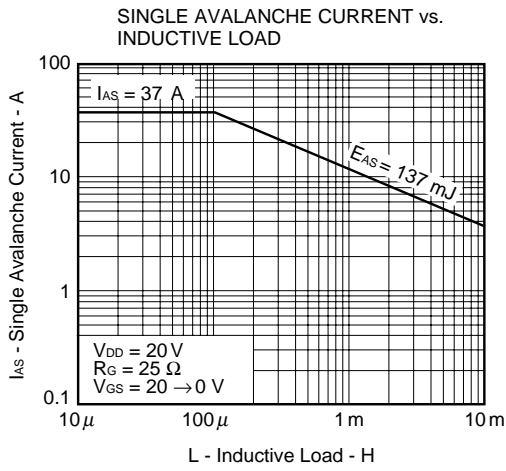


REVERSE RECOVERY TIME vs. DRAIN CURRENT



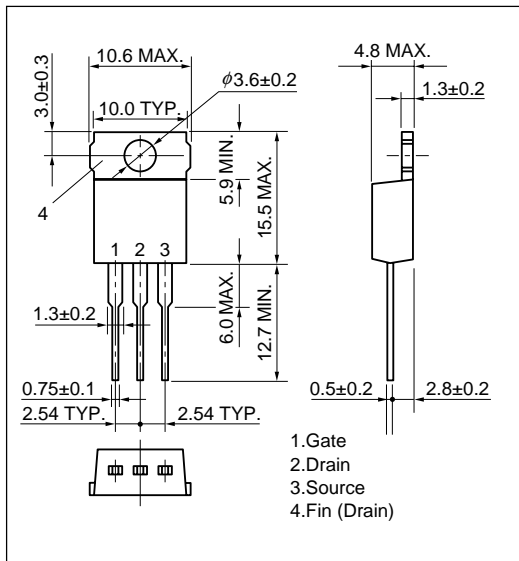
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



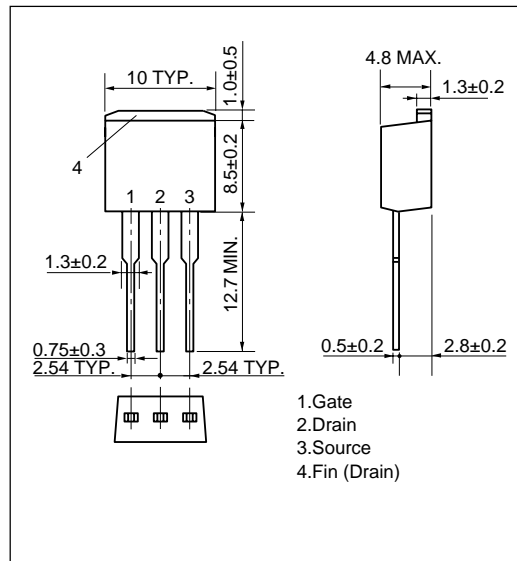


★ PACKAGE DRAWINGS (Unit: mm)

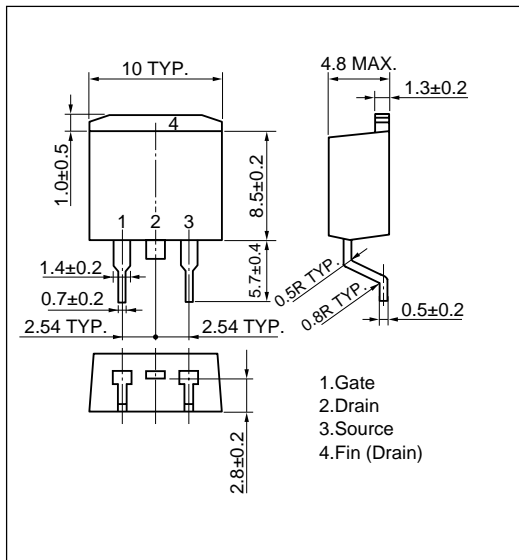
1) TO-220AB(MP-25)



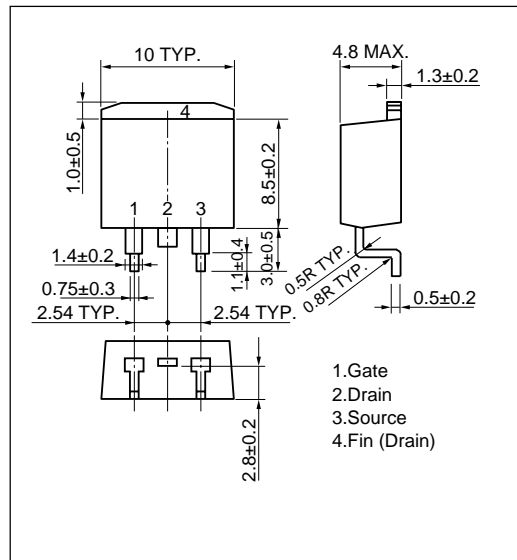
2) TO-262(MP-25 Fin Cut)



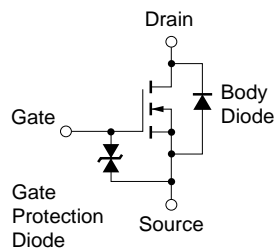
3) TO-263 (MP-25ZJ)



4) TO-220SMD (MP-25Z)^{Note}



EQUIVALENT CIRCUIT



Note This package is produced only in Japan.

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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