

SWITCHING
N-CHANNEL POWER MOS FET

DESCRIPTION

The 2SK3455 is N-channel DMOS FET device that features a low gate charge and excellent switching characteristics, designed for high voltage applications such as switching power supply, AC adapter.

FEATURES

- Low gate charge
 $Q_G = 30 \text{ nC TYP. (} V_{DD} = 400 \text{ V, } V_{GS} = 10 \text{ V, } I_D = 12 \text{ A)}$
- Gate voltage rating $\pm 30 \text{ V}$
- Low on-state resistance
 $R_{DS(on)} = 0.60 \Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 6.0 \text{ A)}$
- Avalanche capability ratings
- Isolated TO-220 package

ORDERING INFORMATION

PART NUMBER	PACKAGE
2SK3455	Isolated TO-220

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	500	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	± 30	V
Drain Current (DC) ($T_C = 25^\circ\text{C}$)	$I_{D(DC)}$	± 12	A
Drain Current (Pulse) ^{Note1}	$I_{D(pulse)}$	± 36	A
Total Power Dissipation ($T_A = 25^\circ\text{C}$)	P_{T1}	2.0	W
Total Power Dissipation ($T_C = 25^\circ\text{C}$)	P_{T2}	50	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$
Single Avalanche Current ^{Note2}	I_{AS}	12	A
Single Avalanche Energy ^{Note2}	E_{AS}	103	mJ

Notes 1. $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

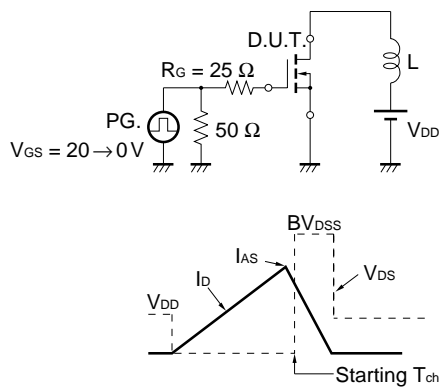
2. Starting $T_{ch} = 25^\circ\text{C}$, $V_{DD} = 150 \text{ V}$, $R_G = 25 \Omega$, $V_{GS} = 20 \rightarrow 0 \text{ V}$

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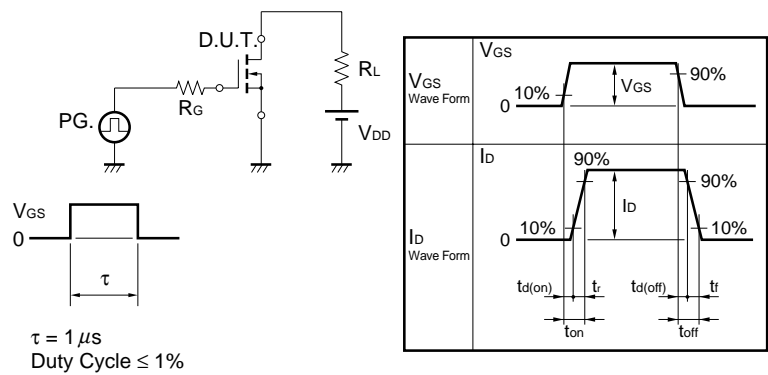
ELECTRICAL CHARACTERISTICS (T_A = 25°C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I _{bss}	V _{DS} = 500 V, V _{GS} = 0 V			100	μA
Gate Leakage Current	I _{GSS}	V _{GS} = ±30 V, V _{DS} = 0 V			±100	nA
Gate Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	2.5		3.5	V
Forward Transfer Admittance	y _{fs}	V _{DS} = 10 V, I _D = 6.0 A	2.0			S
Drain to Source On-state Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 6.0 A		0.50	0.60	Ω
Input Capacitance	C _{iss}	V _{DS} = 10 V		1620		pF
Output Capacitance	C _{oss}	V _{GS} = 0 V		250		pF
Reverse Transfer Capacitance	C _{rss}	f = 1 MHz		10		pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 150 V, I _D = 6.0 A		24		ns
Rise Time	t _r	V _{GS} = 10 V		18		ns
Turn-off Delay Time	t _{d(off)}	R _G = 10 Ω		50		ns
Fall Time	t _f			15		ns
Total Gate Charge	Q _G	V _{DD} = 400 V		30		nC
Gate to Source Charge	Q _{GS}	V _{GS} = 10 V		9		nC
Gate to Drain Charge	Q _{GD}	I _D = 12 A		11		nC
Body Diode Forward Voltage	V _{F(S-D)}	I _F = 12 A, V _{GS} = 0 V		1.0		V
Reverse Recovery Time	t _{rr}	I _F = 12 A, V _{GS} = 0 V		1.5		μs
Reverse Recovery Charge	Q _{rr}	di/dt = 50 A/μs		11		μC

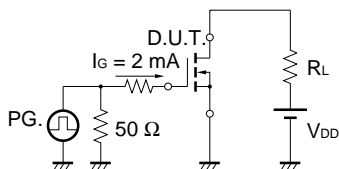
TEST CIRCUIT 1 AVALANCHE CAPABILITY



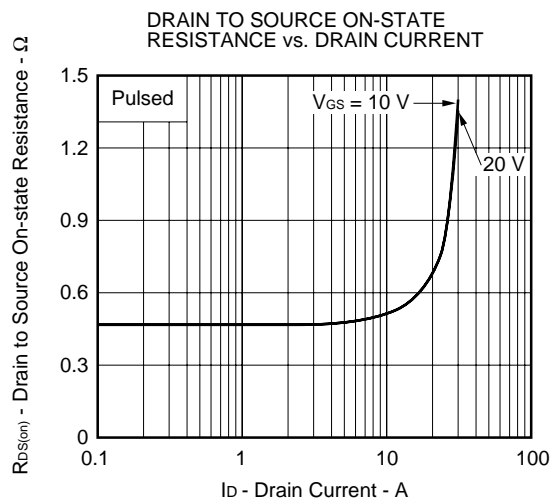
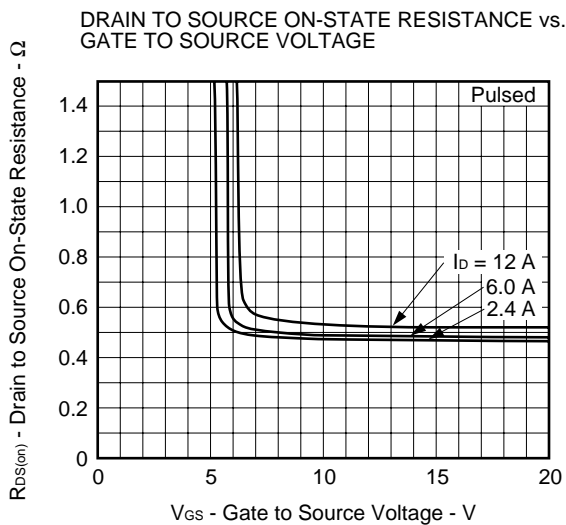
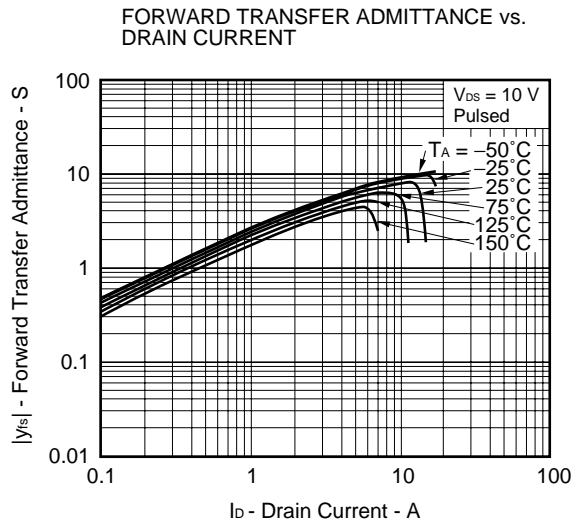
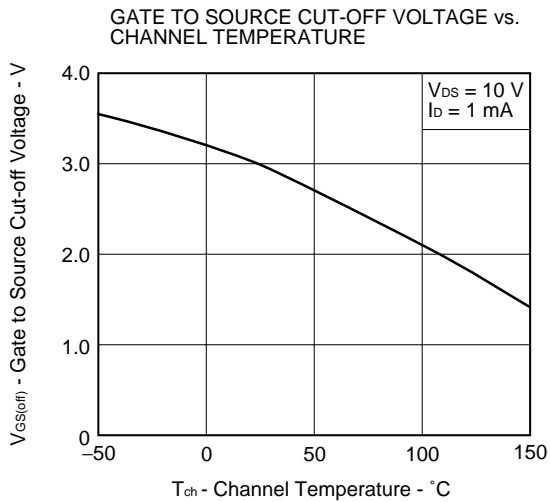
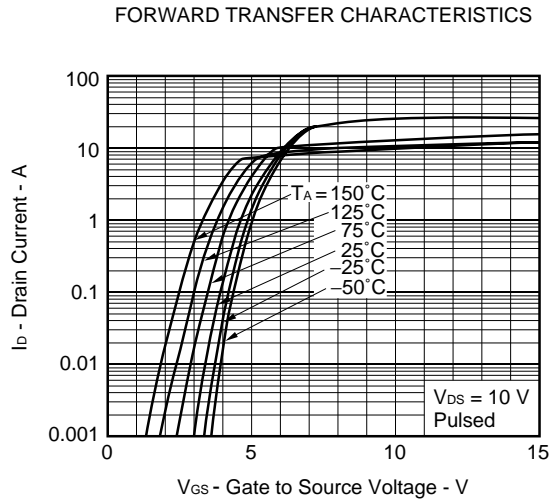
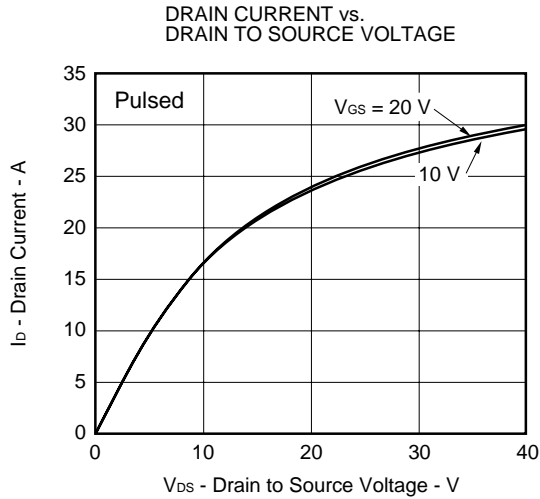
TEST CIRCUIT 2 SWITCHING TIME

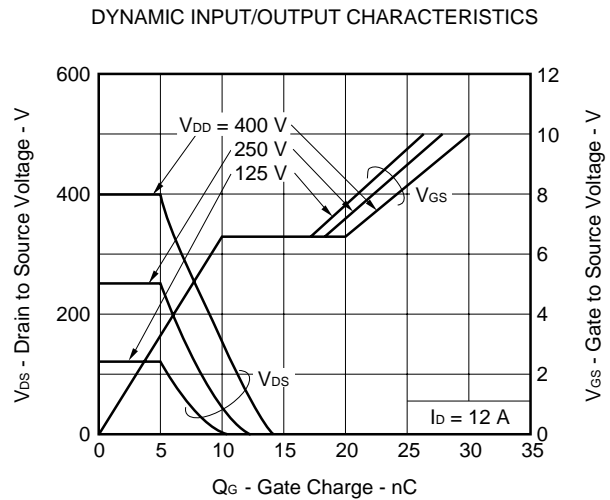
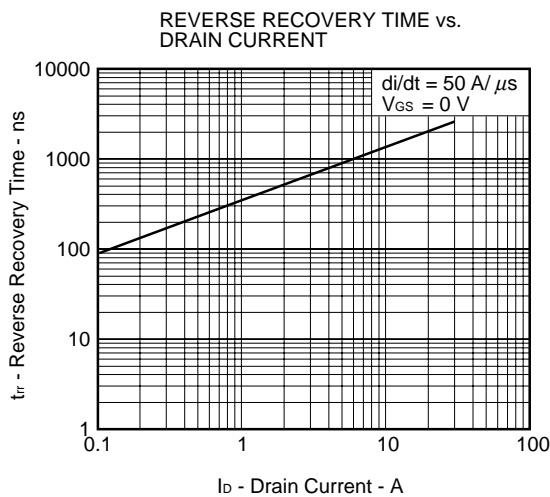
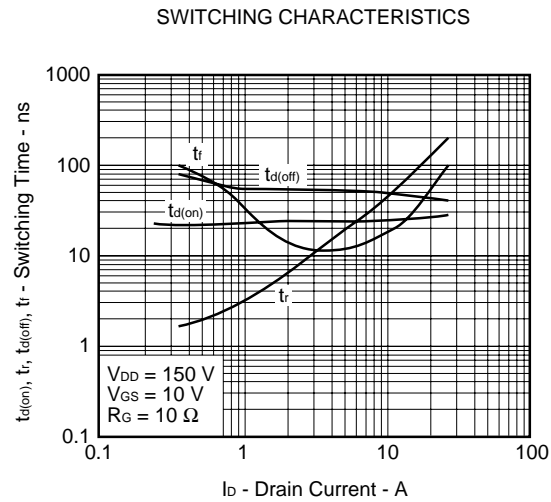
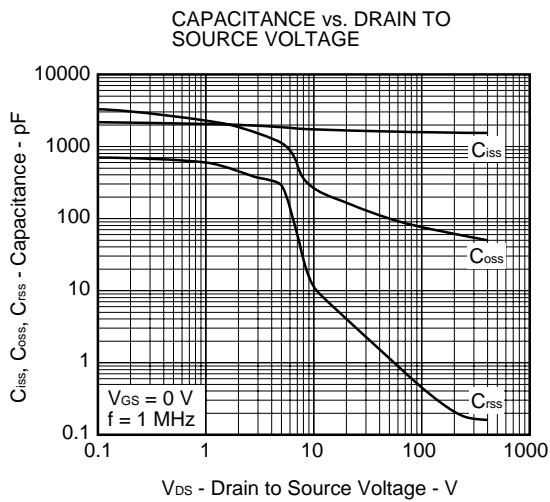
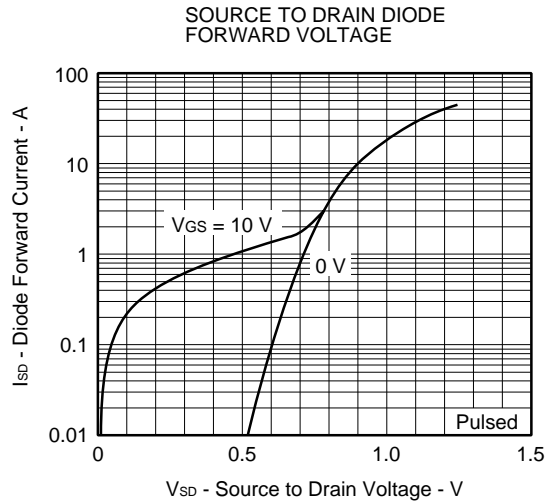
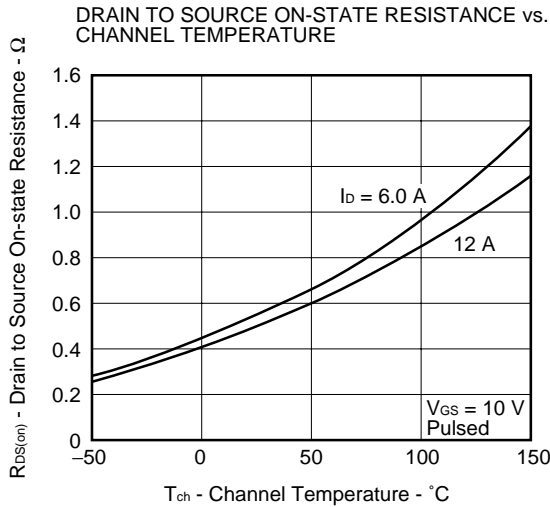


TEST CIRCUIT 3 GATE CHARGE

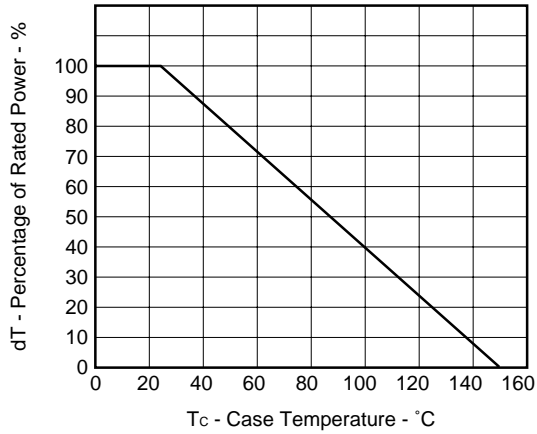


TYPICAL CHARACTERISTICS (T_A = 25°C)

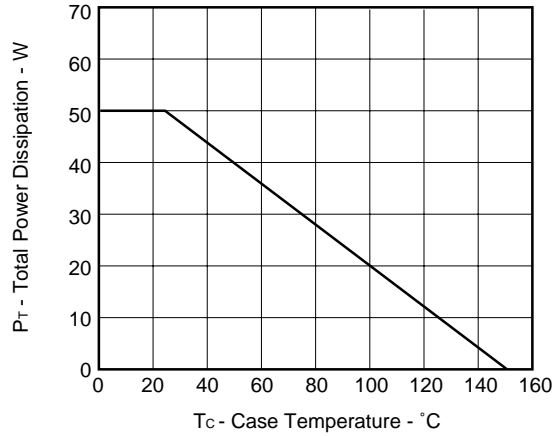




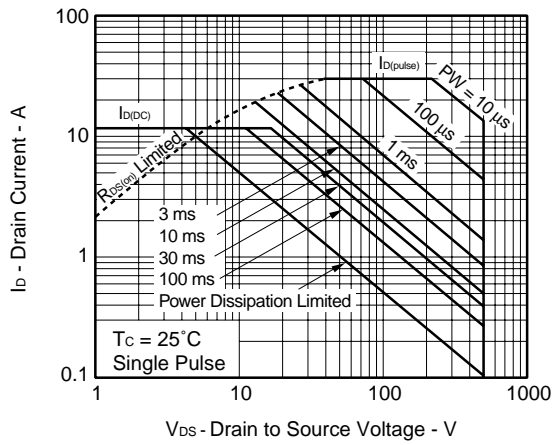
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



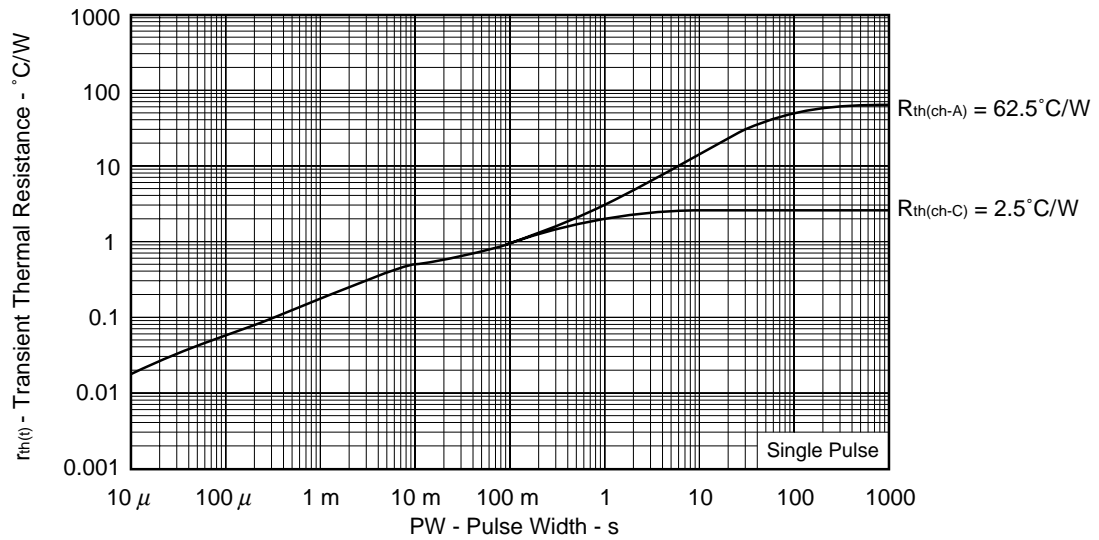
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



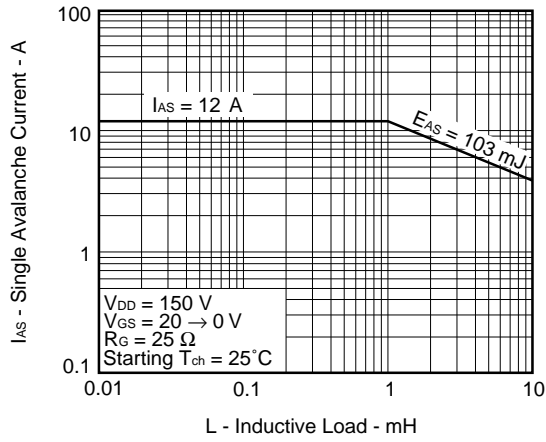
FORWARD BIAS SAFE OPERATING AREA



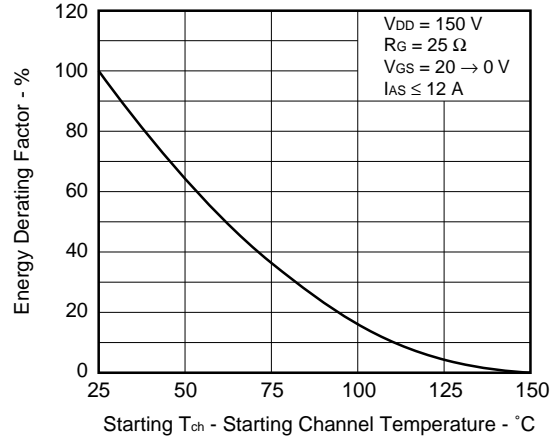
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD

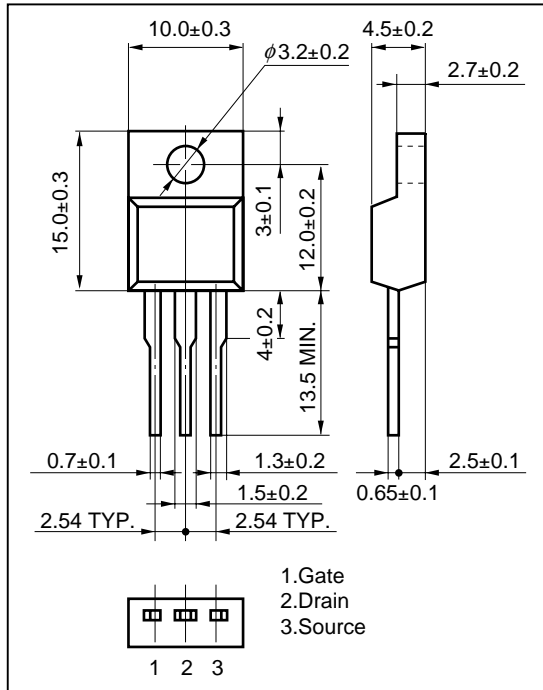


SINGLE AVALANCHE ENERGY DERATING FACTOR

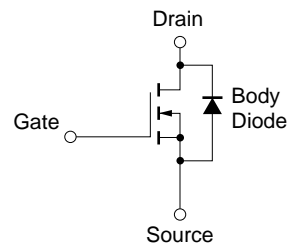


PACKAGE DRAWING (Unit: mm)

Isolated TO-220 (MP-45F)



EQUIVALENT CIRCUIT



Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

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