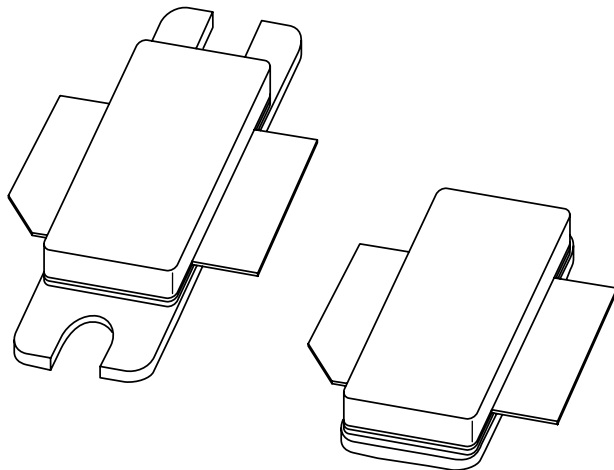


DATA SHEET



BLF0810-180; BLF0810S-180 Base station LDMOS transistors

Product specification
Supersedes data of 2002 Nov 11

2003 May 09

Base station LDMOS transistors

BLF0810-180; BLF0810S-180

FEATURES

- Typical CDMA IS95 performance at standard settings with a supply voltage of 27 V and I_{DQ} of 1130 mA. Adjacent channel bandwidth is 30 kHz, adjacent channel at ± 750 kHz:
 - Output power = 30 W
 - Gain = 16 dB
 - Efficiency = 27%
 - ACPR = -46 dBc at 750 kHz and BW = 30 kHz
- Easy power control
- Excellent ruggedness
- High power gain
- Excellent thermal stability
- Designed for broadband operation (800 to 1000 MHz)
- Internally matched for ease of use.

APPLICATIONS

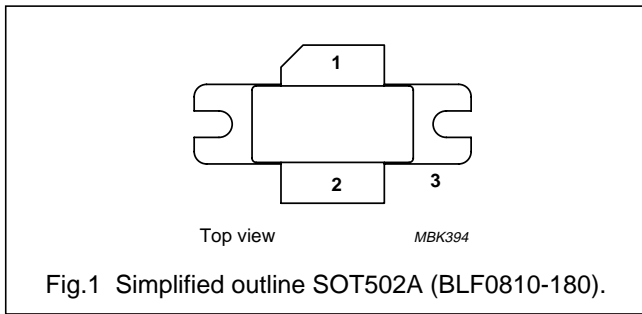
- Common source class-AB operation applications in the 860 to 960 MHz frequency range
- CDMA and multicarrier applications.

DESCRIPTION

180 W LDMOS power transistor for base station applications at frequencies from 800 to 1000 MHz.

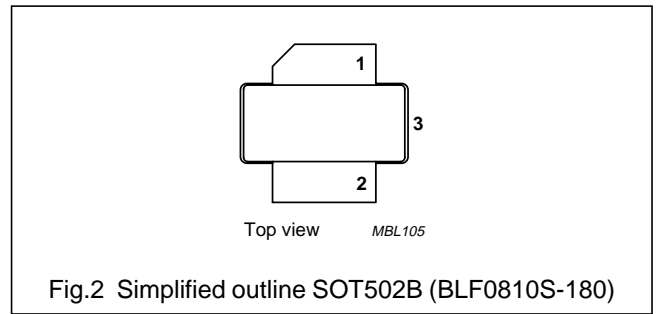
PINNING - SOT502A

PIN	DESCRIPTION
1	drain
2	gate
3	source; connected to flange



PINNING - SOT502B

PIN	DESCRIPTION
1	drain
2	gate
3	source; connected to flange



QUICK REFERENCE DATA

Typical RF performance at $T_h = 25$ °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)	d_3 (dBc)	ACPR 750 (dBc)
Class-AB (2-tone)	$f_1 = 890.0; f_2 = 890.1$	27	140 (PEP)	16	39	-28	-
CDMA (IS95)	890	27	30 (AV)	16	27	-	-46

Base station LDMOS transistors

BLF0810-180; BLF0810S-180

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage	–	75	V
V_{GS}	gate-source voltage	–	±15	V
T_{stg}	storage temperature	–65	+150	°C
T_j	junction temperature	–	200	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-c}$	thermal resistance from junction to case	$T_h = 25\text{ °C}$, $P_L = 35\text{ W (AV)}$, note 1	0.42	K/W
$R_{th\ j-hs}$	thermal resistance from heatsink to junction	$T_h = 25\text{ °C}$, $P_L = 35\text{ W (AV)}$, note 2	0.62	K/W

Notes

1. Thermal resistance is determined under RF operating conditions.
2. Depending on mounting condition in application.

CHARACTERISTICS

$T_j = 25\text{ °C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0$; $I_D = 3\text{ mA}$	75	–	–	V
V_{GSth}	gate-source threshold voltage	$V_{DS} = 10\text{ V}$; $I_D = 300\text{ mA}$	4	–	5	V
I_{DSS}	drain-source leakage current	$V_{GS} = 0$; $V_{DS} = 36\text{ V}$	–	–	3	μA
I_{DSX}	on-state drain current	$V_{GS} = V_{GSth} + 9\text{ V}$; $V_{DS} = 10\text{ V}$	45	–	–	A
I_{GSS}	gate leakage current	$V_{GS} = \pm 20\text{ V}$; $V_{DS} = 0$	–	–	1	μA
g_{fs}	forward transconductance	$V_{DS} = 10\text{ V}$; $I_D = 10\text{ A}$	–	9	–	S
R_{DSon}	drain-source on-state resistance	$V_{GS} = 9\text{ V}$; $I_D = 10\text{ A}$	–	60	–	mΩ

Base station LDMOS transistors

BLF0810-180; BLF0810S-180

APPLICATION INFORMATION

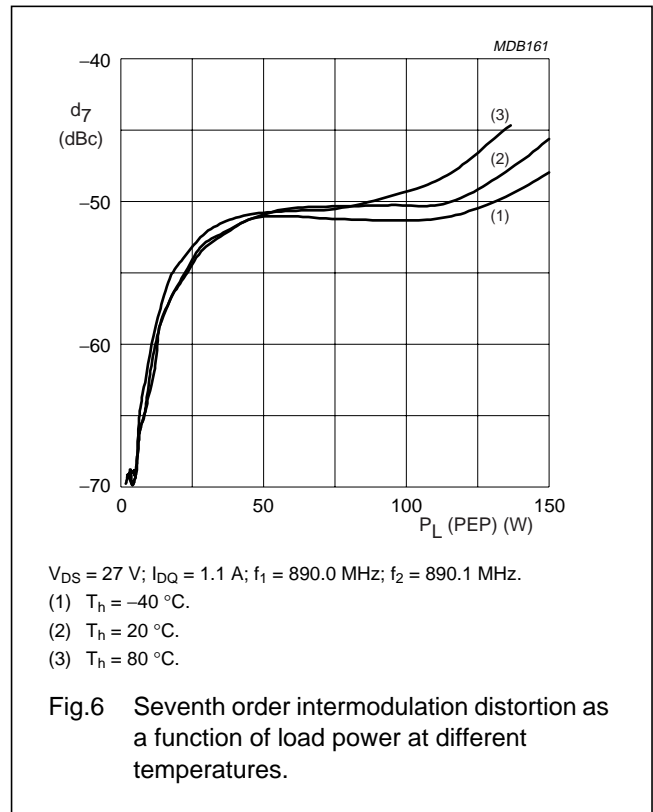
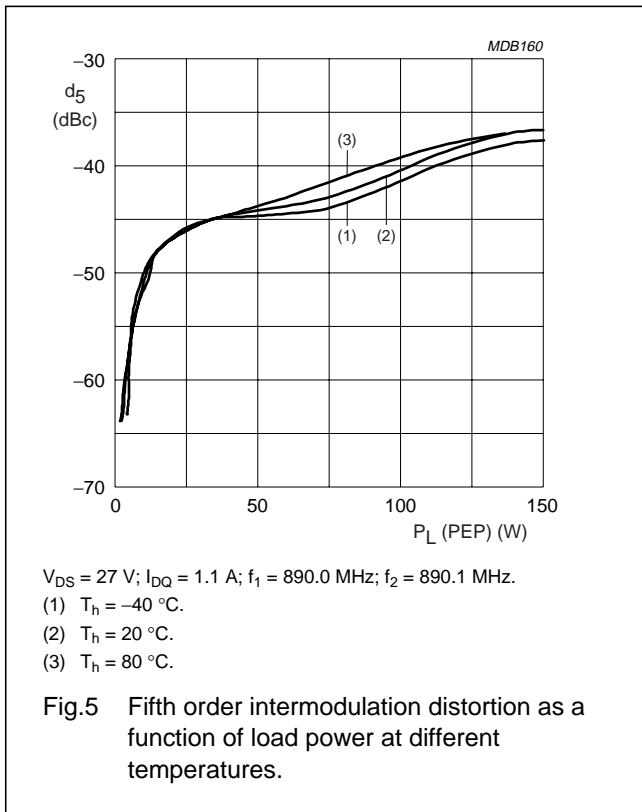
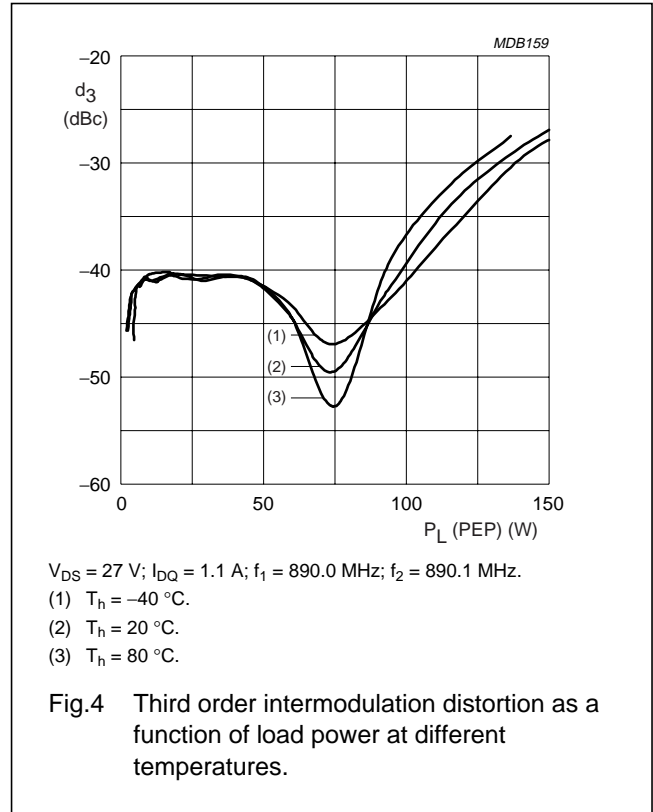
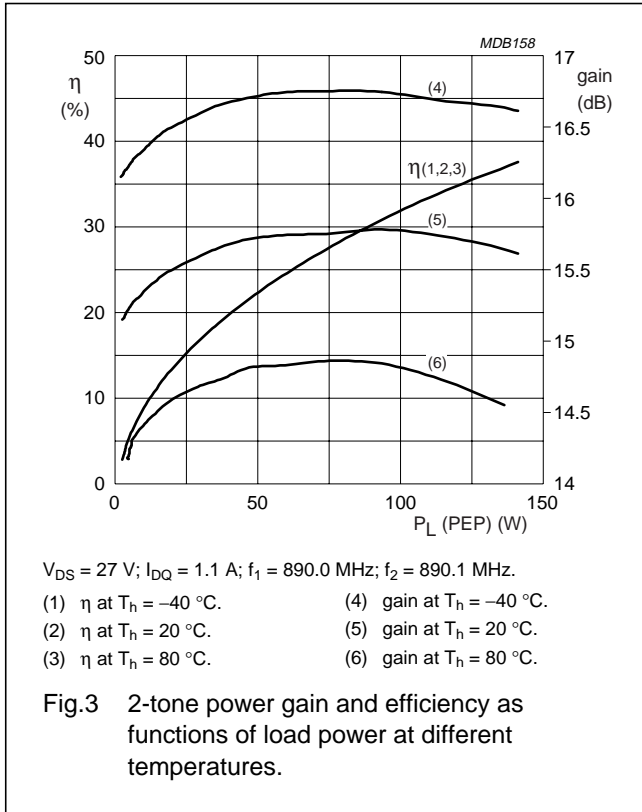
RF performance in a common source class-AB circuit.

$V_{DS} = 27$ V; $I_{DQ} = 1130$ mA; $f = 890$ MHz; $T_h = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Mode of operation: 2-tone CW, 100 kHz spacing						
G_p	gain power	$P_L = 90$ W (PEP)	15	16	–	dB
η_D	drain efficiency		24	30	–	%
IRL	input return loss		–	–13	–6	dB
d_3	third order intermodulation distortion		–	–40	–	dBc
G_p	gain power	$P_L = 125$ W (PEP)	–	16	–	dB
η_D	drain efficiency		33	37	–	%
d_3	third order intermodulation distortion		–	–32	–27	dBc
	ruggedness	VSWR = 15 : 1 through all phases; $P_L = 125$ W (PEP)	no degradation in output power			
Mode of operation: CDMA, IS95 (pilot, paging, sync and traffic codes 8 to 13)						
G_p	gain power	$P_L = 30$ W (AV)	–	16	–	dB
η_D	drain efficiency	$P_L = 30$ W (AV)	–	27	–	%
ACPR 750	adjacent channel power ratio	at BW = 30 kHz	–	–46	–	dBc

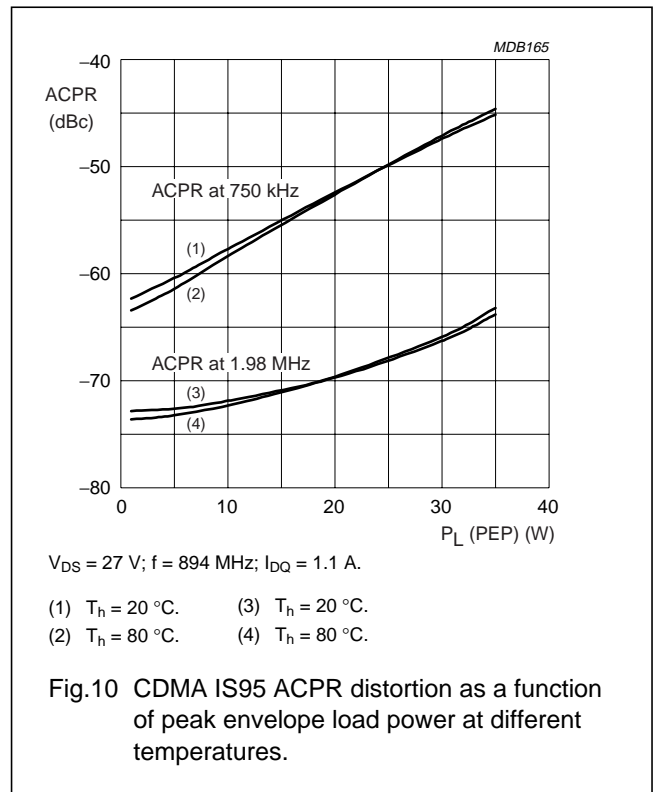
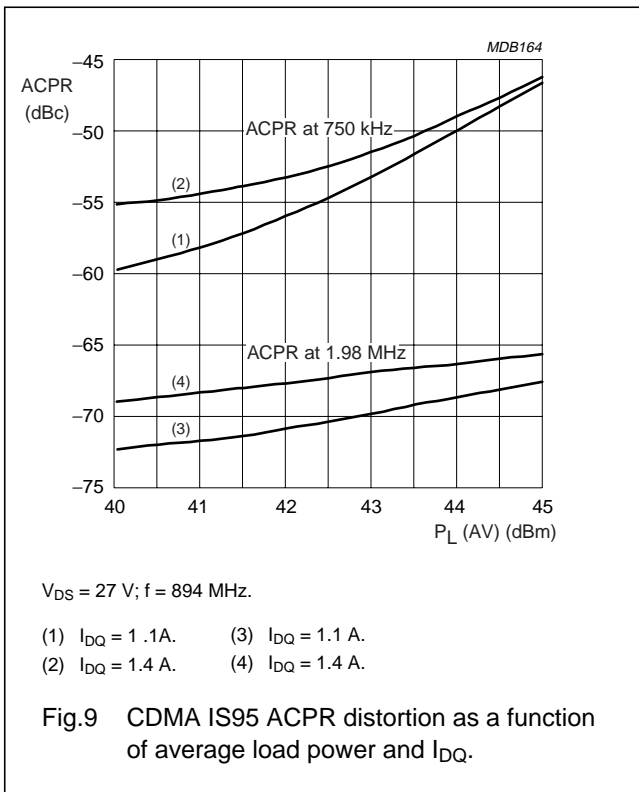
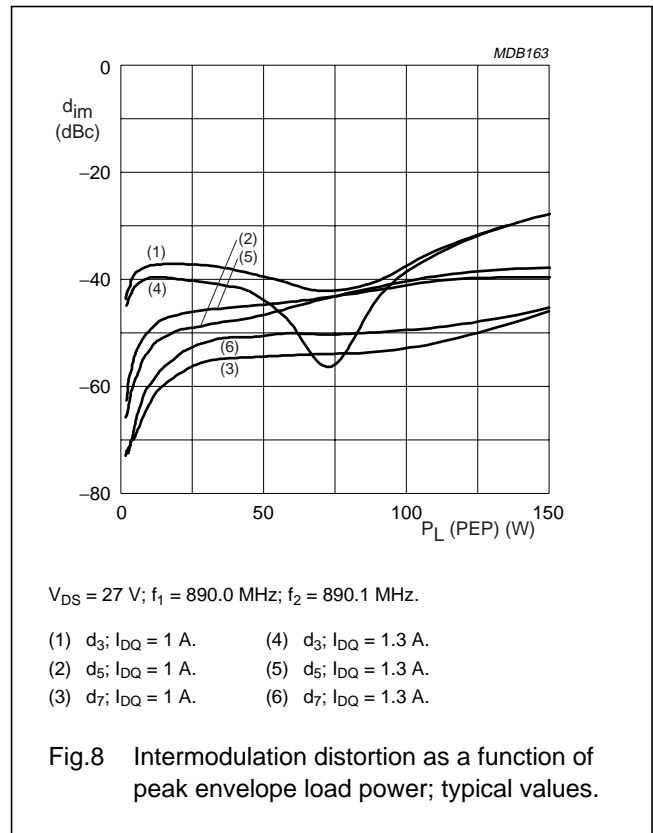
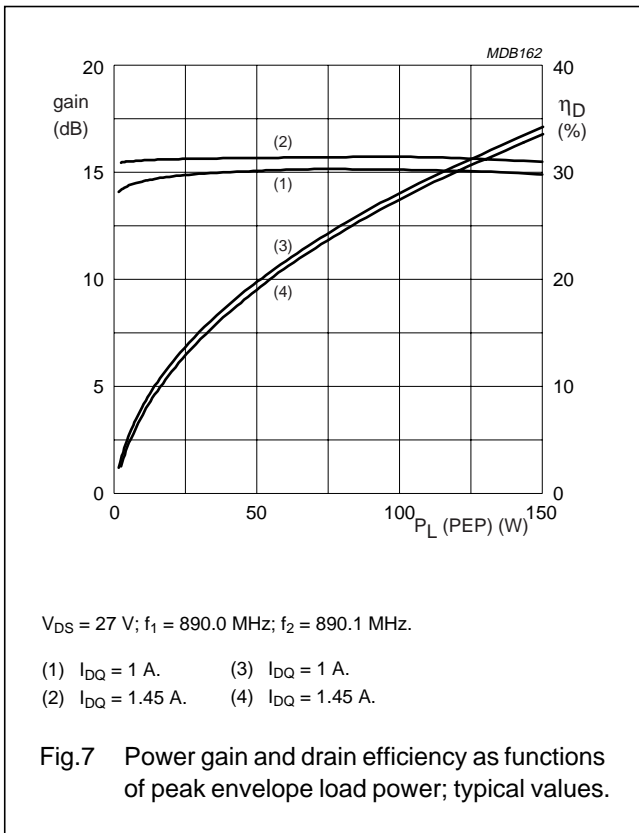
Base station LDMOS transistors

BLF0810-180; BLF0810S-180



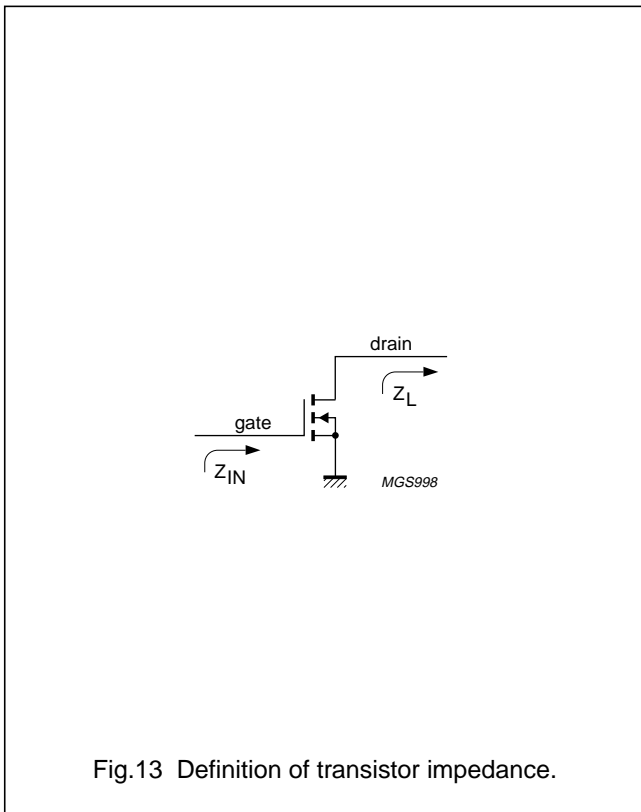
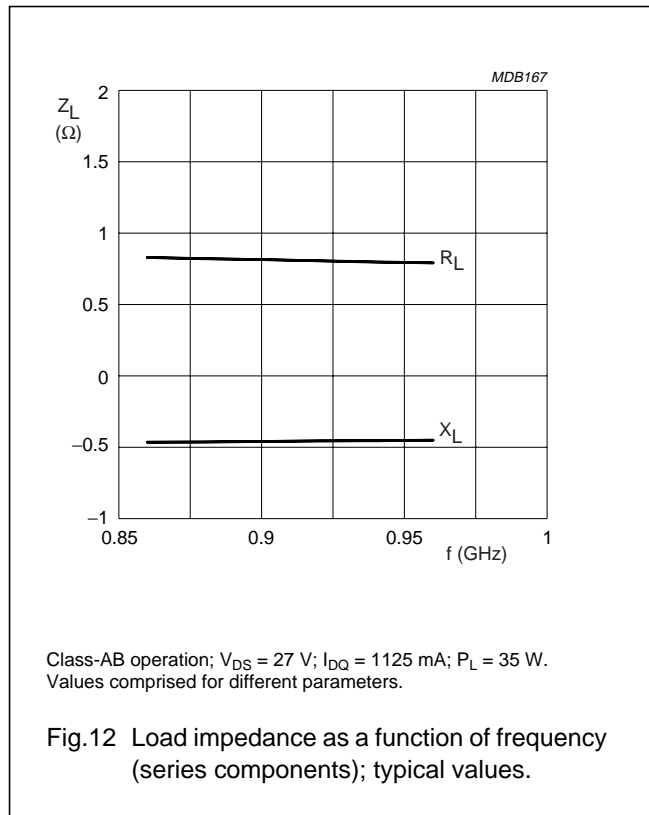
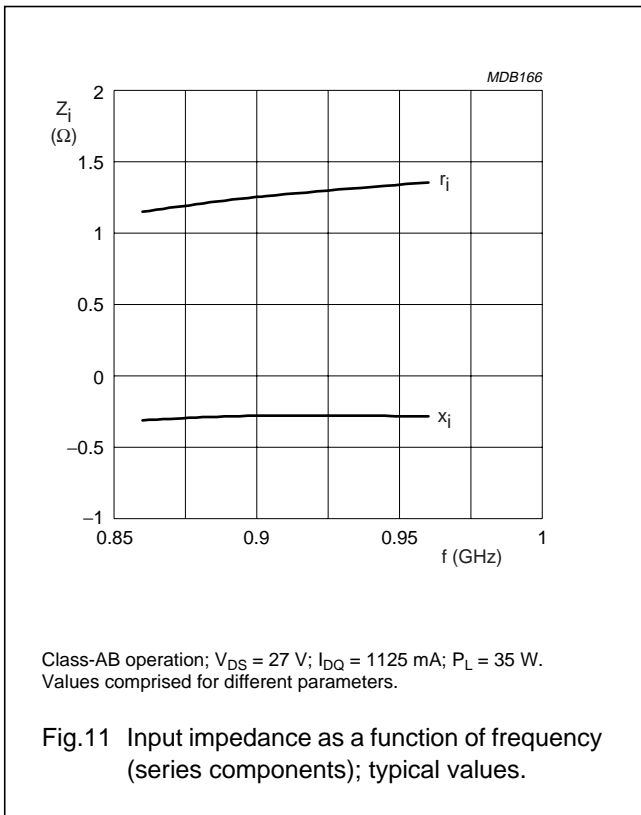
Base station LDMOS transistors

BLF0810-180; BLF0810S-180



Base station LDMOS transistors

BLF0810-180; BLF0810S-180



Base station LDMOS transistors

BLF0810-180; BLF0810S-180

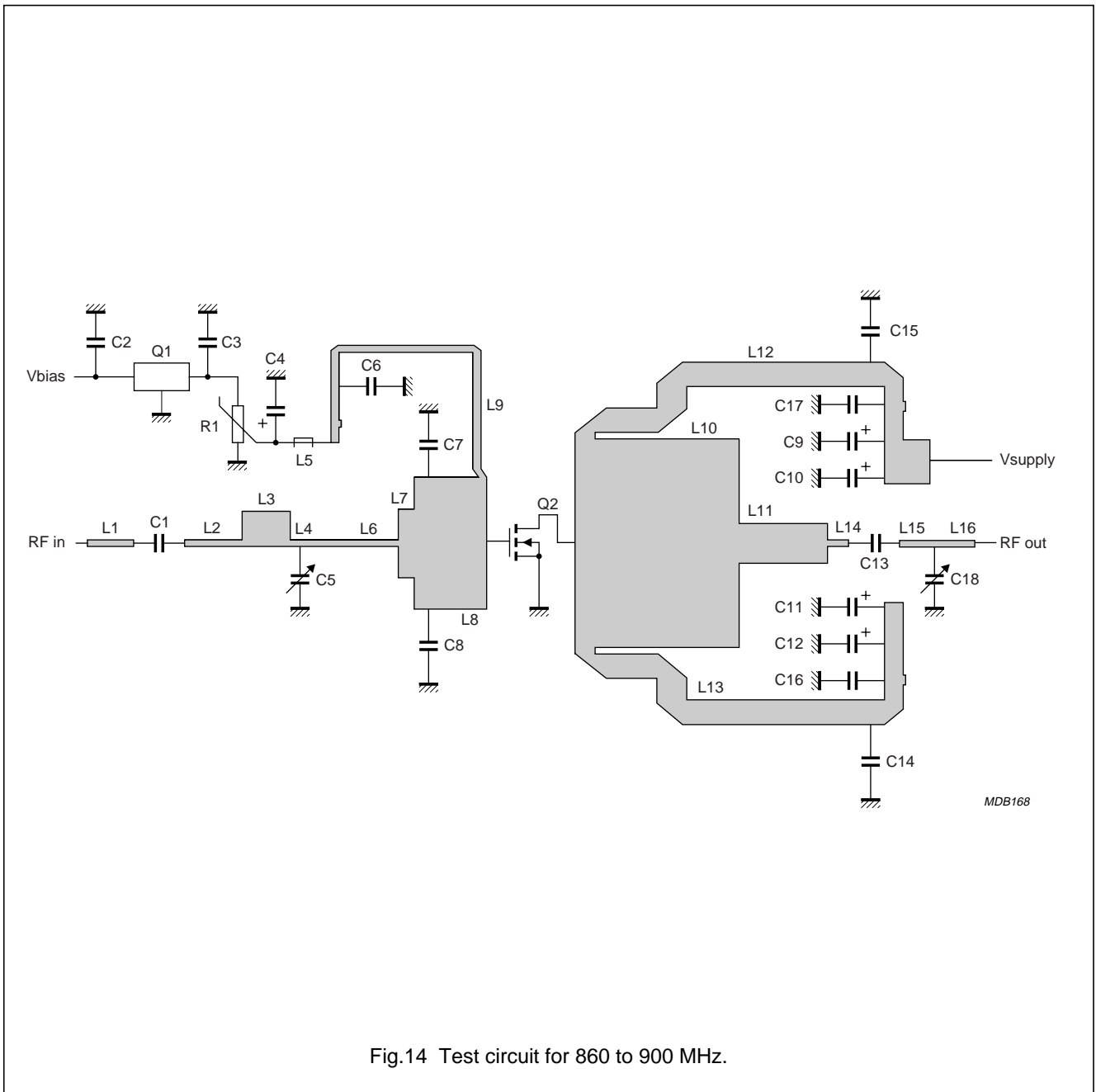
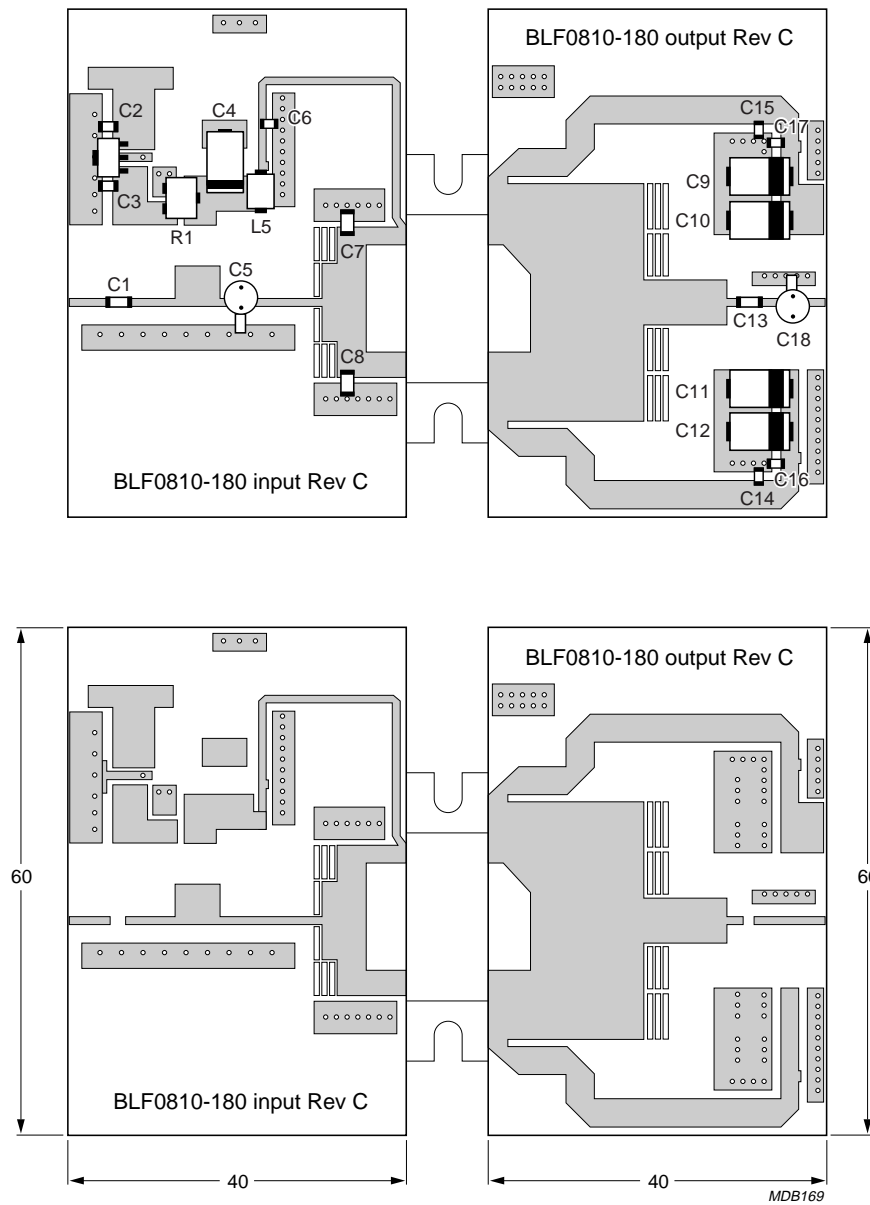


Fig.14 Test circuit for 860 to 900 MHz.

Base station LDMOS transistors

BLF0810-180; BLF0810S-180



Dimensions in mm.

The components are situated on one side of the copper-clad Rogers 6006 printed-circuit board ($\epsilon_r = 6.15$); thickness = 25 mm. The other side is unetched and serves as a ground plane.

Fig.15 Component layout for 860 to 900 MHz test circuit.

Base station LDMOS transistors

BLF0810-180; BLF0810S-180

List of components (see Figs 14 and 15)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS
C1, C6, C13, C14, C15, C16, C17	multilayer ceramic chip capacitor; note 1	68 pF	
C2	multilayer ceramic chip capacitor; note 1	330 nF	
C3	multilayer ceramic chip capacitor; note 1	100 nF	
C4, C9, C10, C11, C12	tantalum capacitor	10 μ F	
C5, C18	air trimmer capacitor	5 pF	
C7, C8	multilayer ceramic chip capacitor	8.2 pF	
R1	potentiometer	1 k Ω	
Q1	7808 voltage regulator		
Q2	BLF0810-180/BLF0810-180S LDMOS transistor		
L1	stripline; note 2		5.22 \times 0.92 mm
L2	stripline; note 2		6.47 \times 0.92 mm
L3	stripline; note 2		5.38 \times 4.8 mm
L4	stripline; note 2		2.4 \times 0.92 mm
L5	ferroxcube		
L6	stripline; note 2		9.73 \times 0.92 mm
L7	stripline; note 2		1.82 \times 9.3 mm
L8	stripline; note 2		8.15 \times 17.9 mm
L9	stripline; note 2		44 \times 0.92 mm
L10	stripline; note 2		18.45 \times 28.3 mm
L11	stripline; note 2		9.95 \times 5.38 mm
L12, L13	stripline; note 2		37.6 \times 3.35 mm
L14	stripline; note 2		2.36 \times 0.92 mm
L15, L16	stripline; note 2		4.22 \times 0.92 mm

Notes

1. American Technical Ceramics type 100A or capacitor of same quality.
2. The striplines are on a double copper-clad Rogers 6006 printed-circuit board ($\epsilon_r = 6.15$); thickness = 0.64 mm

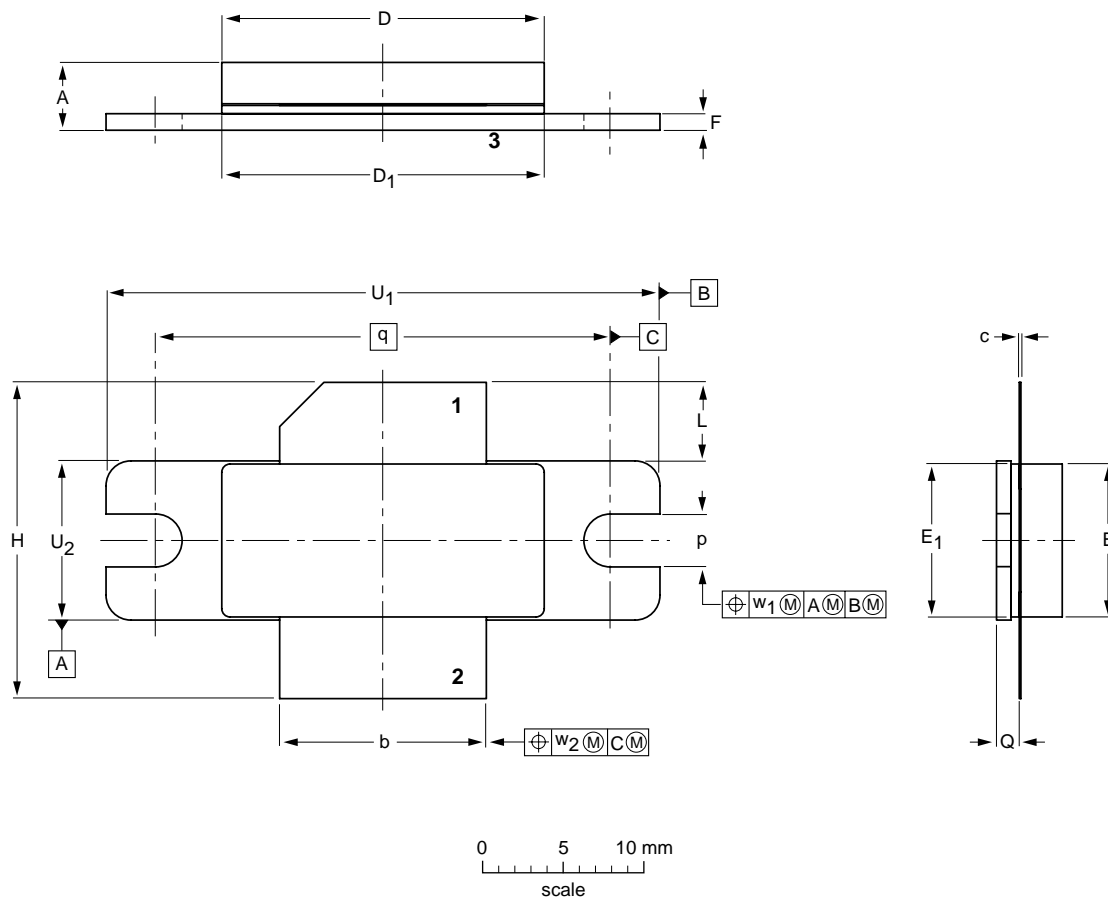
Base station LDMOS transistors

BLF0810-180; BLF0810S-180

PACKAGE OUTLINE

Flanged LDMOST ceramic package; 2 mounting holes; 2 leads

SOT502A



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D ₁	E	E ₁	F	H	L	p	Q	q	U ₁	U ₂	w ₁	w ₂
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	3.38 3.12	1.70 1.45	27.94	34.16 33.91	9.91 9.65	0.25	0.51
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.133 0.123	0.067 0.057	1.100	1.345 1.335	0.390 0.380	0.01	0.02

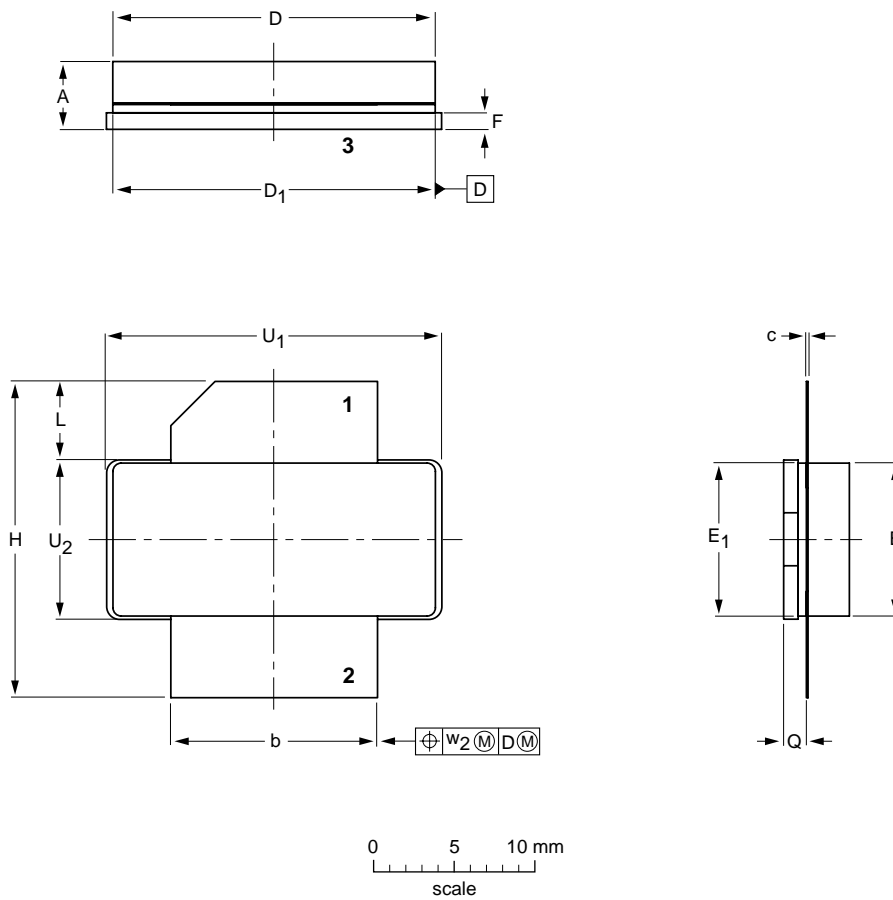
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT502A						99-12-28 03-01-10

Base station LDMOS transistors

BLF0810-180; BLF0810S-180

Earless flanged LDMOST ceramic package; 2 leads

SOT502B



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D ₁	E	E ₁	F	H	L	Q	U ₁	U ₂	w ₂
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	1.70 1.45	20.70 20.45	9.91 9.65	0.25
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.067 0.057	0.815 0.805	0.390 0.380	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT502B						99-12-28- 03-01-10

Base station LDMOS transistors

BLF0810-180; BLF0810S-180

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾⁽³⁾	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.
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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Base station LDMOS transistors

BLF0810-180; BLF0810S-180

NOTES

Base station LDMOS transistors

BLF0810-180; BLF0810S-180

NOTES

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