

VHF power MOS transistor

BLF147

FEATURES

- High power gain
- Low intermodulation distortion
- Easy power control
- Good thermal stability
- Withstands full load mismatch.

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS transistor designed for industrial and military applications in the HF/VHF frequency range.

The transistor is encapsulated in a 4-lead, SOT121 flange envelope, with a ceramic cap. All leads are isolated from the flange.

A marking code, showing gate-source voltage ( $V_{GS}$ ) information is provided for matched pair applications. Refer to 'General' section for further information.

PIN CONFIGURATION

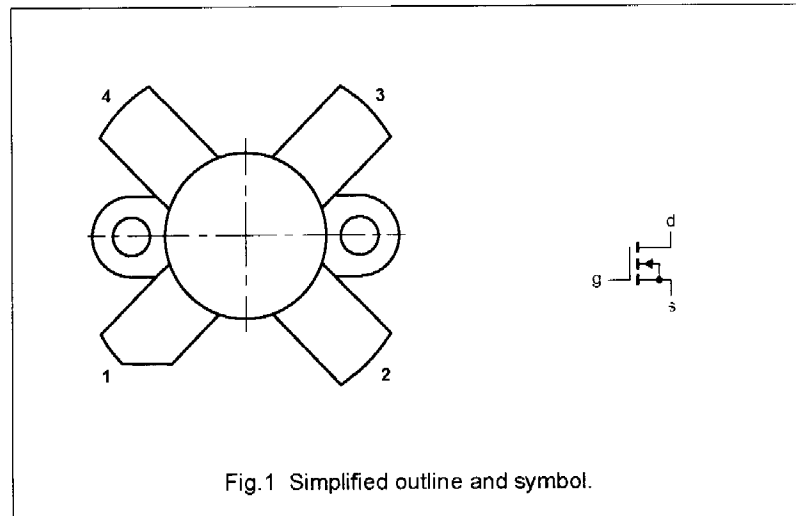


Fig.1 Simplified outline and symbol.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

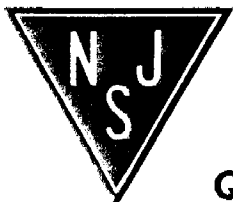
PINNING - SOT121

PIN	DESCRIPTION
1	drain
2	source
3	gate
4	source

QUICK REFERENCE DATA

RF performance at  $T_h = 25^\circ\text{C}$  in a common source test circuit.

MODE OF OPERATION	f (MHz)	$V_{DS}$ (V)	$P_L$ (W)	$G_p$ (dB)	$\eta_D$ (%)	$d_3$ (dB)	$d_5$ (dB)
SSB, class-AB	28	28	150 (PEP)	> 17	> 35	< -30	< -30
CW, class-B	108	28	150	typ. 70	typ. 70	-	-



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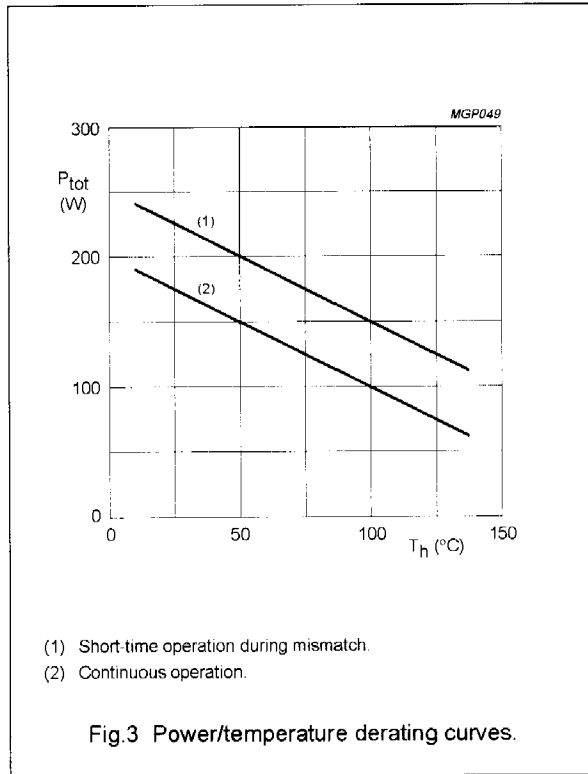
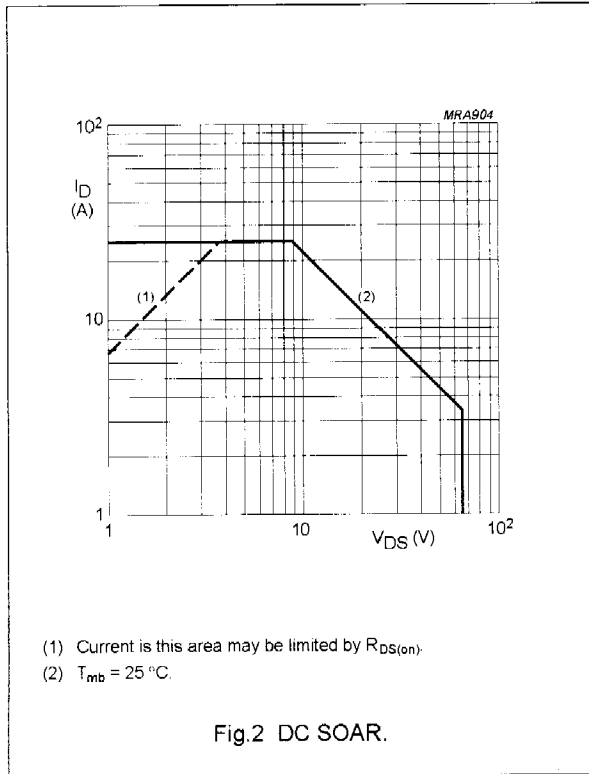
**LIMITING VALUES**

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DS}$	drain-source voltage		-	65	V
$\pm V_{GS}$	gate-source voltage		-	20	V
$I_D$	DC drain current		-	25	A
$P_{tot}$	total power dissipation	up to $T_{mb} = 25\text{ }^\circ\text{C}$	-	220	W
$T_{stg}$	storage temperature		-65	150	$^\circ\text{C}$
$T_j$	junction temperature		-	200	$^\circ\text{C}$

**THERMAL RESISTANCE**

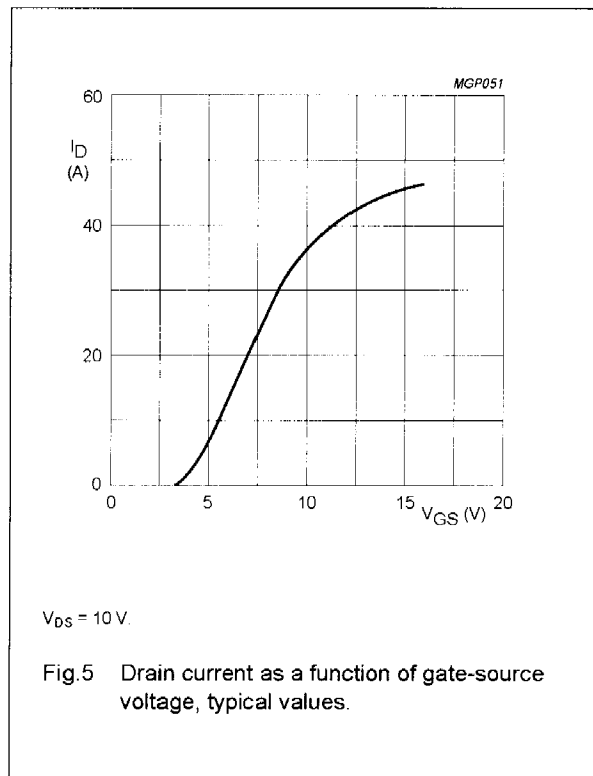
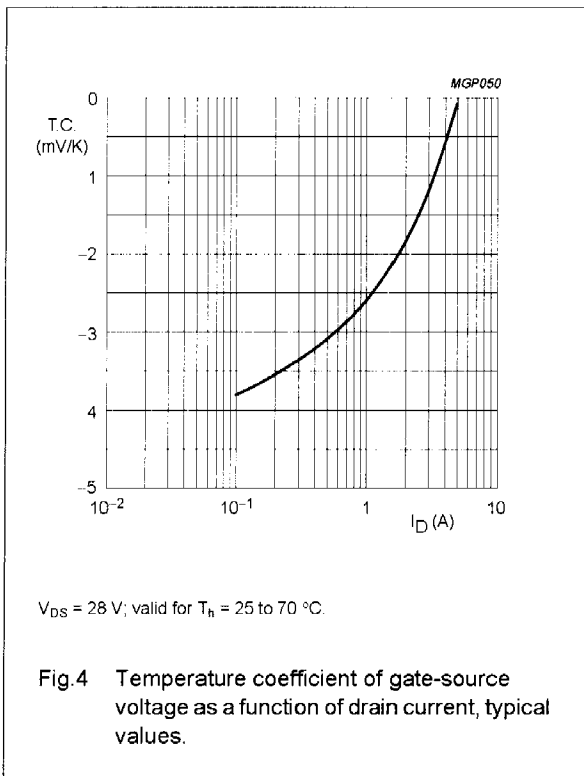
SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j-mb}$	thermal resistance from junction to mounting base	0.8 K/W
$R_{th\ mb-h}$	thermal resistance from mounting base to heatsink	0.2 K/W



**CHARACTERISTICS**

$T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified.

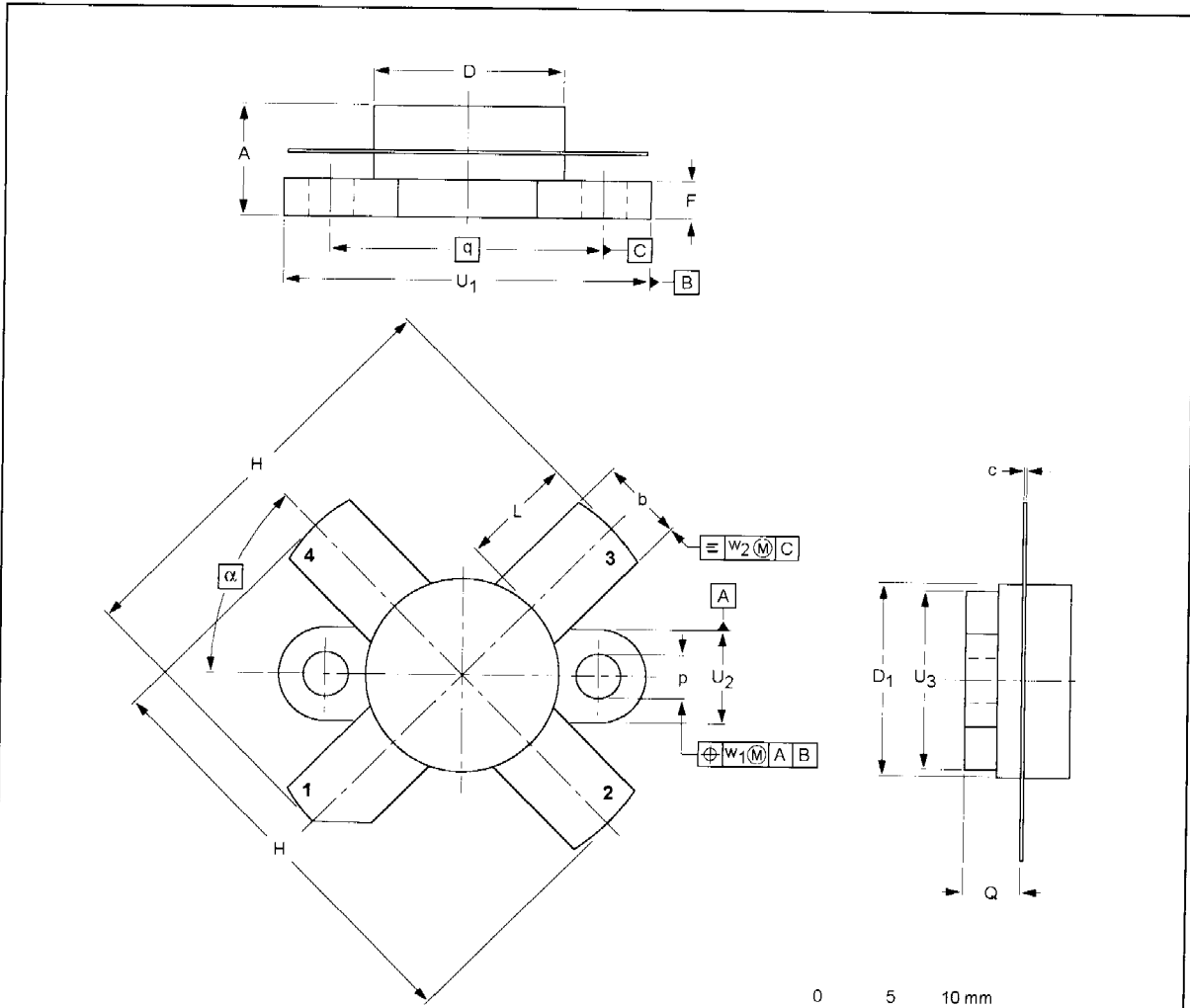
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 100\text{ mA}; V_{GS} = 0$	65	–	–	V
$I_{DSS}$	drain-source leakage current	$V_{GS} = 0; V_{DS} = 28\text{ V}$	–	–	5	mA
$I_{GSS}$	gate-source leakage current	$\pm V_{GS} = 20\text{ V}; V_{DS} = 0$	–	–	1	$\mu\text{A}$
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 200\text{ mA}; V_{DS} = 10\text{ V}$	2	–	4.5	V
$\Delta V_{GS}$	gate-source voltage difference of matched pairs	$I_D = 100\text{ mA}; V_{DS} = 10\text{ V}$	–	–	100	mV
$g_{fs}$	forward transconductance	$I_D = 8\text{ A}; V_{DS} = 10\text{ V}$	5	7.5	–	S
$R_{DS(on)}$	drain-source on-state resistance	$I_D = 8\text{ A}; V_{GS} = 10\text{ V}$	–	0.1	0.15	$\Omega$
$I_{DSX}$	on-state drain current	$V_{GS} = 10\text{ V}; V_{DS} = 10\text{ V}$	–	37	–	A
$C_{iS}$	input capacitance	$V_{GS} = 0; V_{DS} = 28\text{ V}; f = 1\text{ MHz}$	–	450	–	pF
$C_{oS}$	output capacitance	$V_{GS} = 0; V_{DS} = 28\text{ V}; f = 1\text{ MHz}$	–	360	–	pF
$C_{rS}$	feedback capacitance	$V_{GS} = 0; V_{DS} = 28\text{ V}; f = 1\text{ MHz}$	–	55	–	pF



PACKAGE OUTLINE

Flanged ceramic package; 2 mounting holes; 4 leads

SOT121B



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D <sub>1</sub>	F	H	L	p	Q	q	U <sub>1</sub>	U <sub>2</sub>	U <sub>3</sub>	w <sub>1</sub>	w <sub>2</sub>	α
mm	7.27 6.17	5.82 5.56	0.16 0.10	12.86 12.59	12.83 12.57	2.67 2.41	28.45 25.52	7.93 6.32	3.30 3.05	4.45 3.91	18.42	24.90 24.63	6.48 6.22	12.32 12.06	0.51	1.02	45°
inches	0.286 0.243	0.229 0.219	0.006 0.004	0.506 0.496	0.505 0.495	0.105 0.095	1.120 1.005	0.312 0.249	0.130 0.120	0.175 0.154	0.725	0.98 0.97	0.255 0.245	0.485 0.475	0.02	0.04	

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT121B					97-06-28